University of Barishal
Department of Computer Science and Engineering

Course Title: Operating System
Course Code: CSE-2207
2nd Year 2nd Semester (B.Sc.) Final Examination
Admission Session: 2022-2023

Time: 03 Hours **Marks:** 60

N.B.: Answer any **FIVE** questions out of the following. All parts of each question must be answered consecutively. Right side of the question shows the maximum marks.

1. a) Describe the layered structure of an operating system and explain one advantage and one disadvantage of using this structure. [5]

   b) What is system call? Briefly explain the steps taken when a user program invokes a system call. [3]

   c) Differentiate between monolithic, microkernel, and hybrid kernel architectures with one example of each. [4]

2. a) With the help of a diagram, describe the different states of a process in an operating system. [4]

   b) What is Process Control Block (PCB)? List and explain any four types of information stored in a PCB. [5]

   c) Explain the concept of context switching. Why is it necessary and what overheads are associated with it? [3]

3. a) Define CPU scheduling. Consider the following set of processes, with the length of the CPU burst given in milliseconds: [5]

Process	Burst Time	Priority
P1	7	3
P2	5	2
P3	8	3
P4	10	1

   The processes are assumed to have arrived in order P1, P2, P3, P4 all at time 0.

   i) Draw four Gantt charts that illustrate the execution of these processes using the following scheduling algorithms: preemptive priority (a large priority number implies a higher priority) and RR (quantum = 6)
   ii) What is the turnaround time of each process for each of the scheduling algorithms?
   iii) What is the waiting time of each process for each of these scheduling algorithms?
   iv) Which of the algorithms results in the minimum average waiting time (over all processes)?

   b) Explain the concept of scheduling criteria. Describe any four common criteria used to evaluate CPU scheduling algorithms. [3]

   c) Define CPU burst and I/O burst. How do these concepts influence CPU scheduling decisions? [4]

4. a) Define process synchronization. Why is it necessary in a multiprogramming environment? [3]

   b) Describe the Producer-Consumer problem and explain how semaphores can be used to solve it. [4]

   c) Two processes, **P1** and **P2**, share a common variable `counter` initialized to 0. Both processes increment `counter` by 1 in a loop 5 times. The code for incrementing is not protected by any synchronization mechanism. [5]

      i) Explain what problem can occur if both processes execute concurrently.
      ii) Suggest a synchronization mechanism to prevent this problem and briefly explain how it works.

5. a) Describe the **resource allocation graph (RAG)** method for detecting deadlocks. How can a cycle in the graph indicate a deadlock? [4]

b) Consider the following system with 3 processes (P1, P2, P3) and 4 identical resources: [5]

Process	Max Need	Allocation
P1	2	1
P2	2	1
P3	1	0

Determine whether the system is in a **safe state** or a **deadlock state** using the **Banker's algorithm.**

c) Explain the difference between deadlock prevention and deadlock avoidance. Give one example of each. [3]

6. a) A system has memory blocks of sizes: 100 KB, 500 KB, 200 KB, 300 KB, 600 KB. Four processes arrive requesting memory of sizes: 212 KB, 417 KB, 112 KB, 426 KB. [4]

i) Allocate memory to the processes using **Best Fit** strategy. Show the remaining memory in each block after allocation.
ii) Allocate memory to the processes using **Worst Fit** strategy. Show the remaining memory in each block after allocation.
iii) Which allocation strategy is better in terms of minimizing fragmentation? Justify briefly.

b) A system uses paging for memory management. The logical address space of a process is 16 KB, and the physical memory size is 32 KB. The page size is 1 KB. [6]

i) Calculate the number of pages in the logical address space and the number of frames in physical memory.
ii) Draw a diagram showing the mapping from the logical address to the physical address using a page table.
iii) Explain how paging helps to eliminate external fragmentation.
iv) Briefly discuss the advantages and disadvantages of paging.

c) A system has a memory access time of **100 ns**. The **TLB hit ratio** is 80%, and TLB access time is **20 ns**. [2]

i) Compute the **effective memory access time**.
ii) Explain how increasing TLB hit ratio affects performance.

7. a) Define segmentation. A process has segments with base addresses as follows: [4]

Segment	Base Address	Limit
0 (Code)	4000	1000
1 (Data)	6000	500
2 (Stack)	7000	300

Find the **physical address** corresponding to the following logical addresses:
i) Segment 0, offset 500
ii) Segment 1, offset 200
iii) Segment 2, offset 250

b) Describe the concept of a **Translation Lookaside Buffer (TLB)**. How does it improve virtual memory performance? [5]

c) A system uses demand paging and has: [3]

Memory access time = 200 ns
TLB access time = 20 ns
TLB hit ratio = 90%
Page fault service time = 10 µs

i) Calculate the **effective memory access time** considering TLB.
ii) Explain briefly how increasing the TLB hit ratio affects EMAT.

8. a) Describe LRU (Least Recently Used) algorithm for the following reference string 6 2 1 5 4 0 3 0 7 2 3 0 3 2 1. Also calculate the number of page fault for frame size 3. [5]

b) Define following terms: i) CPU Thrashing ii) RAID [4]

c) Define page replacement in virtual memory. Why is it necessary? [3]