DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
UNIVERSITY OF BARISHAL

FINAL EXAMINATION-2013

Course Title: Computer Architecture and Organization

Course Code: CSE-2203

2nd Year, 2nd Semester, Session: 2021-22

Time: 3 hours **Marks:** 60

Answer any Five (5) Questions from the followings.

1. a) Constructing a computer that utilizes only static RAM is technically feasible. Such a system would offer exceptional speed and eliminate the need for cache memory. An assessment of its cost implications is required. 4
   b) Analyze the structure of the "Control Unit". 2
   c) Differentiate the terms architecture and organization in terms of computer. 2
   d) Figure 1 illustrates a partial program execution, showing the relevant portions of memory and CPU registers. The program fragment shows the contents of the memory word at address 940 to the contents of the memory word at address 941 and stores the result in the latter location. Continue the program execution steps until program counter (PC) is 302. 4

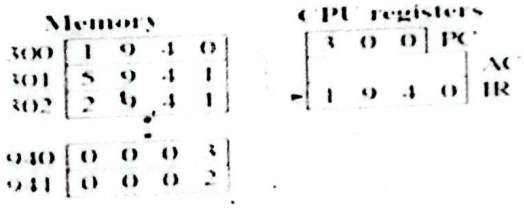

Figure 1: Program execution (initial step) for Ques. 1(d).

2. a) Display the synchronous system bus read/write timing diagram. 6
   b) Regarding Address Bus, Bus width determines maximum memory capacity of system. For example, 8080 has 16 bit address bus. Then how much memory space it will provide ? 2
   c) In interrupt cycle, analyze the step(s) if : (i) no interrupt, (ii) interrupt pending. 4

3. a) In cache memory, overwriting a block before main memory is updated should be avoided. With "Write Through", every write updates both cache and main memory, increasing traffic and slowing performance. To reduce this bottleneck, consider using "Write Back", which updates main memory only when a cache block is replaced. Analyze the concept of "Write Back" in order to avoid the bottleneck of "Write Through". 4
   b) We would like to design a cache of 64kByte. Main memory is 16Mbytes. Cache block is 4 bytes (2 bit word identifier) and rest of bits is block identifier. Use the concept of direct mapping address. 8

4. a) Examine the pros and cons of CD-ROMs. 2
   b) Distinguish between RAID 4 and RAID 5. 3

c) Regarding internal memory, analyze the error correction methods and its correcting code function. 4

d) Discuss about Synchronous DRAM (SDRAM) as external memory. 3

5. a) How can processor performance be evaluated? Explain. 2

b) Describe the multiplexed bus with advantages and disadvantages. 3

b) The ENIAC was a decimal machine, where a register was represented by a ring of 10 vacuum tubes. At any time, only one vacuum tube was in the ON state, representing one of the 10 digits. Assuming that ENIAC had the capability to have multiple vacuum tubes in the ON and OFF state simultaneously, why is this representation "wasteful" and what range of integer values could we represent using the 10 vacuum tubes? 4

c) Discuss the concept of *von Neumann computer architecture*. 3

6. a) In Direct Memory Access (DMA) operation, describe about "Cycle Stealing" 6

b) In I/O controller in computer architecture, O/S works as a resource manager. Discuss this statement with suitable figure(s). 6

7. a) I/O is much slower than the CPU, so the CPU can remain idle even in multi programming systems. What solutions exist to synchronize them? 4

b) What are the key elements of an operating system in computer architecture and organization? Explain with relevant diagrams. 4

c) Analyze the geometric depiction of 4-bit numbers for 2's Complement Integers. 4

8. a) Distinguish between 3-addresses, 2-addresses, 1-address, and 0-addresses instruction with the example $a = b + c$. 8

b) Discuss the concept of associate mapping address in main memory while designing a cache memory. 4

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