DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
UNIVERSITY OF BARISAL

FINAL EXAMINATION-2024

Course Title: Computer Architecture and Organization

Course Code: CSE-2203

Time: 3 hours — 2nd Year, 2nd Semester, Session: [redacted] 20-21 — **Marks:** 60

Answer any Five (5) Questions from the followings.

1. a) How to determine the performance of a processor? 2
   b) Differentiate between SRAM and DRAM. 4
   c) Write short notes on the following: 6
      i) Hit time
      ii) Miss penalty

2. a) Analyze the step(s): (i) no interrupt, (ii) interrupt pending. 4
   b) The ENIAC was a decimal machine, where a register was represented by a ring of 10 vacuum tubes. At any time, only one vacuum tube was in the ON state, representing one of the 10 digits. Assuming that ENIAC had the capability to have multiple vacuum tubes in the ON and OFF state simultaneously, why is this representation "wasteful" and what range of integer values could we represent using the 10 vacuum tubes? 4
   c) Show the Asynchronous timing diagram for system bus Read/Write cycle. 4

3. a) Analyze the concept of "Write Back" in order to avoid the bottleneck of "Write Through" 4
   b) Let's design a cache of 64kByte. Main memory is 16Mbytes. Cache block is 4 bytes (2 bit word identifier) and rest of bits is block identifier. Use the concept of direct mapping address. 8

4. a) What are the differences among direct mapping, associative mapping and set-associative mapping? 4
   b) Assume that there are three (03) small caches, each consisting of eight (08) one-word blocks. One cache is fully associative, a second is two-way set associative, and third is direct mapped. Now, find the number of misses for each cache organization given the following sequence of block address: 5

      0, 8, 0, 6, 8

   c) List and briefly define three (03) techniques for performing I/O. 3

5. a) A computer has a 256 KByte, 4-way set associative, write back data cache with block size of 32 KBytes. The processor sends 32-bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit. Find the number of bits in the tag field for an address. 3
   c) *Von Neumann computer architecture* is the basic computer architecture for the modern computer. Explain this. 5
   d) Describe the multiplexed bus with advantages and disadvantages. 4

6. a) Describe the necessity of I/O modules? 2
   b) In Direct Memory Access (DMA) operation, describe about "Cycle Stealing" 6
   c) Describe O/S as a resource manager in I/O controller. 4

7. a) Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 1 KB. The average seek time is 8 ms, the track-to-track access time is 1.5 ms, and the drive rotates at 3600 rpm. Successive tracks in a cylinder can be read without head movement. 4
      i) What is the disk capacity?
      ii) What is the burst transfer rate?

      Estimate the time required to transfer a 5-MB file.
   b) Briefly describe the data processing and data movement functions of computer. 3
   c) Briefly describe the instruction cycle of program execution. 5

8. a) Define pipelining. Show the timing diagram of pipelining. 4
   b) Explain Processor with an accumulator register. 3
   c) Briefly describe the data processing and data movement functions of computer. 5

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
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FINAL EXAMINATION-2021

Course Title: Computer Architecture and Organization
Course Code: CSE-2203
2nd Year, 2nd Semester, Session: 2019-20

Time: 3 hours **Marks:** 60

Answer any Five (5) Questions from the followings.

1. a) Differentiate between SRAM and DRAM. 4
   b) Explain Moor's Law in Computer architecture. 4
   c) Regarding Cache design, write short notes on the following: 4
      i) Hit time
      ii) Miss penalty

2. a) In interrupt handler, analyze the step(s): (i) no interrupt, (ii) interrupt pending. 4
   b) How much memory space 8080 will provide that has 16 bit address bus ? 2
   c) Describe with figure: Asynchronous timing diagram for system bus Read/Write cycle. 6

3. a) Analyze the concept of "Write Back" in order to avoid the bottleneck of "Write Through". 4
   b) Let's design a cache of 64kByte. Main memory is 16Mbytes. Cache block is 4 bytes (2 bit word identifier) and rest of bits is block identifier. Use the concept of direct mapping address. 8

4. a) What are the differences among direct mapping, associative mapping and set-associative mapping? 4
   b) Assume that there are three (03) small caches, each consisting of eight (08) one-word blocks. One cache is fully associative, a second is two-way set associative, and third is direct mapped. Now, find the number of misses for each cache organization given the following sequence of block address: 5

      0, 8, 0, 6, 8

   c) List and briefly define three (03) techniques for performing I/O. 3

5. a) Explain the performance of a processor. 3
   c) *Von Neumann computer architecture* is the basic computer architecture for the modern computer. Explain this. 5
   d) Describe the multiplexed bus with advantages and disadvantages. 4

6. a) Describe the necessity of I/O modules? 2
   b) In Direct Memory Access (DMA) operation, describe about "Cycle Stealing" 6
   c) Describe O/S as a resource manager in I/O controller. 4

7. a) By Showing the major components of a CPU, briefly describe how a CPU works. 2
   b) Distinguish between RISC and CISC processor. 2
   c) How Stack is organized in CPU ? With proper block diagram, describe following types of stack: (i) Register and (ii) Memory Stack. 8

8. a) Describe how an assembler works with its two phases. 3
   b) Distinguish between 0-addresses, 2-addresses, 3-addresses instruction with the example $a = b + c$. 4
   b) Write two short notes from the below: 5
      i) Op-code, ii) Machine Language, iii) Vector Processor.

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FINAL EXAMINATION-2021
Course Title: Computer Architecture and Organization
Course Code: CSE-2203
2nd Year, 2nd Semester, Session: 2017-18

Time: 3 hours

Marks: 60

Answer any Five (5) Questions from the followings.

1. a) Explain Moor's Law in Computer architecture. 4
   b) Differentiate between SRAM and DRAM. 4
   c) Write short notes on the following: 4
      i) Hit time
      ii) Miss penalty

2. a) Analyze the step(s): (i) no interrupt, (ii) interrupt pending. 4
   b) 8080 has 16 bit address bus. Then how much memory space it will provide? 2
   c) Show the Asynchronous timing diagram for system bus Read/Write cycle. 6

3. a) Analyze the concept of "Write Back" in order to avoid the bottleneck of "Write Through". 4
   b) Let's design a cache of 64kByte. Main memory is 16Mbytes. Cache block is 4 bytes (2 bit word identifier) and rest of bits is block identifier. Use the concept of direct mapping address. 8

4. a) What are the differences among direct mapping, associative mapping and set-associative mapping? 4
   b) Assume that there are three (03) small caches, each consisting of eight (08) one-word blocks. One cache is fully associative, a second is two-way set associative, and third is direct mapped. Now, find the number of misses for each cache organization given the following sequence of block address: 5

      0, 8, 0, 6, 8

   c) List and briefly define three (03) techniques for performing I/O. 3

5. a) Explain the performance of a processor. 3
   c) *Von Neumann computer architecture* is the basic computer architecture for the modern computer. Explain this. 5
   d) Describe the multiplexed bus with advantages and disadvantages. 4

6. a) Describe the necessity of I/O modules? 2
   b) In Direct Memory Access (DMA) operation, describe about "Cycle Stealing" 6
   c) Describe O/S as a resource manager in I/O controller. 4

7. a) What is instruction? Mention the elements of an instruction. 4
   b) Briefly describe the data processing and data movement functions of computer. 3
   c) Briefly describe the instruction cycle of program execution. 5

8. a) Distinguish between 0-addresses, 2-addresses, 3-addresses instruction with the example $a = b + c$. 6
   b) Explain the trade-off (more or less) of the number of addresses for instruction. 6

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
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FINAL EXAMINATION-2020
Course Title: Computer Architecture and Organization
Course Code: CSE-2203
2nd Year, 2nd Semester; **Session:** 2018-19

Time: 3 hours

Answer any Five (5) Questions from the followings. **Marks:** 60

1. a) The ENIAC was a decimal machine, where a register was represented by a ring of 10 vacuum tubes. At any time, only one vacuum tube was in the ON state, representing one of the 10 digits. Assuming that ENIAC had the capability to have multiple vacuum tubes in the ON and OFF state simultaneously, why is this representation "wasteful" and what range of integer values could we represent using the 10 vacuum tubes? [6]

   b) Explain Moor's Law in Computer architecture. [3]

   c) Distinguish between computer architecture and computer organization. [3]

2. a) *Von Neumann computer architecture* is the basic computer architecture for the modern computer. Explain this. [3]

   b) While processor power has raced ahead at breakneck speed, other critical components of the computer have not kept up. The result is a need to look for performance balance: an adjusting of the organization and architecture to compensate for the mismatch among the capabilities of the various components. Nowhere is the problem created by such mismatches more critical than in the interface between processor and main memory.
   There are a number of ways that a system architect can attack this problem, all of which are reflected in contemporary computer designs. Analyse to solve these mismatch between processor and main memory. [5]

   c) Instruction processing consists of two steps: The processor reads (fetches) instructions from memory one at a time and executes each instruction. Program execution consists of repeating the process of instruction fetch and instruction execution. Distinguish between fetch cycle and instruction cycle with suitable figures. [4]

3. a) Interrupts are provided primarily as a way to improve processing efficiency. For example, most external devices are much slower than the processor. Describe with figure(s) for the following:
   (a) No interrupt, b) short I/O wait interrupt, c) long I/O wait interrupt. [3]

   b) Distinguish between traditional bus architecture and high performance bus architecture. [4]

   c) Discuss with figures: Timing of Asynchronous Bus Operations [5]

4. a) Discuss about the memory hierarchy and typical cache organization. [4]

   b) What are the differences among direct mapping, associative mapping, and set-associative mapping? [3]

   c) Discuss the features of Synchronous DRAM (SDRAM). [5]

5. a) Write notes on associative mapping function related to cache memory. [6]

   b) Draw and explain the block diagram of the hardware for implementing the addition and subtraction operation. [6]

6. a) The simplest technique for replacement policy in cache is called write through. Using this technique, all write operations are made to main memory as well as to the cache, ensuring that main memory is always valid. Any other processor–cache module can monitor traffic to main memory to maintain consistency within its own cache. The main disadvantage of this technique is that it generates substantial memory traffic and may create a bottleneck. An alternative technique, known as write back, minimizes memory writes. Discuss the term "write back". [6]

b) RAID 4 involves a write penalty when an I/O write request of small size is performed. Each time that a write occurs, the array management software must update not only the user data but also the corresponding parity bits. [6]
Consider an array of five drives in which X0 through X3 contain data and X4 is the parity disk. Suppose that a write is performed that only involves a strip on dlsk X1. How data can be reconstructed for RAID 4 ?

7. a) Distinguish between RAID 4 and RAID 5? [4]

b) In Direct Memory Access (DMA) operation, describe about "Cycle Stealing" [5]

c) Describe O/S as a resource manager in I/O controller. [3]

8. a) What is the purpose of using addressing mode techniques in computer? [3]

b) How can you classify computer instructions? Explain your idea about logical and bit manipulation instruction. [5]

c) Explain interrupt driven I/O technique. [4]

Good Luck!!!