DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

UNIVERSITY OF BARISAL

Final Examination

Course Title: Digital Logic Design

Course Code: CSE-2103

2nd Year 1st Semester

Session: 2020-21 (Admission Session 2019-20)

Time: 3 hour **Marks:** 60

Answer any five Questions from the followings.

1. a) Implement the Boolean function [3]

$$F = xy + x'y' + y'z$$

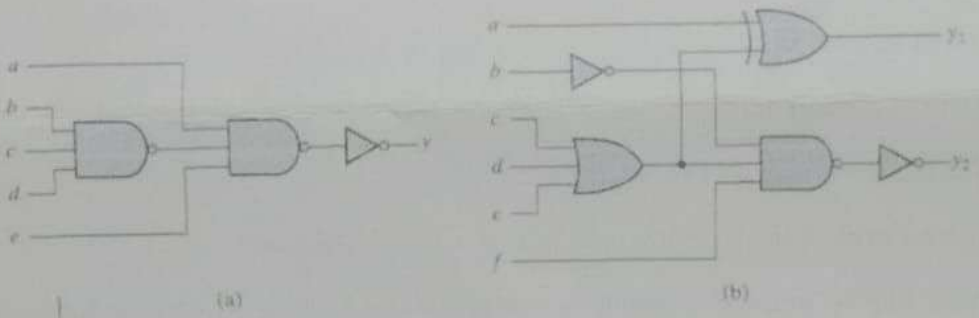
i. With AND, OR, and inverter gates,

ii. With NOR and inverter gates,

iii. With NAND and inverter gates.

b) Show that a positive logic NAND gate is a negative logic NOR gate and vice versa. [3]

c) Write Boolean expressions and construct the truth tables describing the outputs of the circuits described by the following logic diagrams: [6]



2. a) Express the following function as a sum of minterms and as a product of maxrerms: [2]

$$F(A,B,C,D) = B'D + A'D + BD$$

b) Simplify the following Boolean functions, using *Karnaugh* maps: [6]

$$F(w,x,y,z) = \sum(2,3,12,13,14,15)$$

$$F(A,B,C,D) = \sum(0,2,4,5,6,7,8,10,13,15)$$

c) Implement the following Boolean function F, together with the don't-care conditions d, using no more than two NOR gates: [4]

$$F(A,B,C,D) = \sum(2,4,6,10,12)$$

$$d(A,B,C,D) = \sum(0,8,9,13)$$

Assume that both the normal and complement inputs are available.

3. a) Explain how a NAND/NOR latch store a bit. Mention their limitations. [3]

b) What is the limitation of S-R flip-flop? Explain how the limitation can be resolved. [4]

c) Define race-around condition in J-K flip-flop. How can you overcome the problem? Explain with an appropriate figure and waveforms. [5]

4. a) What is the limitation of a parallel adder? Using 74LS83 ICs, draw a 16 bit parallel Adder. [3]

b) Explain how 2's complement system can facilitate arithmetic operations in digital computing. [3]

c) Draw a parallel adder/subtractor using 2's-complement system and explain its operations. [6]

5. a) Draw a Mod-14 and a Decade ripple counter with their state transition diagram. [4]

b) Show how to wire the 74293 IC as a MOD-6 counter. [2]

c) Explain the operation of a Synchronous up/down MOD-8 counter with an appropriate diagram. [6]

6. a) Write short notes on the followings: [5]

I) Fan-Out

ii) Noise immunity

III) Propagation delay

IV) Characteristics of TTL logic gate.

b) Design and explain the working principle of a TTL NOR gate. [5]

c) A certain TTL IC output is rated at $I_{OH}(max) = 800\ \mu A$ and $I_{OL} = 48$ mA. Express the IC's fan-out in terms of unit loads. [consider 1UL = 40 μA in the HIGH state and 1.6 mA in the LOW state] [2]

7. a) Design a 1 of 8 decoder using logic gates. [4]

b) Use 74LS138 ICs to design a 1 of 32 decoder. [5]

c) Draw the internal diagram of a 8:1 encoder. [3]

8. a) What is Multiplexer? Design an 8-input MUX and explain its operation. [4]

b) How can you use a 74138 IC as a DEMUX? Explain with diagram. [4]

c) Draw the logic diagram for the 7442 BCD to decimal decoder. [4]