Question No. (20-21)	Question No. (19-20)	Chapter/Section Number	Topic Name
1. a)	5. b)	2.5	Performance Assessment
1. b)	1. a)	5.1	Semiconductor Main Memory (SRAM vs DRAM)
1. c) i)	1. c) i)	4.2 / 4.3	Cache Memory Principles / Elements of Cache Design (Hit time)
1. c) ii)	1. c) ii)	4.2 / 4.3	Cache Memory Principles / Elements of Cache Design (Miss penalty)
2. a)	2. a)	7.4	Interrupt-Driven I/O (Interrupt handling)
2. b)	-	2.1	A Brief History of Computers (ENIAC)
2. c)	2. c)	3.4 & App 3A	Bus Interconnection (Asynchronous timing diagram for system bus Read/Write cycle)
3. a)	3. a)	4.3	Elements of Cache Design (Write Back vs Write Through)
3. b)	3. b)	4.3	Elements of Cache Design (Direct Mapping cache design problem)
4. a)	4. a)	4.3	Elements of Cache Design (Direct, Associative, Set-Associative Mapping differences)
4. b)	4. b)	4.3	Elements of Cache Design (Cache miss calculation problem)
5. a)	5. a)	7.2, 7.3, 7.4, 7.5	I/O Modules / Programmed I/O / Interrupt-Driven I/O / Direct Memory Access (I/O Techniques)
5. b)	-	4.3	Elements of Cache Design (Complex cache design calculation problem)
5. c)	5. c)	1.1 / 1.2	Organization and Architecture / Structure and Function (Von Neumann Architecture)
5. d)	5. d)	3.4	Bus Interconnection (Multiplexed Bus)
6. a)	6. a)	7.2	I/O Modules (Necessity of I/O modules)
6. b)	6. b)	7.5	Direct Memory Access (DMA Cycle Stealing)
6. c)	6. c)	8.1	Operating System Overview (OS as resource manager in I/O controller)
7. a) i)	-	6.1	Magnetic Disk (Disk capacity calculation)
7. a) ii)	-	6.1	Magnetic Disk (Burst transfer rate calculation)
7. b)	-	1.2	Structure and Function (Data processing and data movement functions)
7. c)	-	12.3	The Instruction Cycle (Execution cycle of program execution)
7. d)	-	1.2	Structure and Function (Data processing and data movement functions)
8. a)	-	12.4	Instruction Pipelining (Definition and timing diagram)
8. b)	-	12.2	Register Organization (Processor with an accumulator register)
8. c)	-	1.2	Structure and Function (Data processing and data movement functions)
-	1. b)	2.1 / 2.2	A Brief History of Computers / Designing for Performance (Moore's Law)
-	2. b)	3.1	Computer Components (Memory address space calculation)
-	7. a)	12.1 / 12.3	Processor Organization / The Instruction Cycle (CPU components and working)
-	7. b)	13.8	The RISC versus CISC Controversy (Distinguishing RISC and CISC)
-	7. c)	12.2 / App 10A	Register Organization / Stacks (Stack organization, Register and Memory Stack)
-	8. a)	11.5	Assembly Language (Assembler workings)
-	8. b)	10.1 / 10.4	Machine Instruction Characteristics / Types of Operations (0, 2, 3-address instructions)
-	8. c) i)	10.1	Machine Instruction Characteristics (Op-code)
-	8. c) ii)	10.1	Machine Instruction Characteristics (Machine Language)