20-21

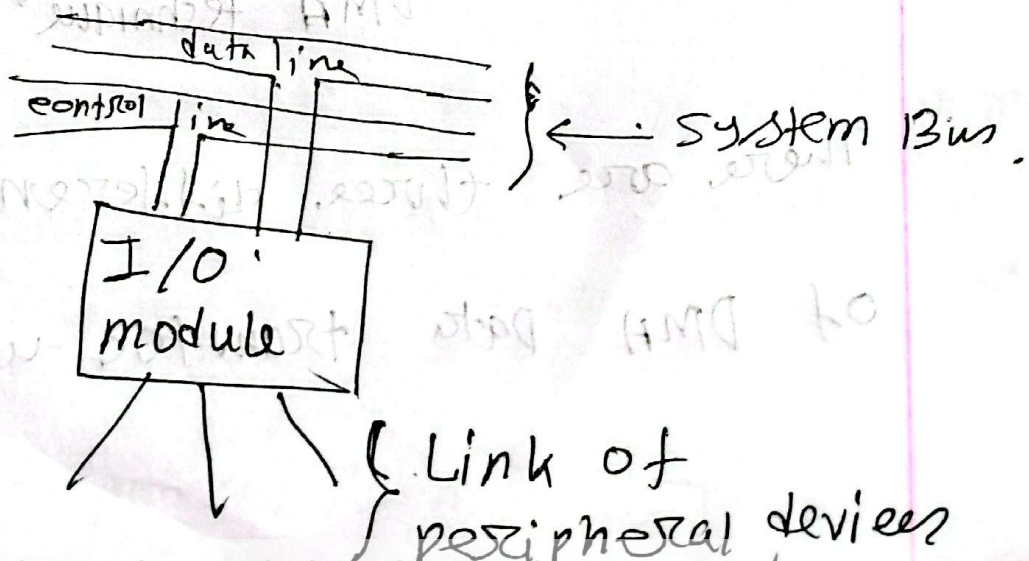
Question 6

ⓐ Describe the necessity of I/O modules?

Sol^n Input/Output (I/O) modules are needed to connect input and output devices like (keyboard, mouse, printer) to the computer.

They help the CPU communication with these devices by sending and receiving data properly.

Without I/O modules, the CPU can't directly handle different I/O devices.

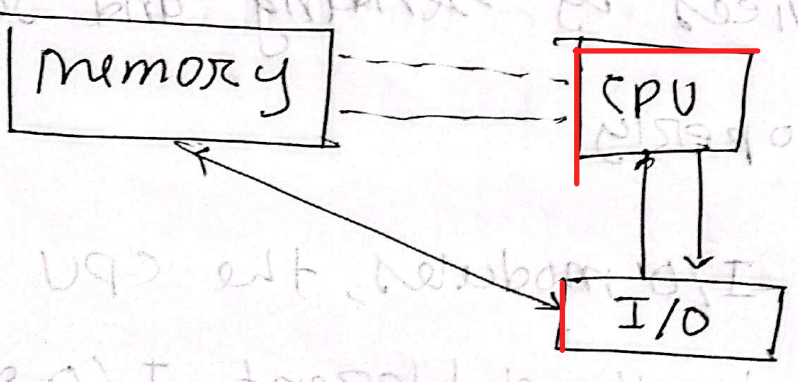


(B)

In Direct memory Access (DMA) operation describe about cycle stealing.

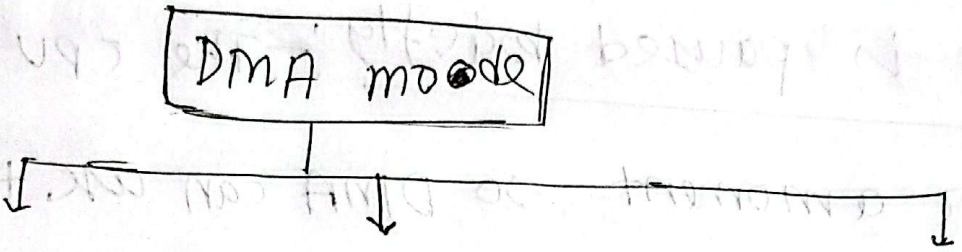
Soln

DMA is a method that allows Hardware devices to ~~allows~~ directly transfer data to or from memory without using the CPU for each data transfer.



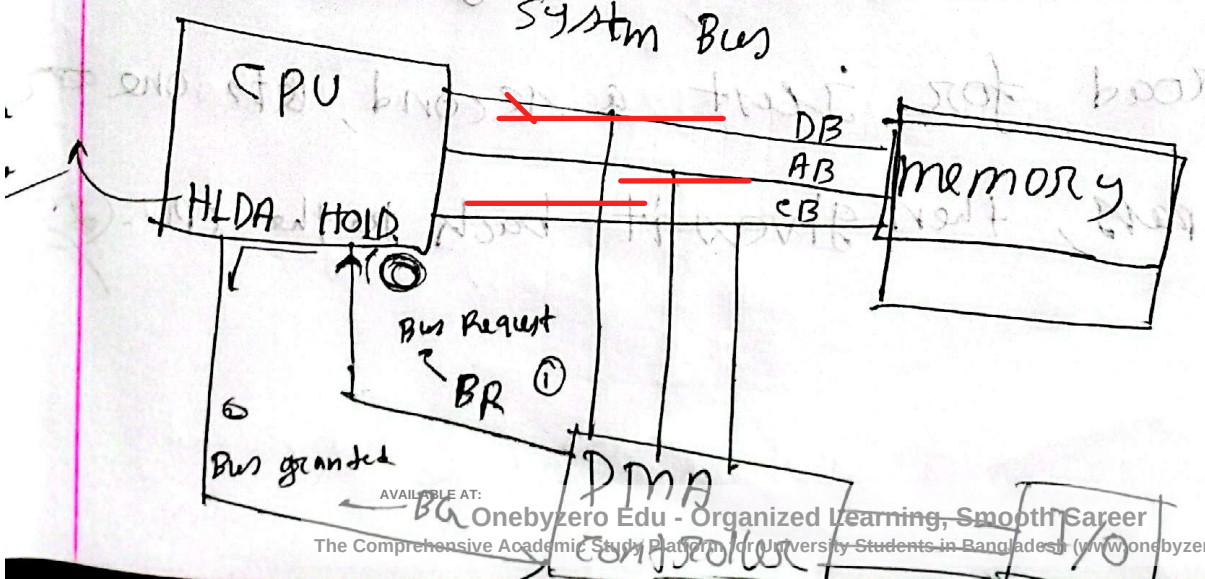
"DMA technique"

There are three differents modes of DMA Data transfer which are -



Burst mode | cycle stealing mode | Interleaving mode

cycle stealing mode: cycle stealing is a process used in DMA operations where DMA controller takes control of the system bus for a short time to transfer data while the CPU is temporarily paused.



CPU is paused briefly :- The CPU stops for a moment so DMA can use the bus to transfer data.

Transfer for small amount :- only one unit is transferred in each cycle

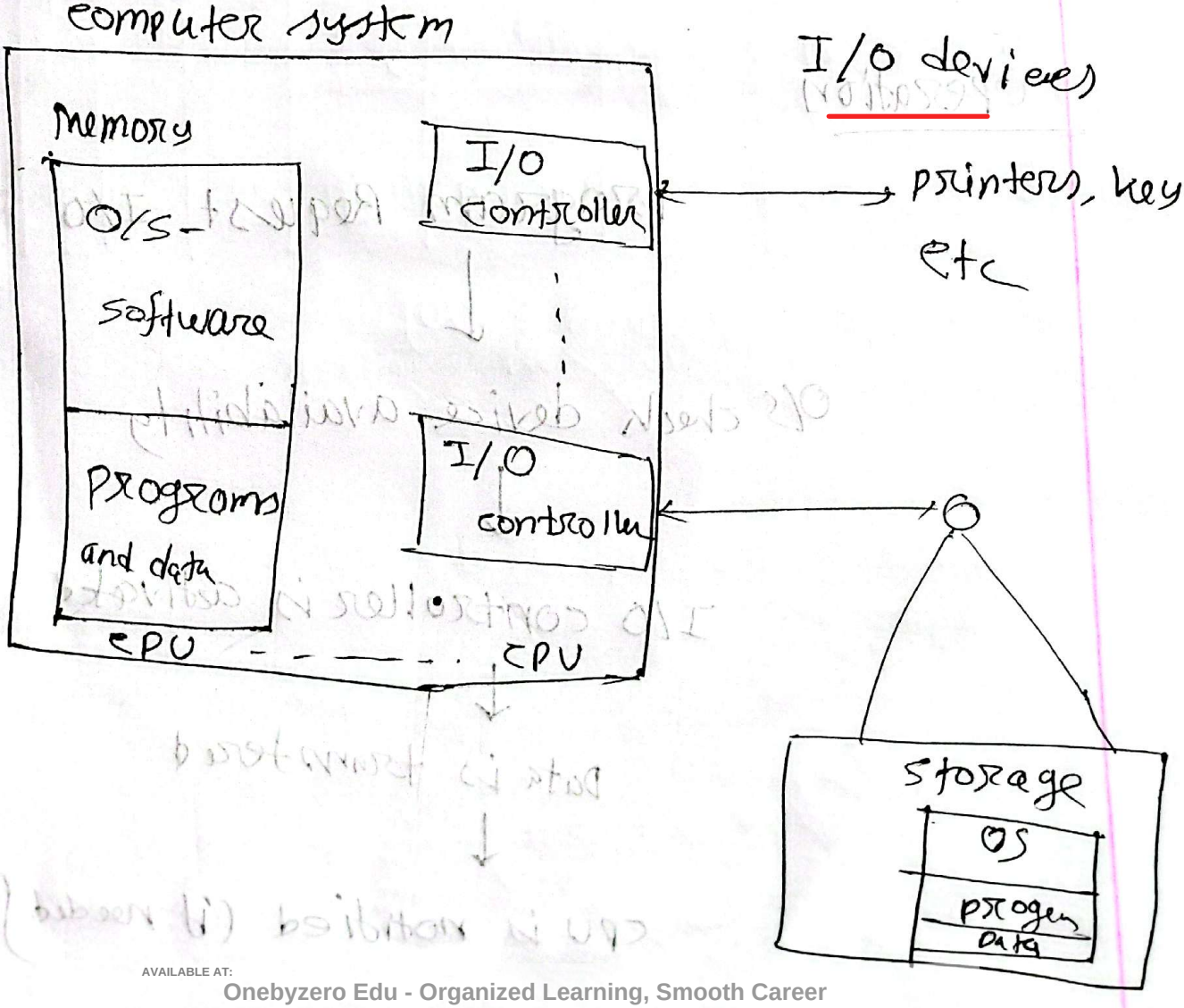
→ The CPU continues its work quickly after each transfer.

Imagine CPU and DMA are sharing a road. In cycle stealing, DMA borrows the road for just a second, lets one car pass, then gives it back to the CPU. (2)

6(c) Describe OS as a resource manager in I/O controller.

Ans

The operating system works as a resource manager to manages I/O devices through the I/O controller



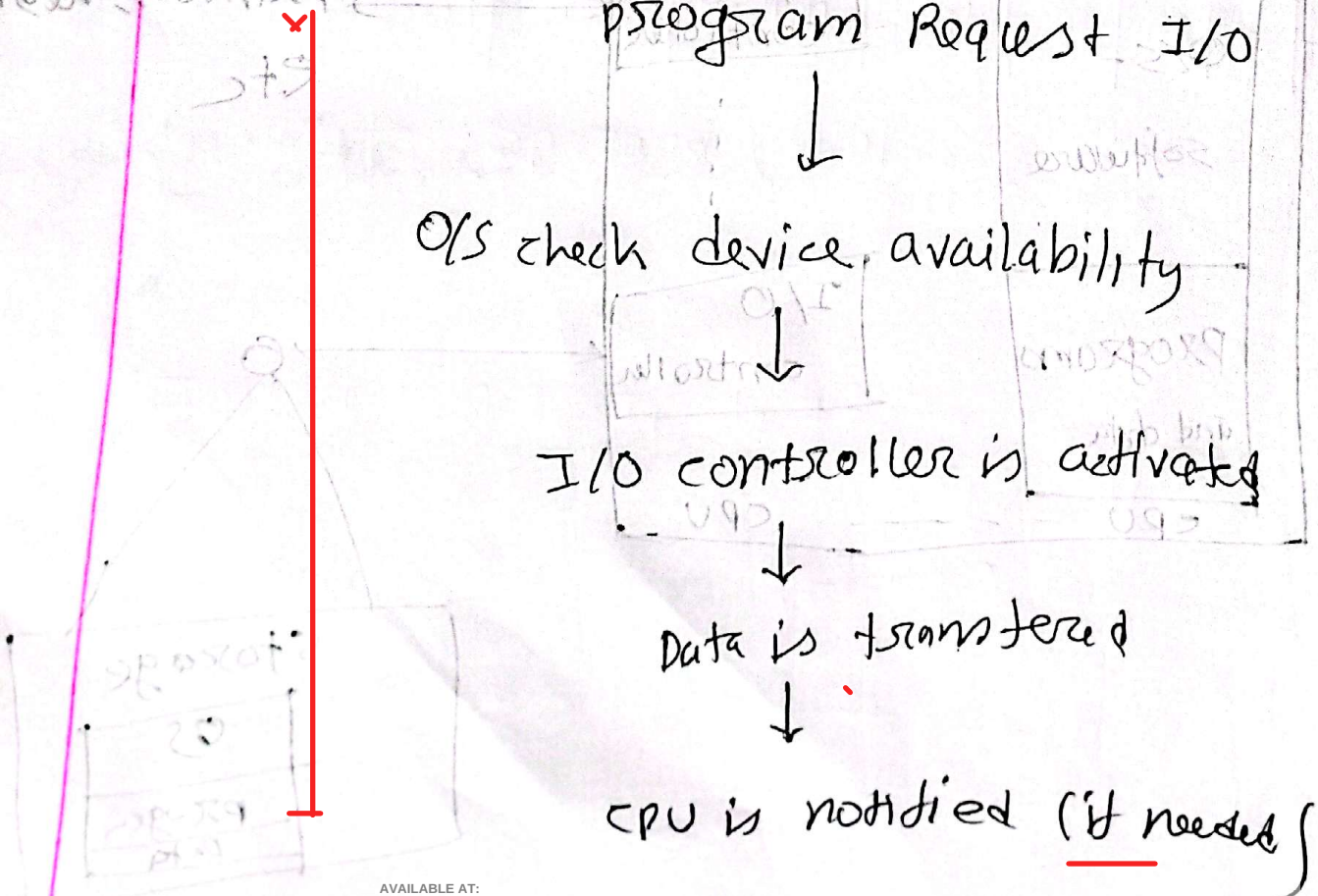
Functions of O/S as a Resource manager

→ The O/S allocates I/O devices to different process as needed

→ It schedules I/O requests and maintain

→ It manages data transfer between memory and devices using I/O controller.

Operation



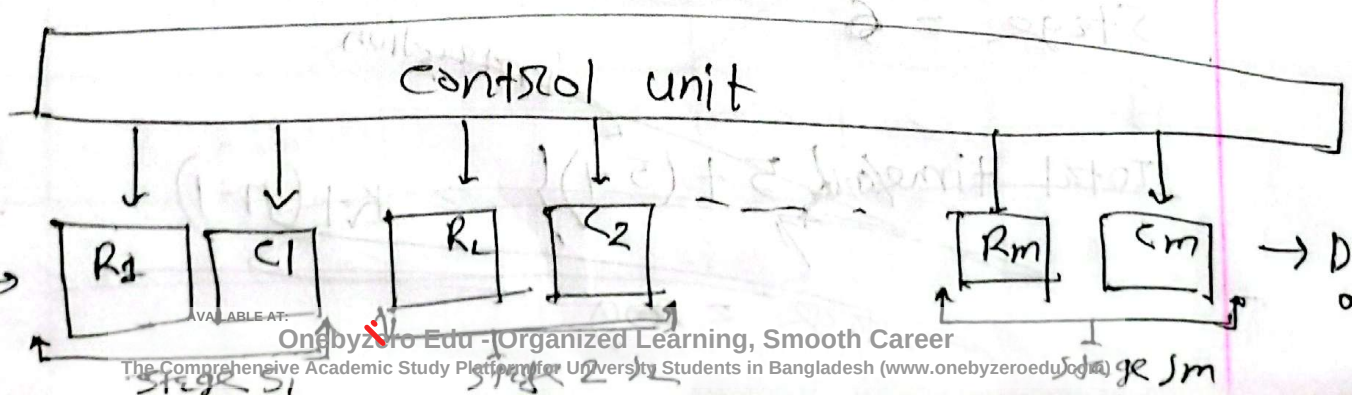
8(a) Define Pipelining. Show the timing diagram of Pipelining.

Ans

Pipelining :- Pipelining is a technique used in CPUs to increase instruction execution speed by dividing the instruction into multiple stages.

Each stage works at the same time on different instructions.

while one instructions is being executed the next one can be decoded, and another can be fatched all the same time.



Timing diagram for 5 instructions

5 stage pipeline

1. FI
2. Decode Instruction (DI)
3. Calculate operands (CO)
4. Fetch operands (FO)
5. Execute Instruction (EI)
6. write operand (WO)

Instruction = 5 (I_1, I_2, I_3, I_4, I_5)

Stage = 5

Total time = $5 + (5-1) = K + (n-1)$

Stage = 9

Total cycle = $K + (n-1) = 6 + (5-1) = 10$

Time / In.	1	2	3	4	5	6	7	8	9	10
I_1	FI	DI	CO	FO	EI	WO				
I_2		FI	DI	CO	FO	EI	WO			
I_3			FI	DI	CO	FO	EI	WO		
I_4				FI	DI	CO	FO	EI	WO	
I_5					FI	DI	CO	FO	EI	WO

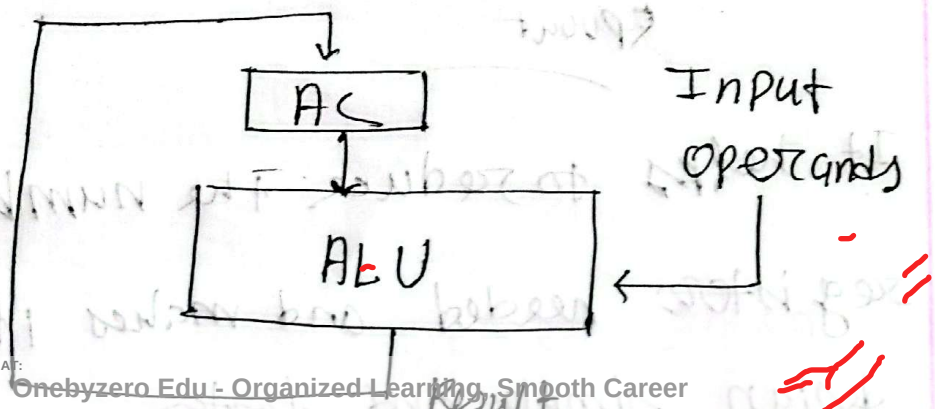
Timing diagram for pipeline

8(b) Explain processor with an accumalator register

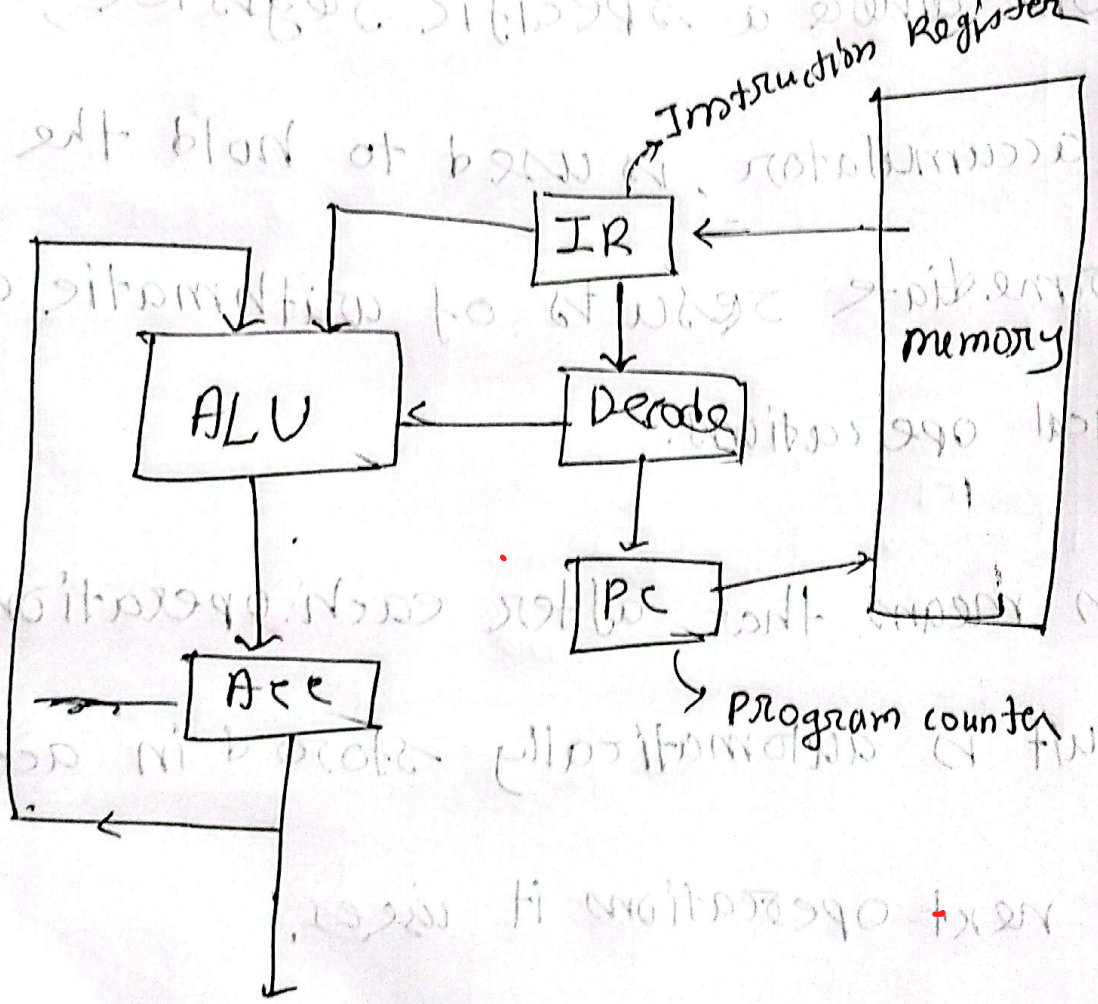
Soln:

A processor with an accumulator register is one where a specific register, called the accumulator, is used to hold the intermediate results of arithmatic and logical operations.

This means that after each operation the result is automatically stored in accumulator and next operations it uses.



All operations like addition, subtraction AND, OR, etc are done using the Accumulator and another value from memory



It helps to reduce the number of registers needed and makes it CPU design simple and faster

8 c → same as 7(b)