2) (b) [20-21, ~~19-20~~, 18-19, ~~17-18~~] [4] (Mid 1 21-22)

Q. টা অনেক বড় তাই উঠাই নি।

(Mid 21-22) Q.1

This representation is wasteful because to represent a decimal digit from 0 to 9, we need to have ten tubes. But at a time, only 1 tube can ON and others will be OFF.

Each tube can be ON or OFF, so 10 tubes can make 2^n patterns or $2^{10} = 1024$ patterns. But ENIAC can use only 10 combination of digits (0 to 9) at a time. So other combinations are not used. For this reason, this representation is wasteful.

The patterns range of integer values ~~could~~ we could represent using 10 vacuum tubes ~~as~~ is $2^n - 1 = 2^{10} - 1 = 1023$. So the range is 0 to 1023.

(Ans)

Subject.....

Date:.....Time:.....

Q:2 Consider a two-level cache with access time 5 sec and 80 sec. If hit ratio is 95% and 75% in the two caches. Main memory access time 250 sec. What is the effective access time?

Ans:

Given,

$T_1 = 5$ sec $\quad T_M = 250$ sec

$T_2 = 80$ sec $\quad h_1 = 0.95$ $\quad h_2 = 0.75$

$\therefore EAT = h_1 T_1 + (1-h_1) h_2 (T_1 + T_2) + (1-h_1)(1-h_2)(T_1 + T_2 + T_M)$

$= 0.95 \times 5 + (1-0.95) \times 0.75 \times (5+80) + (1-0.95)(1-0.75)$
$(5+80+258)$

$= 12.125$ sec.

Ans

Bari Stationary

Q.3 Suppose three interrupt handlers A, B, and C (having priority level A > B > C) with Interrupt Service Routine (ISR) 10, 30 and 20 respectively. Graphically show the transfer of control for interrupt sequence of C, A and B at time t = 10, 25 and 45 respectively. [10]

Solution:

Given Data,

interrupts = A, B, and C

priority = A > B > C

ISR execution time;

A → 10 units, B → 30 units, C → 20 units.

Interrupt sequence (Time);

C occurs at t = 10

A occurs at t = 25

B occurs at t = 45

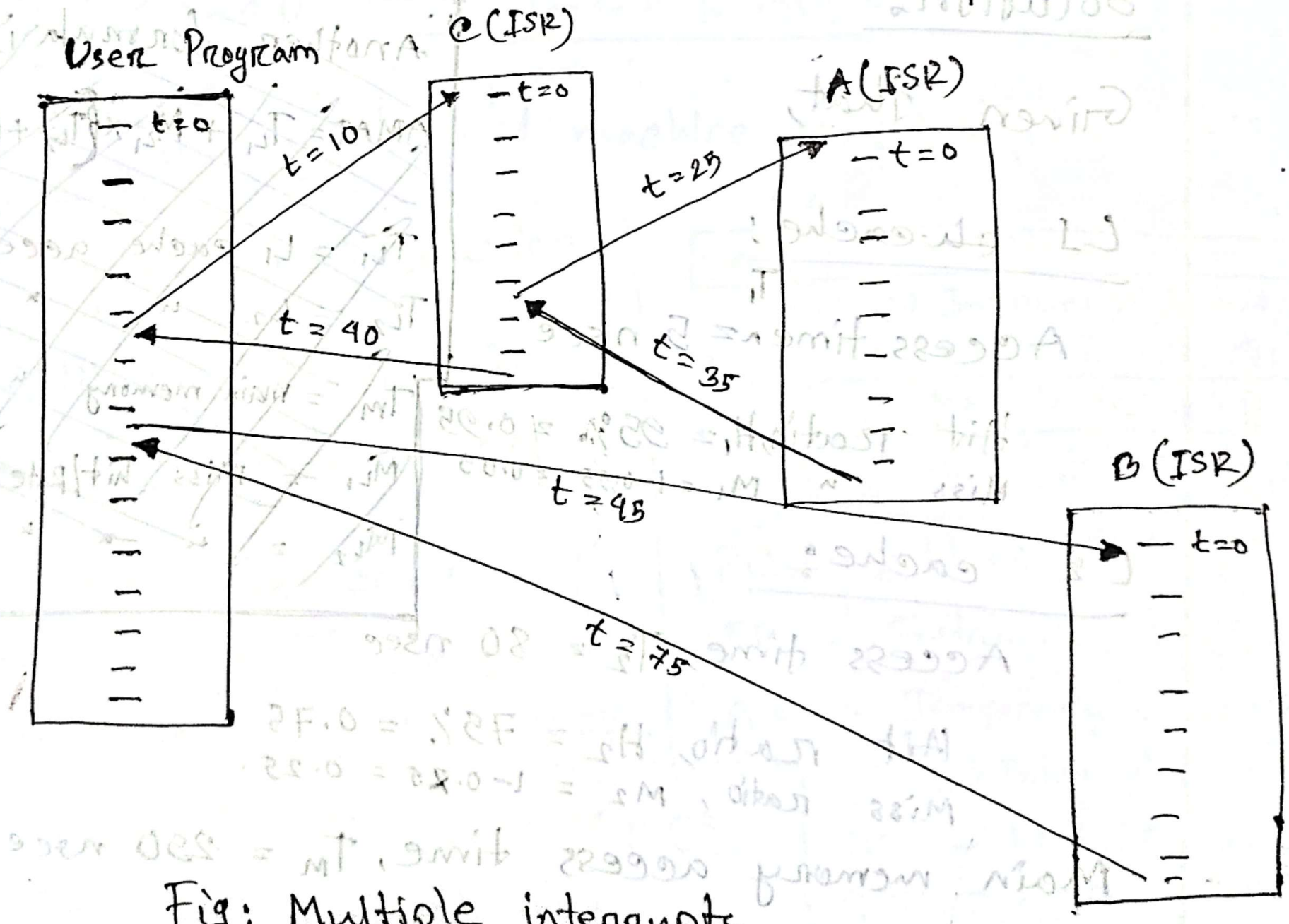

Fig: Multiple interrupts.

Explaination:

When $t_1 = 10$ C starts execution. C needs 20 times units (scheduled $t_1 = 10$ to $t = 30$).

But at $t = 25$ A interrupt because A has higher priority than C, so C is preempted and A starts execution for 10 times units (till $t = 25$ to $t = 35$)

At $t = 35$, A ends execution and again C starts and execute the remaining part untill $t = 40$.

Then $t = 40$ to $t = 45$ processor remain Idle and at ~~45~~ $t = 45$ B start execution. B execute ~~was~~ 30 times unit. ~~is~~ till $t = 75$.

Q. 4 maximum memory capacity of system. For example 8080 has 16 bit address bus. Then how much memory space it will provide? [5]

Solution:

Formula for maximum addressable memory,

$$\text{memory capacity} = 2^{\text{Address Bus width}} \times \text{word size}$$

since each address typically refers to one byte (word size = 1 byte). So the total memory capacity is $2^{16} = 65536$ byte $= 64$ KB.

Subject.....

Date:.....Time:.....

Q.5 A bottleneck refers to a limitation on constraints that ~~slows~~ slow down the overall performance of a system. It is the weakest point that restricts efficiency of a system and prevents the system to achive its full potential.

There are several bottlenecks ~~that impacts of system~~ we faces to design a cache which impacts on system performance. such as,

1. Cache Size vs Access Time: Larger caches store more data but increase access time.

2. Cache Hit vs Miss Rate: A high miss rate forces the processor to access slower main memory, increasing Latency.

3. Memory Bandwidth: Cache misses increase memory traffic, causing delays in data retrieval.

Subject.....

Date:.....Time:.....

4: Cache Coherency: In multi-core system, maintaining ~~cons~~ consistency between caches leads to additional overhead.

5. Power Consumption: Larger and faster caches consume more power.

6. Associativity Trade-offs: It reduces conflicts but increase lookup time and hardware complexity.