

1. What is counter? Difference between synchronous and asynchronous or ripple counter.

Answer:

Counter: counter is the sequential circuits that count the number of pulses that can be either in binary code or BCD form.

Difference between synchronous and ripple counter is given below:-

Synchronous counter	Ripple Counter
1. In synchronous counter, all flip-flops are triggered with same clock simultaneously.	1. In ripple counter, all flip-flops are triggered with different clock, not simultaneously.
2. It is faster than ripple counter.	2. It is slower than synchronous counter.
3. Does not produce any decoding errors.	3. It produces decoding error.

4. It is also called parallel counter.

5. It's ~~desing~~ designing and implementation are complex.

6. Example:

Ring counter,

Johnson counter.

7. Propagation delay is less.

4. It is also called serial counter.

5. It's designing and implementation are simple.

6. Example:

Ripple up counter

Ripple down counter.

7. There is high propagation delay.

2. What is Mod number? what is the method of designing a counter with "Mod Number" $< 2^N$.

Answers

The modulus of a counter is the number of states in its count sequence. The maximum possible modulus is determined by the number of flip-flop.

Mod numbers that are equal to 2^n , where, n is the number of ffs.

Sy:

Adv: -

- (i) Faster operation
- (ii) Less propagation
- (iii) Easier to design
- (iv) Reliable for high-speed applications

Dis:

- (i) complex circuitry
- (ii) power consumption

Adv:-

- Adv: (i) Simple design
- (ii) Low power consumption
 - (iii) Fewer components

Dis:

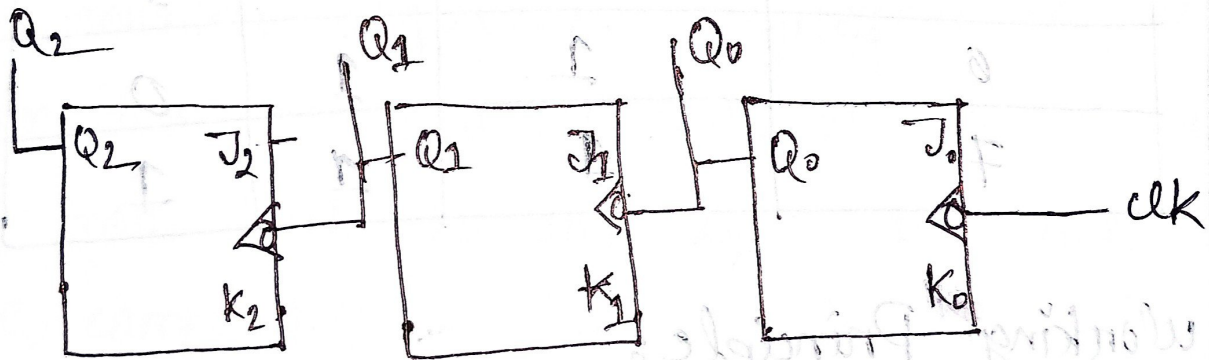
- (i) Slower operation
- (ii) propagation delay accumulation
- (iii) complexity in large counting

3. Explain the working principle of 3-bit ripple counter with timing diagram.

Answer:

Ripple counter: Ripple counter is a cascaded arrangement of flip-flop where the output of one flip-flop derives the clock input of the following flip-flop.

A 3-bit ripple counter using a JK FF is: —



→ All the J & K inputs are assumed to be 1.

Here;

Number of flip-flop, $n = 3$

Number of states, $N = 2^3 = 8$

Range of counting 0 to $(N-1) = 0$ to $(8-1)$
 $= 0$ to 7

Traffic table:

count state	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

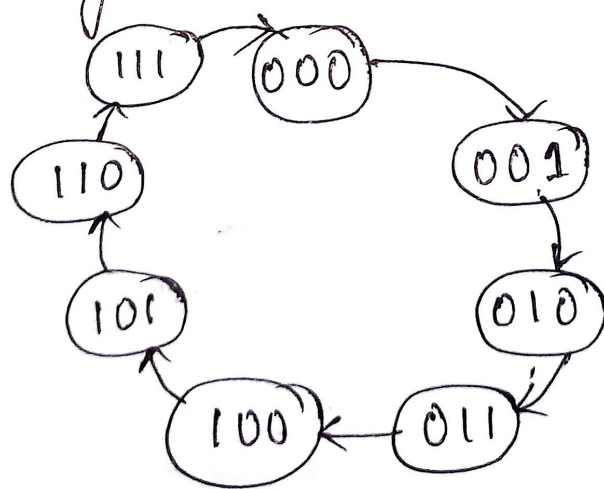
Working Principle:

The 3 bit ripple counter is used in the circuit has eight different state each one of which represent a count value. $8 = 2^3 = n$.

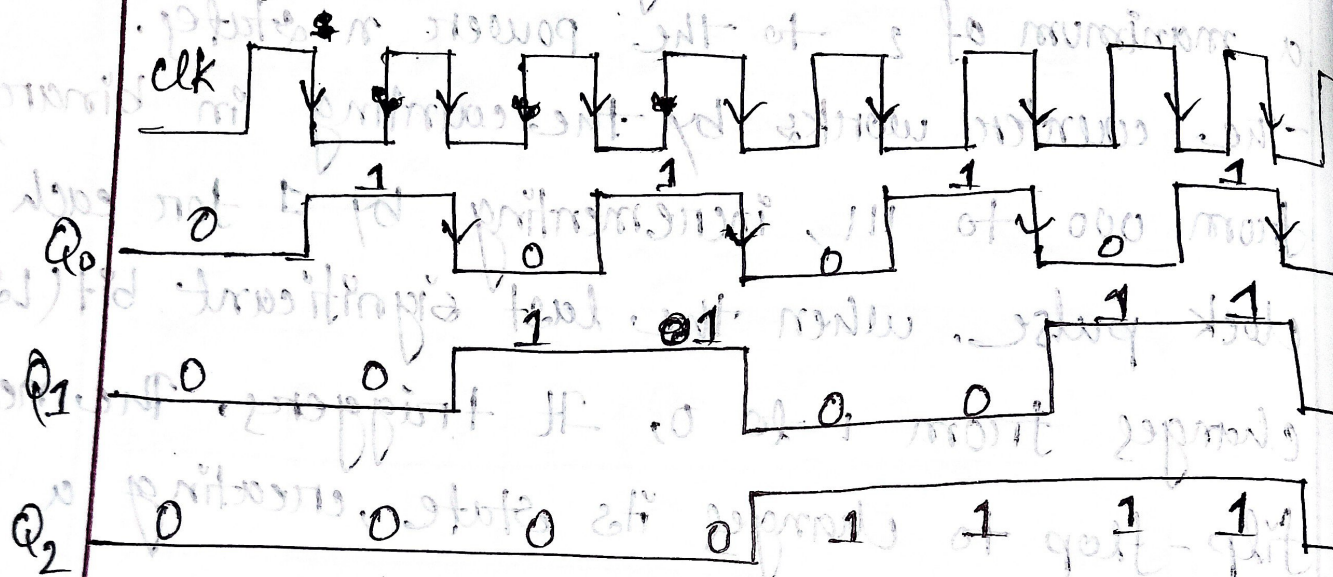
Similarly a counter having n flip-flop can have a maximum of 2 to the power n states.

The counter works by the counting in binary from 000 to 111 , incrementing by 1 for each clock pulse. When the last significant bit (LSB) changes from 1 to 0 , it triggers the next flip-flop to change its state, creating a ripple effect through the counter.

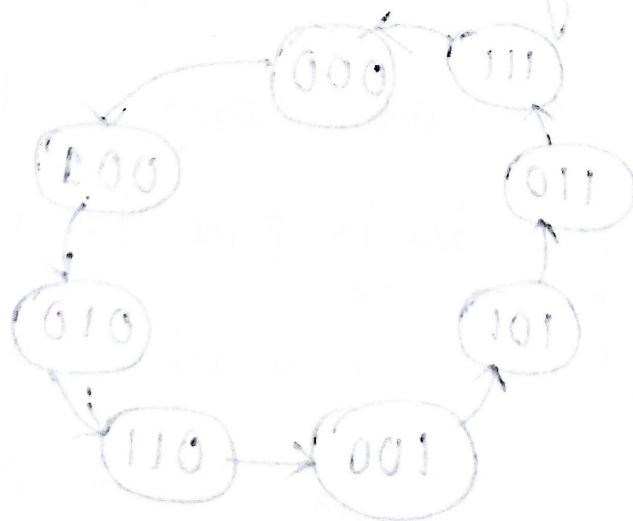
The counter sequence progresses in a binary state $000, 001, 010, 011, 100, 101, 110, 111$ and then rolls back to 000 with the next clock pulse, completing a full cycle.



Timing Diagram:



The counter sequence progresses in the following order: 000, 001, 010, 011, 100, 101, 110, 111, and then rolls back to 000 with the next clock cycle.



4. Draw a Mod-14 and a Decade ripple counter with their state transition diagram.

Answers

Mod-14 ripple counter using JK-flip-flop:-

Here,

number of clock pulse count by the counter, $N = 14$

Range for counting 0 to $(N-1) = 0$ to 13

Number of FF, $n = 4$

Number of state, $= 2^n = 2^4 = 16$

State tables

clk	Q_A Q _B	Q_A Q _C	Q_B Q_C	Q_A Q _D	Q _R
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	0	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1 1	X
					X

State Transferring diagram

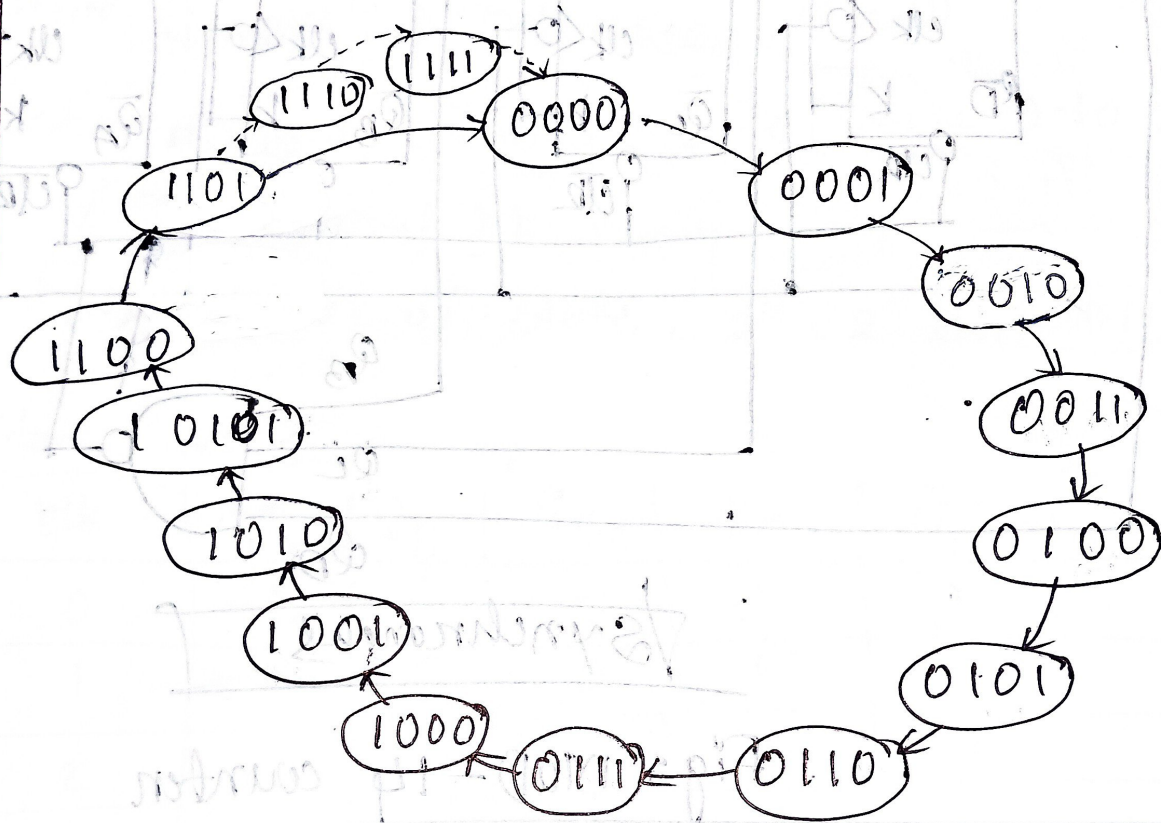


Fig: state diagram of MOD-14 counter

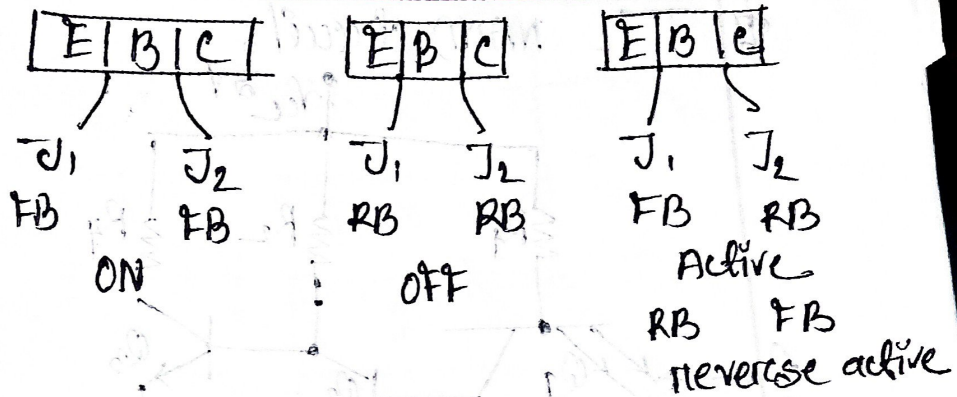
$$\overline{clk} = \overline{QAQBQC}$$

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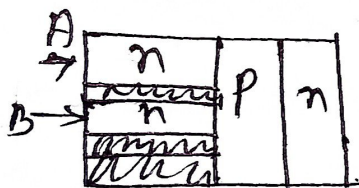
Chapter: 08

TTL Basics

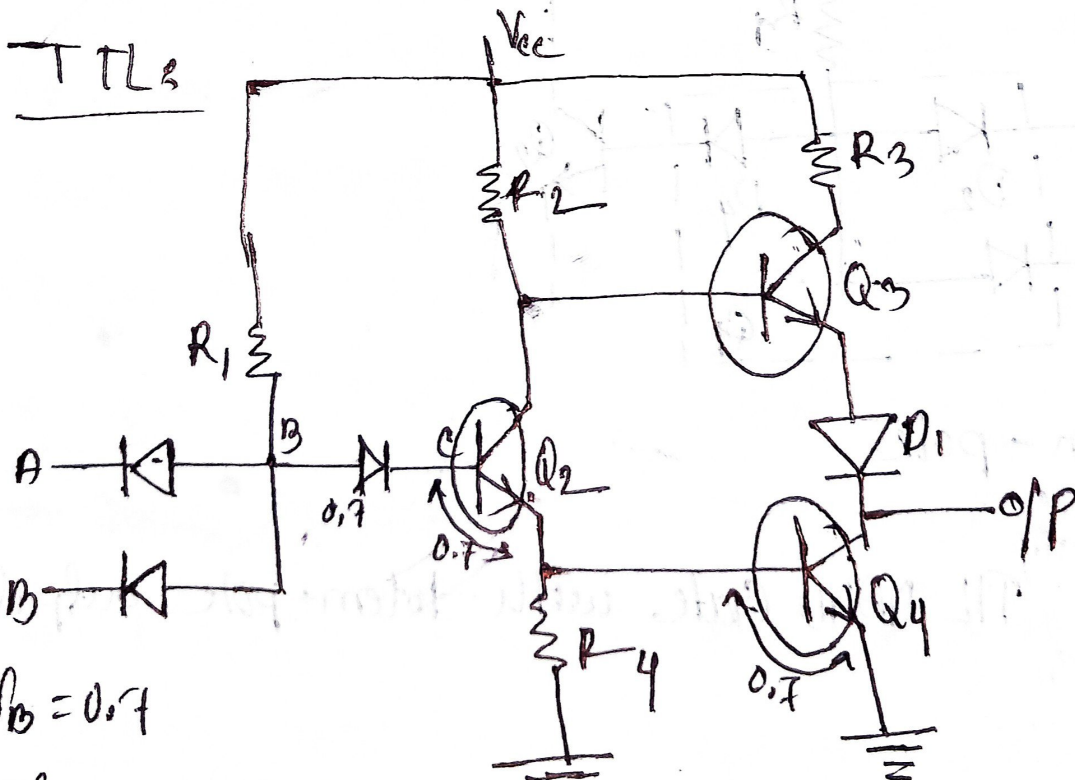
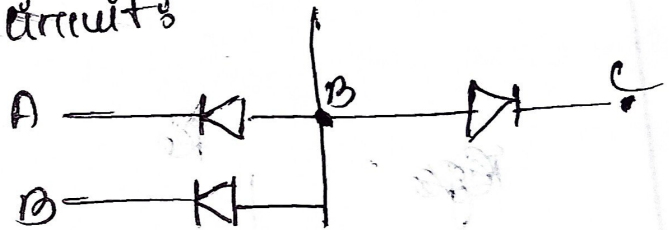


TTL works 4 mode of configurations.

Multi-Emitter Transistors -



Circuits

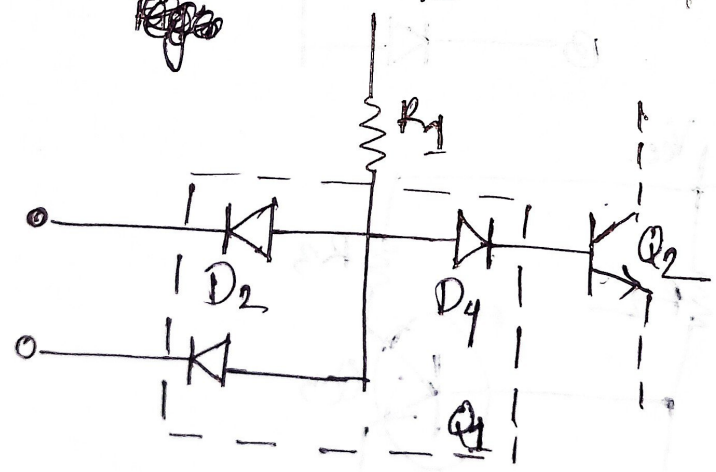
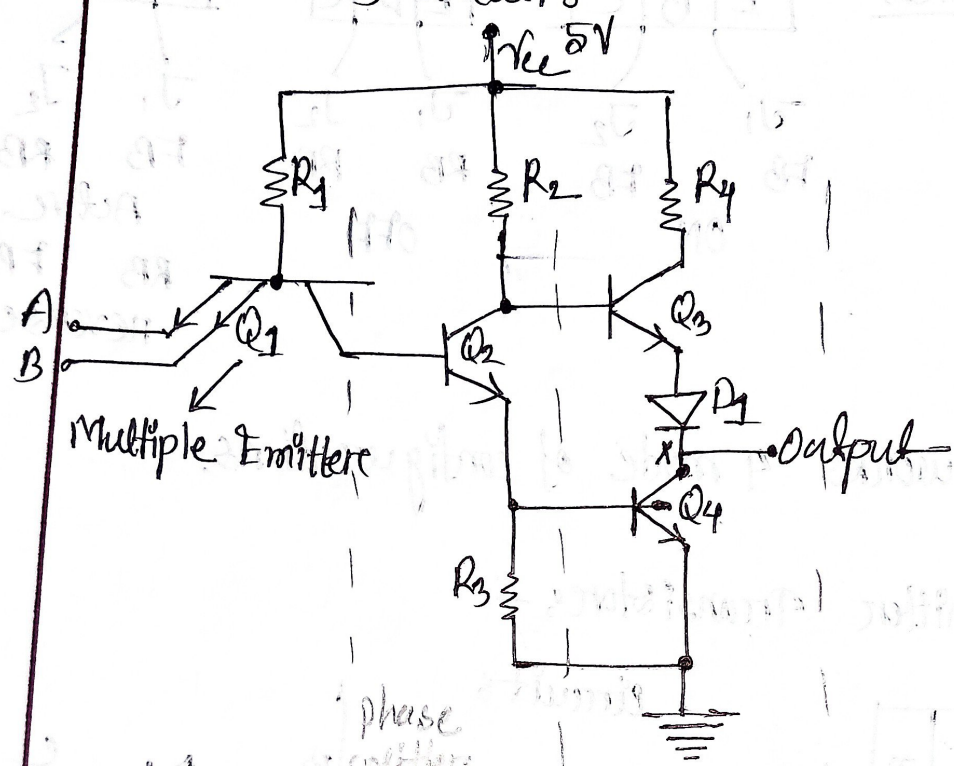


A, B, OFF
2 (V)
 $V_B = 0.7$
 $+ 1.4$
 $= 2.1V$
Current flow 200

$V_B = 0.7$

$V_C = 0.7 + 0.7 = 1.4$
(current flow 210 μA)

TTL NAND circuit:



totem - pole

Fig: TTL NAND Gate with totem-pole output.

Truth table:

A	B	Q ₁	Q ₂	Q ₃	Q ₄	Output
0	0	ON	OFF	ON	OFF	1
0	1	ON	OFF	ON	OFF	1
1	0	ON	OFF	ON	OFF	1
1	1	OFF	ON	OFF	ON	0

Explanation:

1. Multiple Emitter transistor (Q₁):

→ The input section of the TTL NAND gate includes a multiple-emitter transistor, Q₁, which has two emitters connected to inputs A and B.

→ when both A & B are high, Q₁ is active, allowing current to flow, which affects the rest of the circuit.

2. Base Resistors (R₁, R₂, R₃ & R₄):

→ These resistors control the base current for each transistor, managing the biasing and ensuring proper operation of each transistor stage.

3. Transistor Q_2 :

→ Q_2 is connected as a phase splitter, meaning it generates complementary signals needed for the next stage.

→ It responds to the state of Q_1 and helps in determining the output state of the circuit.

4. Diode (D_1):

→ D_1 is used to control the ~~the~~ totem-pole configuration by blocking certain current paths based on the state of the inputs.

5. Totem pole output (Q_3 & Q_4):

→ The totem-pole configuration involves transistors Q_3 & Q_4 stacked vertically.

→ When the circuit output is high, Q_3 is active, allowing the output to be pulled to the supply voltage.

→ When the output is low, Q_4 is active, pulling the output to ground.

→ This totem-pole configuration provides a strong output drive capability and fast switching.

Functionality:—

- Output is low, when inputs are high.
- If either A or B is low, Q_1 does not conduct preventing Q_2 from turning on Q_4 , which makes the output high.

Characteristics of TTL logic gates:

- Fast operation: TTL circuits are known for their high speed operation.
- Low power consumption: It has relatively low power consumption.
- Wide operating voltage range.
- Compatibility
- High noise immunity
- Standardized packages
- Popular for digital design.

TTL NOR gate:

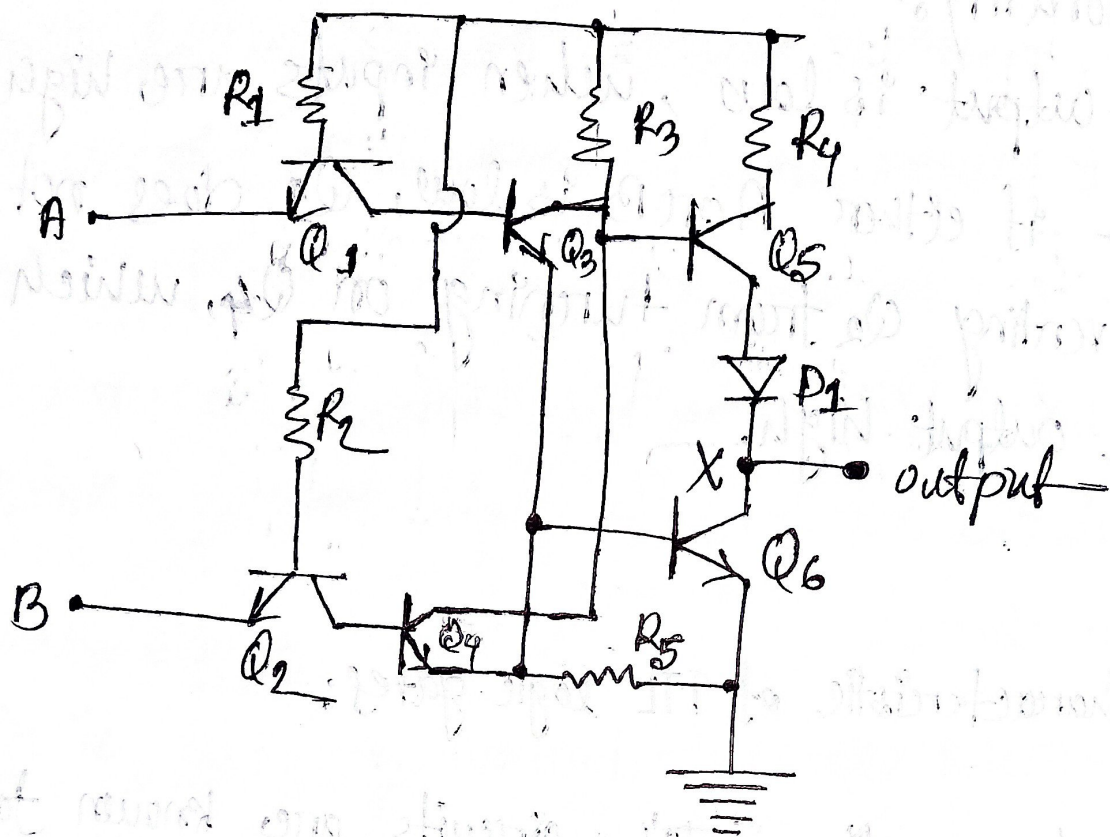


Fig: TTL NOR gate

truth table:

A	B	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	output
0	0	ON	ON	OFF	OFF	ON	ON	1
0	1	ON	OFF	OFF	ON	OFF	OFF	0
1	0	OFF	ON	ON	OFF	OFF	OFF	0
1	1	OFF	OFF	ON	OFF	OFF	OFF	0

cmos $\rightarrow$ Complementary Metal Oxide Semiconductor

Characteristics of ~~cmos~~ CMOS: —

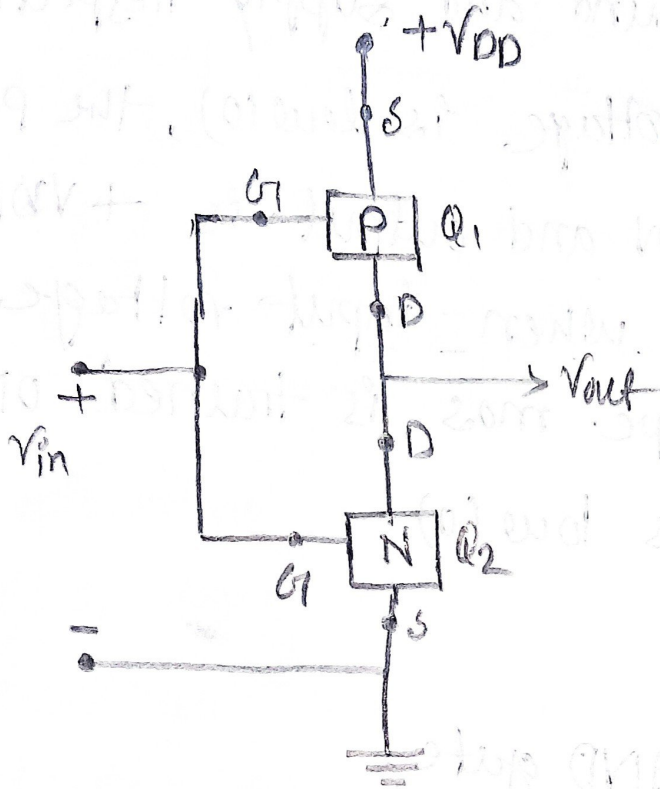
PMOS $\rightarrow$

I	O
(0) Low	(1) High
(1) High	(0) Low

Basic CMOS inverter:

NMOS $\rightarrow$

I	O
(0) Low	(0) Low
(1) High	(1) High



V_{in}	Q_1	Q_2	V_{out}
$+V_{DD}$ 1	OFF	ON	0
0V 0	ON	OFF	1

This figure shows the circuitry for the basic CMOS inverter.

CMOS inverter gate is one type of logic gate used to implement logical negation ($\neg$).

The basic structure of a CMOS inverter consists of an n-mos & p-mos transistor as a load and the gates of the two transistors are shorted at the input; the drains of the two transistors are also shorted where the output is obtained.

The sources n-mos and p-mos transistors are connected to the ground and supply respectively. When the input voltage is low (0), the p-type mos is turned ON and output is $+V_{DD}$ (1). On the other hand, when input voltage is high (1), the n-type mos is turned ON and the output is low (0).

CMOS NAND gate

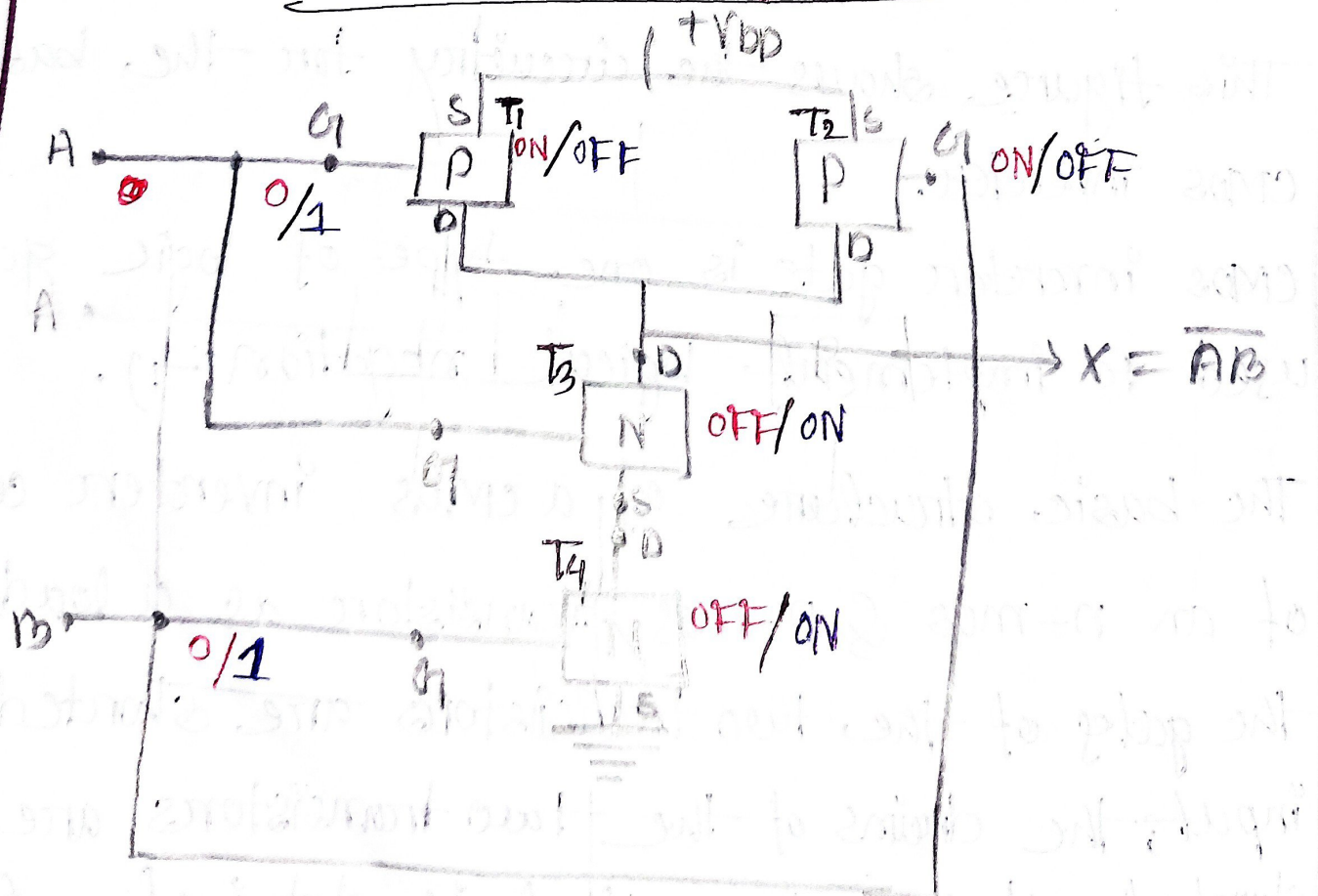


Fig: CMOS NAND gates.

Truth table; —

A	B	T ₁	T ₂	T ₃	T ₄	X
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

Explanation:

1. A CMOS two input NAND gate. P-channel transistors T₁ and T₂ are connected in parallel between +V and the output terminal.
2. N-channel transistors T₃ and T₄ are connected in series between the output terminal and ground.
3. When T₃ & T₄ Transistors on and T₁ & T₂ transistor off, the output is a logic 0. This condition happens when both inputs A & B are logic 1.
4. When logic 0 in input A & B, T₃ and T₄ transistors are off and T₁ and T₂ transistors

CMOS NOR gate:

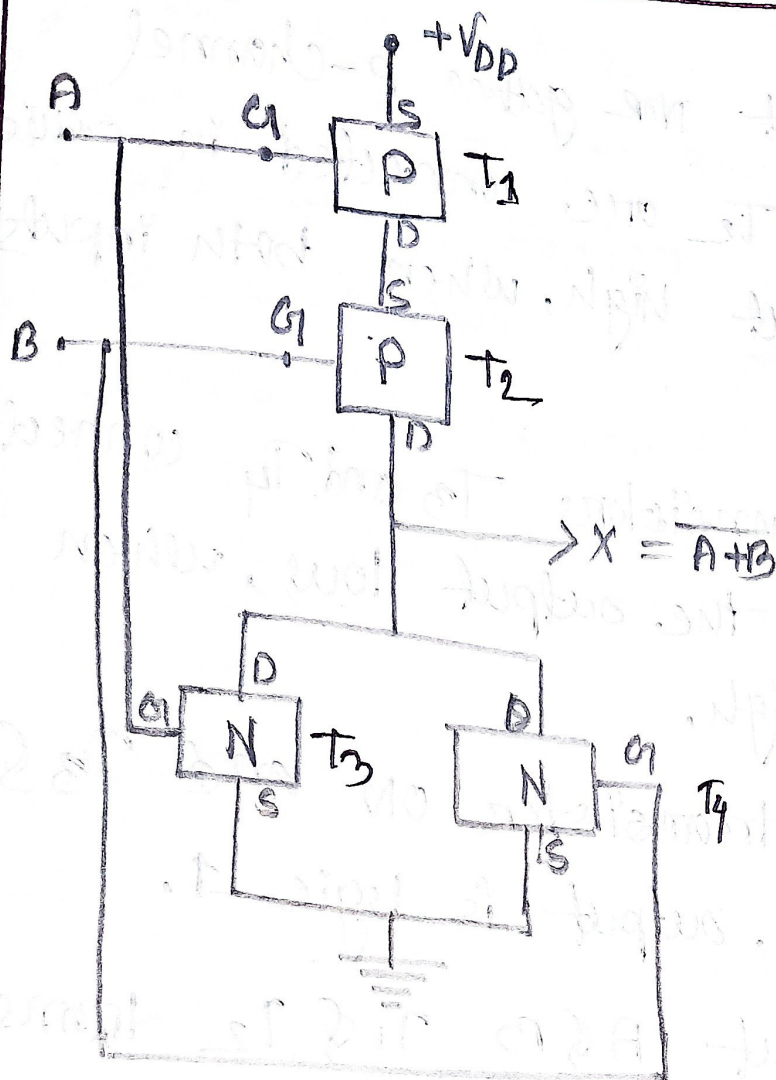


Fig: CMOS NOR gate

A	B	T_1	T_2	T_3	T_4	X
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

are ON, producing a logic 1.

~~So when one of is a logic '0' or~~

5. When one of the inputs is a logic 1 and other one is logic '0' or '1'. The output in both cases is logic 1.

CMOS NOR gate:

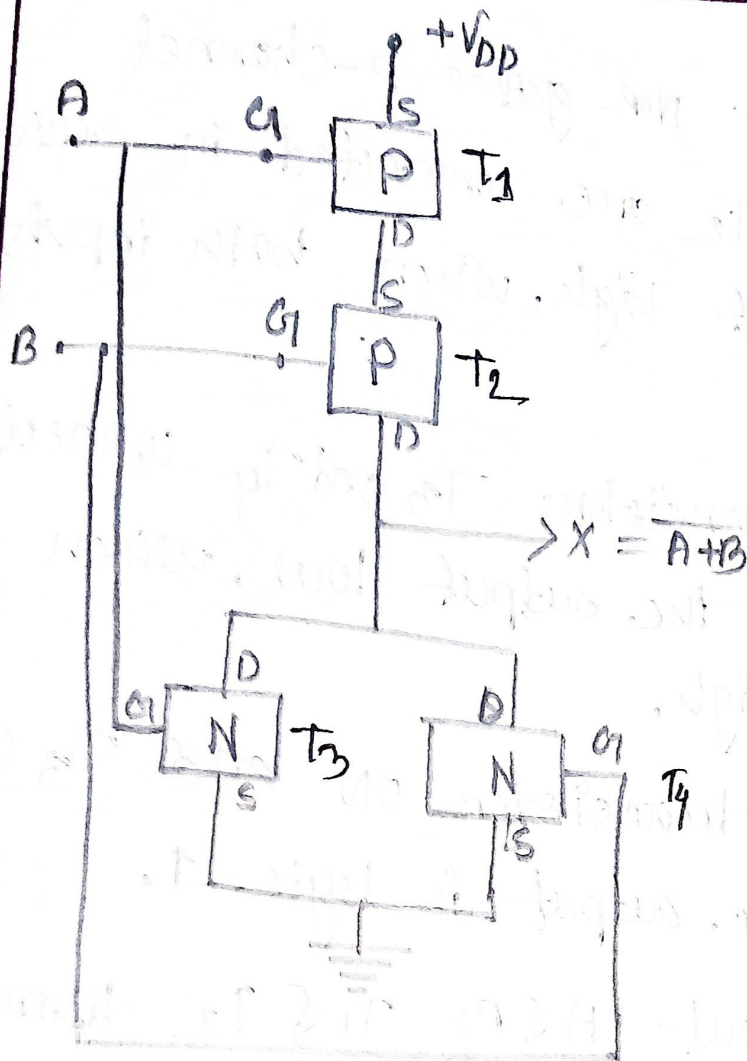


Fig: CMOS NOR gate

A	B	T_1	T_2	T_3	T_4	X
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

Explanation:

A CMOS two input NOR gate. P-channel transistors T_1 and T_2 are connected in series to pull the output high, when both inputs are low.

The N-channel transistors T_3 and T_4 connected in parallel to pull the output low, when either input is high.

- when ~~the~~ T_1 & T_2 transistors ON and T_3 & T_4 transistors off the output is logic 1.
- when logic 1 in put A & B T_1 & T_2 transistors off and T_3 & T_4 are ON, producing ~~logic~~ is a logic 0.
- when one of the input is logic 1 or 0 and other one is 0 or 1, in both cases ~~logics~~ the output is logic 0.

NIL NAND :-

1. when both A & B are low, both the diodes are forward biased. so the current due to the supply voltage $V_{cc} = 5V$ will go to the ground through R_1 and two diodes DA & DB. because of voltage drop Q_2 remain off. ~~base-emitter~~ and transistor Q_4 also remain off, but the transistor Q_3 is pulled ON (HIGH). Since Q_3 is an emitter follower, the output at the terminal will also be High (1).

2] when any input either A or B is low, the diode with low input will be forward biased. The same operation will take place as explain 1st case. In case, the output remain HIGH.

3] when both the inputs A & B are high, both diode at the emitter-base junction will be reverse biased. The collector-base junction is forward biased. It will turn ON Q_2 , with Q_2 turned ON Q_4 will also be turn ON. In case, the output will low, which is logic 0.

TTL NOR

1. Fan-Out :- The Fan-out is defined as the maximum number of logic inputs that an ~~an~~ output can drive reliably. Fan-out also called Loading Factor. It is calculated by dividing the output current of the driving IC by the input current of the driven ICs.

Logic gate	Fan-out
Transisto-to Transisto Logic (TTL)	up to 10 other digital gates
CMOS	over 50 connected devices

(ii) Noise immunity :- Noise immunity is a measure of a digital circuits ability to tolerate external noise without affecting its performance. In the digital electronics logic noise refers to unwanted, ~~electrical~~ ~~noise~~ and, ~~spurious~~ spurious signals. A quantitative

quantitative measure of noise immunity is called noise margin.

TTL are known their good noise immunity. The noise margin between the minimum input voltage level that ensures a low output and maximum input voltage level that ensures a high output, is a key parameter in assessing noise immunity.

Propagation delay:—

A logic signal always experiences a delay in going through a circuit. There are two propagation delay times are defined as follows:—

1. t_{PLH} : Delay time in going from logical 0 to logical 1 state (Low to High)
2. t_{PHL} : Delay time in going from logical 1 to logical 0 state. (High to Low)



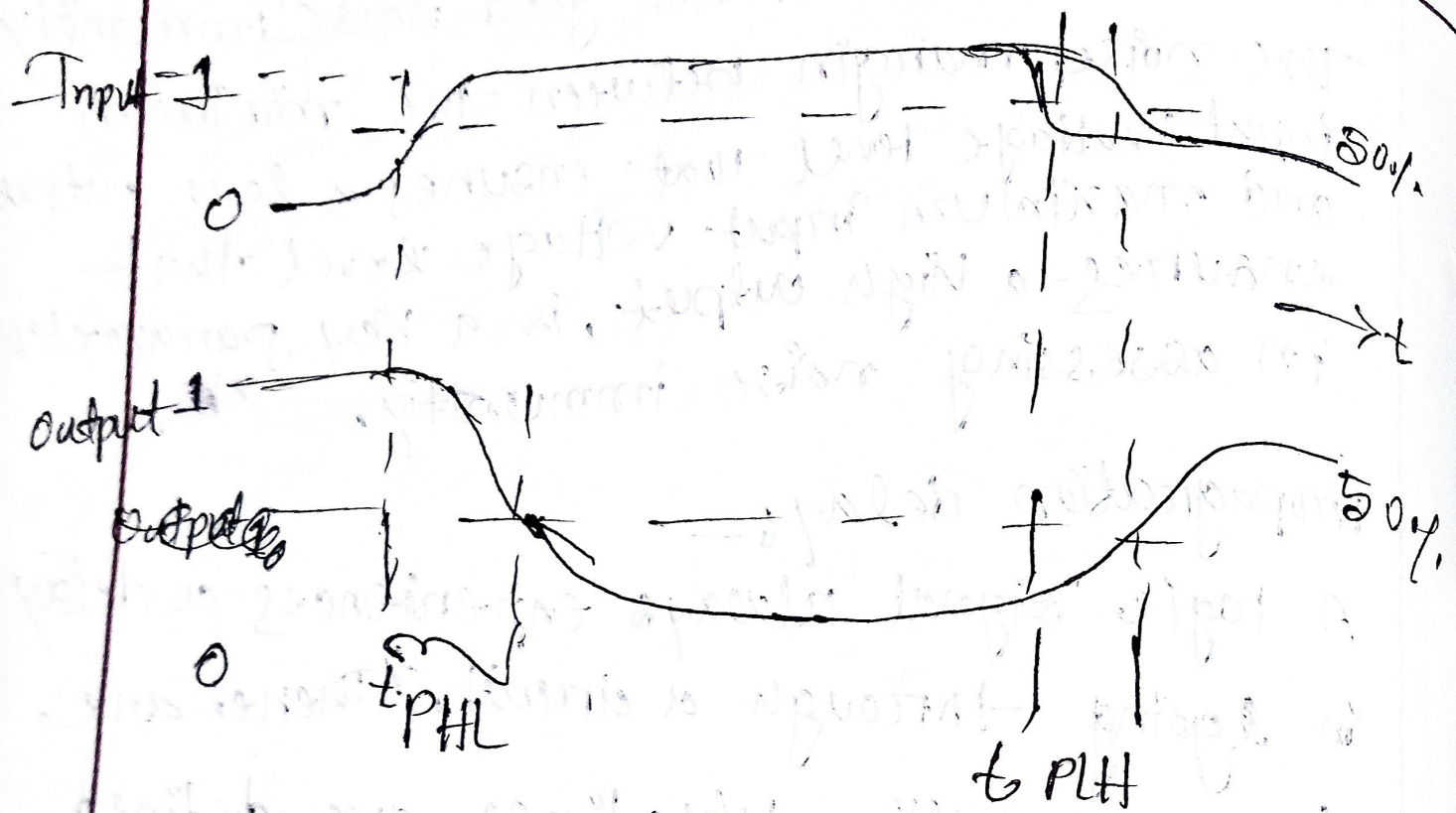


Fig: propagation delay

characteristic of TTL:

- (i) Fast switching speed
- (ii) Short propagation delay
- (iii) Moderate power consumption
- (iv) Fan-out typically around 10
- (v) Typical input voltage levels of 0-0.9V (logic 0) and 2-5V (logic-1)

Given, $I_{OH} = 800 \mu A$

$$I_{OL} = 48 mA$$

$$I_{UL} \Rightarrow \text{Unit load} = 40 \mu A \text{ (high)}$$

$$I_{UL} = 1.6 mA \text{ (low)}$$

For High state:

$$\text{Fan-out} = \frac{I_{OH}}{I_{UL}} = \frac{800}{40} = 20$$

For low state:

$$\text{Fan-out} = \frac{I_{OH}}{I_{UL}} = \frac{48}{1.6}$$

$$= 30$$

Ans

TTL

CMOS

Transistor Transistor
logic

Complementary Metal Oxide
Semiconductor

uses bipolar
junction Transistor

uses Field Effect Transistor

Lower density
than CMOS

Higher density than TTL

consume more
power

consume less power

Less susceptible
to static charges

More susceptible to
static charges

Operate at low
speed

operate at high speed

Lower fan-out
capability

Higher fan-out capability

Noise immunity is
low

Noise immunity is high