

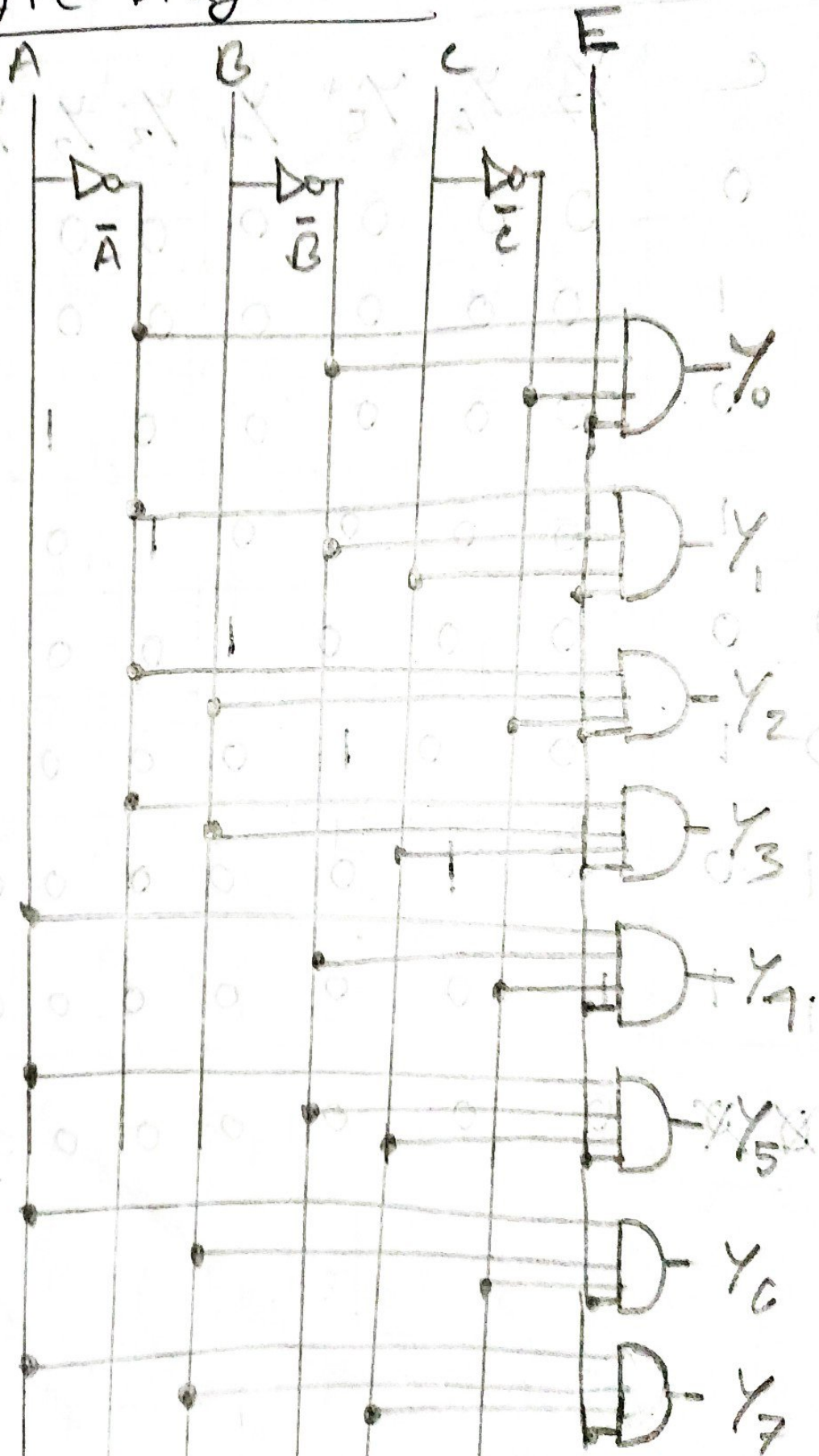
DLD

20-21

Truth table: $F(a)$

E	A	B	C	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	
1	0	0	0	0	0	0	0	0	0	0	1	$Y_0 = \bar{A}\bar{B}\bar{C}$
1	0	0	1	0	0	0	0	0	0	1	0	$Y_1 = \bar{A}\bar{B}C$
1	0	1	0	0	0	0	0	0	1	0	0	$Y_2 = \bar{A}B\bar{C}$
1	0	1	1	0	0	0	0	1	0	0	0	$Y_3 = \bar{A}BC$
1	1	0	0	0	0	0	1	0	0	0	0	$Y_4 = A\bar{B}\bar{C}$
1	1	0	1	0	0	1	0	0	0	0	0	$Y_5 = A\bar{B}C$
1	1	1	0	0	1	0	0	0	0	0	0	$Y_6 = AB\bar{C}$
1	1	1	1	1	0	0	0	0	0	0	0	$Y_7 = ABC$
0	X	X	X	0	0	0	0	0	0	0	0	

Logic Diagram



AVAILABLE AT:

7(b)

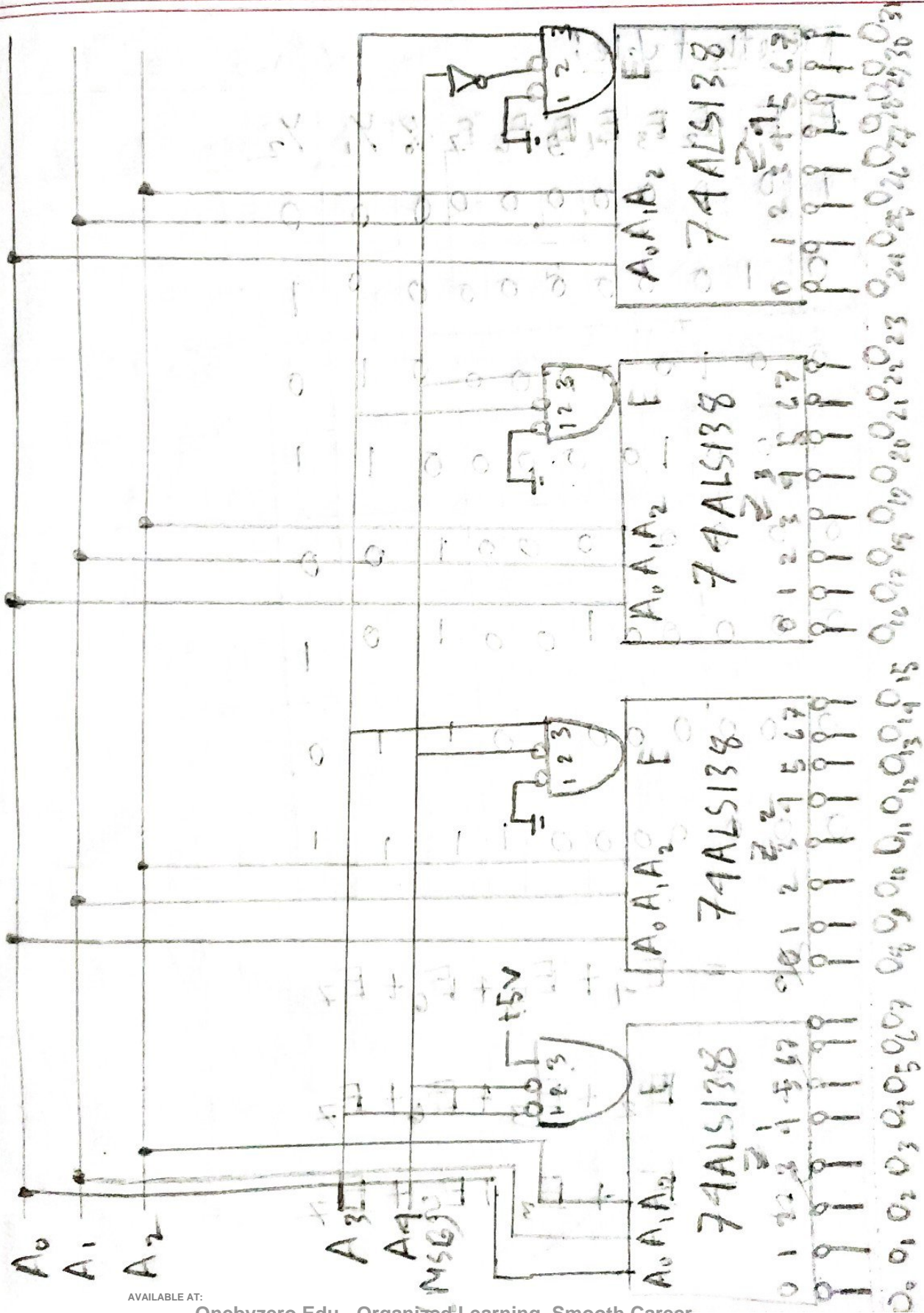


Fig: 1 of 32 decoder.

AVAILABLE AT:

$Z(c)$

Truth table:

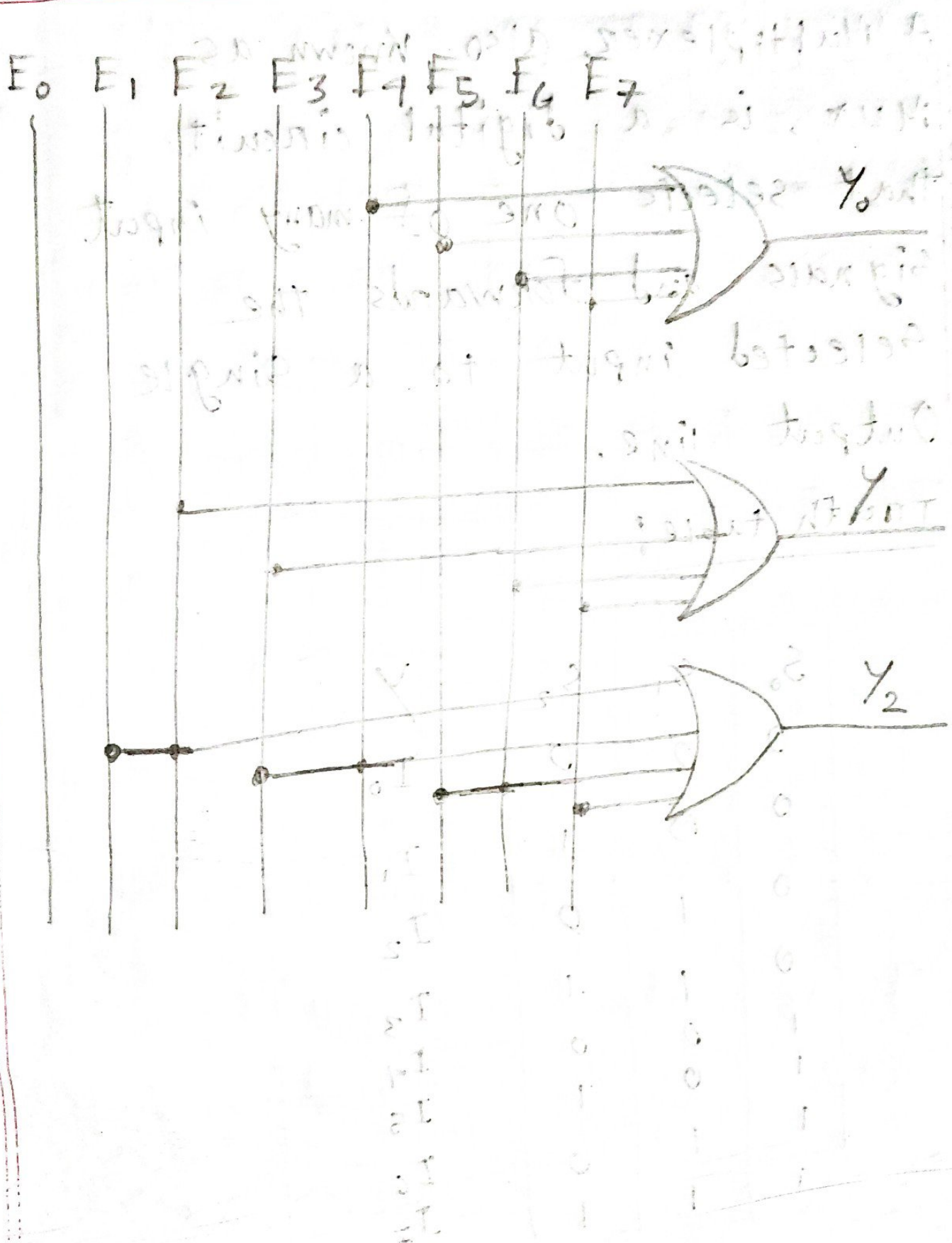
E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	Y_0	Y_1	Y_2
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

$$Y_0 = E_4 + E_5 + E_6 + E_7$$

$$Y_1 = E_2 + E_3 + E_6 + E_7$$

$$Y_2 = E_1 + E_3 + E_5 + E_7$$

(1)E



AVAILABLE AT:

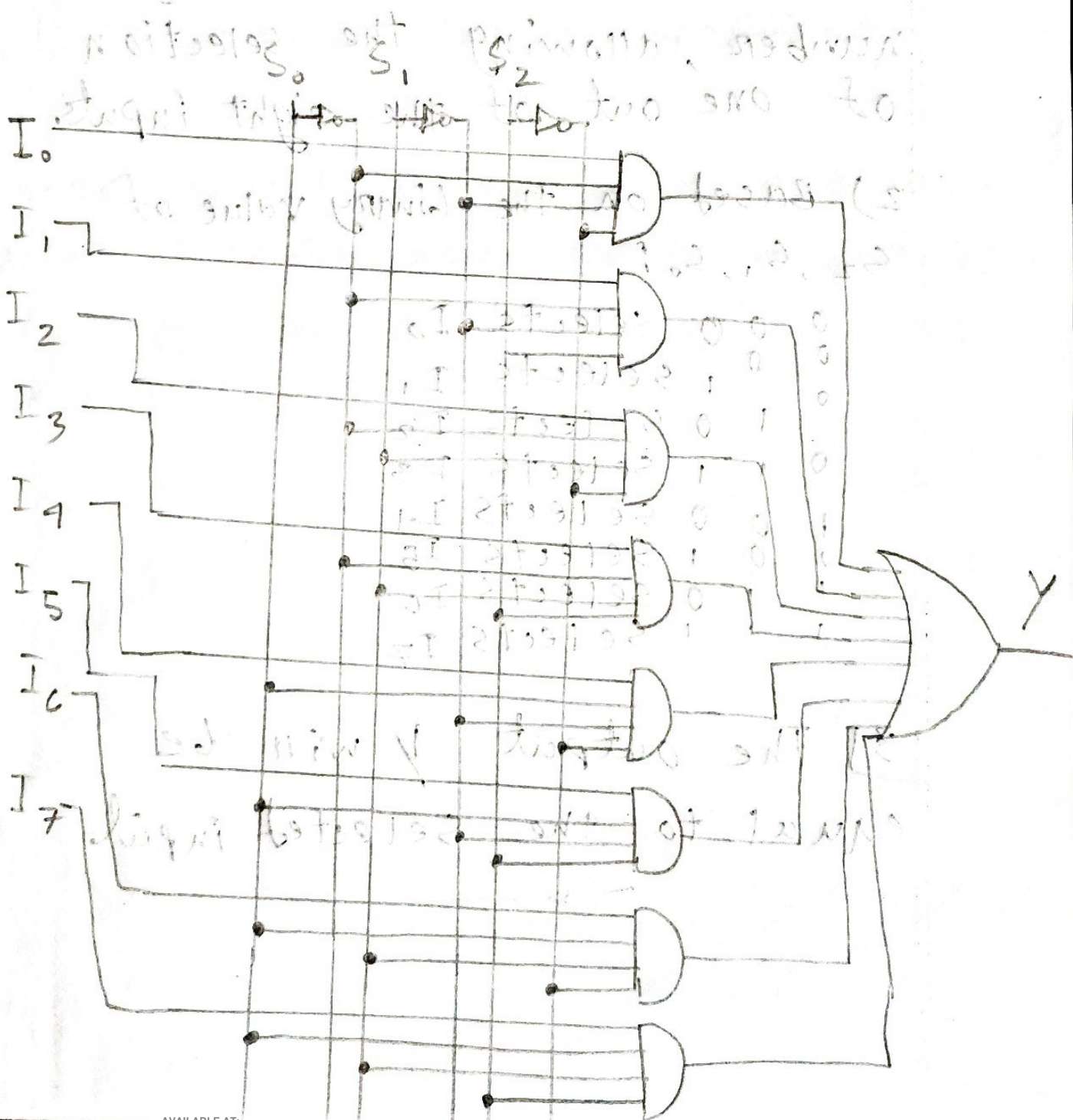
8(a)

A Multiplexer, also known as Mux, is a digital circuit that selects one of many input signals and forwards the selected input to a single output line.

Truth table:

S_0	S_1	S_2	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

$$Y = \bar{S}_0 \bar{S}_1 \bar{S}_2 I_0 + \bar{S}_0 \bar{S}_1 S_2 I_1 + \bar{S}_0 S_1 \bar{S}_2 I_2 + \bar{S}_0 S_1 S_2 I_3 + S_0 \bar{S}_1 \bar{S}_2 I_4 + S_0 \bar{S}_1 S_2 I_5 + S_0 S_1 \bar{S}_2 I_6 + S_0 S_1 S_2 I_7$$



Operation of an 8 input Mux

1) The three select lines S_2, S_1, S_0 create a 3-bit binary number, allowing the selection of one out of the eight inputs.

2) Based on the binary value of S_2, S_1, S_0 :

0	0	0	selects	I_0
0	0	1	selects	I_1
0	1	0	selects	I_2
0	1	1	selects	I_3
1	0	0	selects	I_4
1	0	1	selects	I_5
1	1	0	selects	I_6
1	1	1	selects	I_7

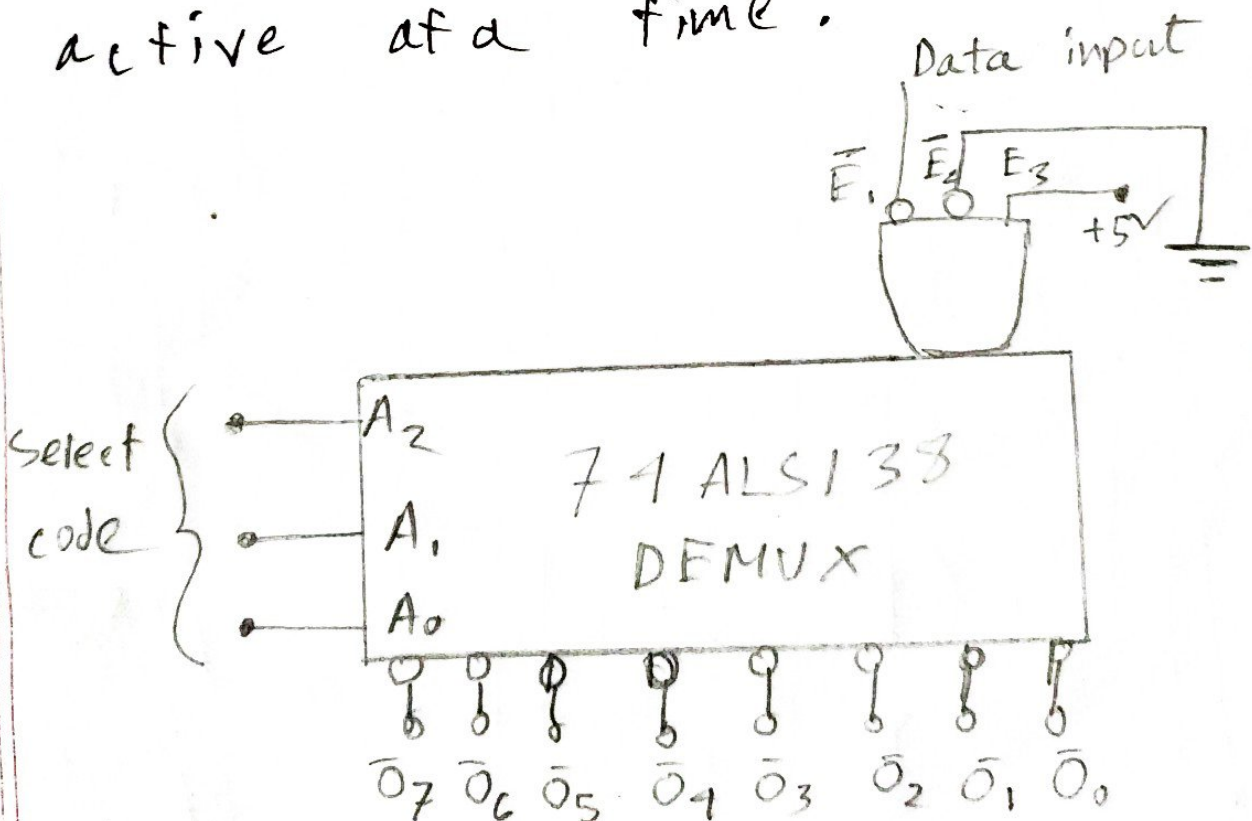
3) The output Y will be equal to the selected input.

Q(b)

Using 74138 IC as a DEMUX.

Data input: The signal that needs to be demultiplexed is applied at one of the enable inputs, specifically E_3 in this case.

here, selection inputs are A_2, A_1, A_0 .
And outputs are O_0 to O_7 . Only one of the output lines will be active at a time.

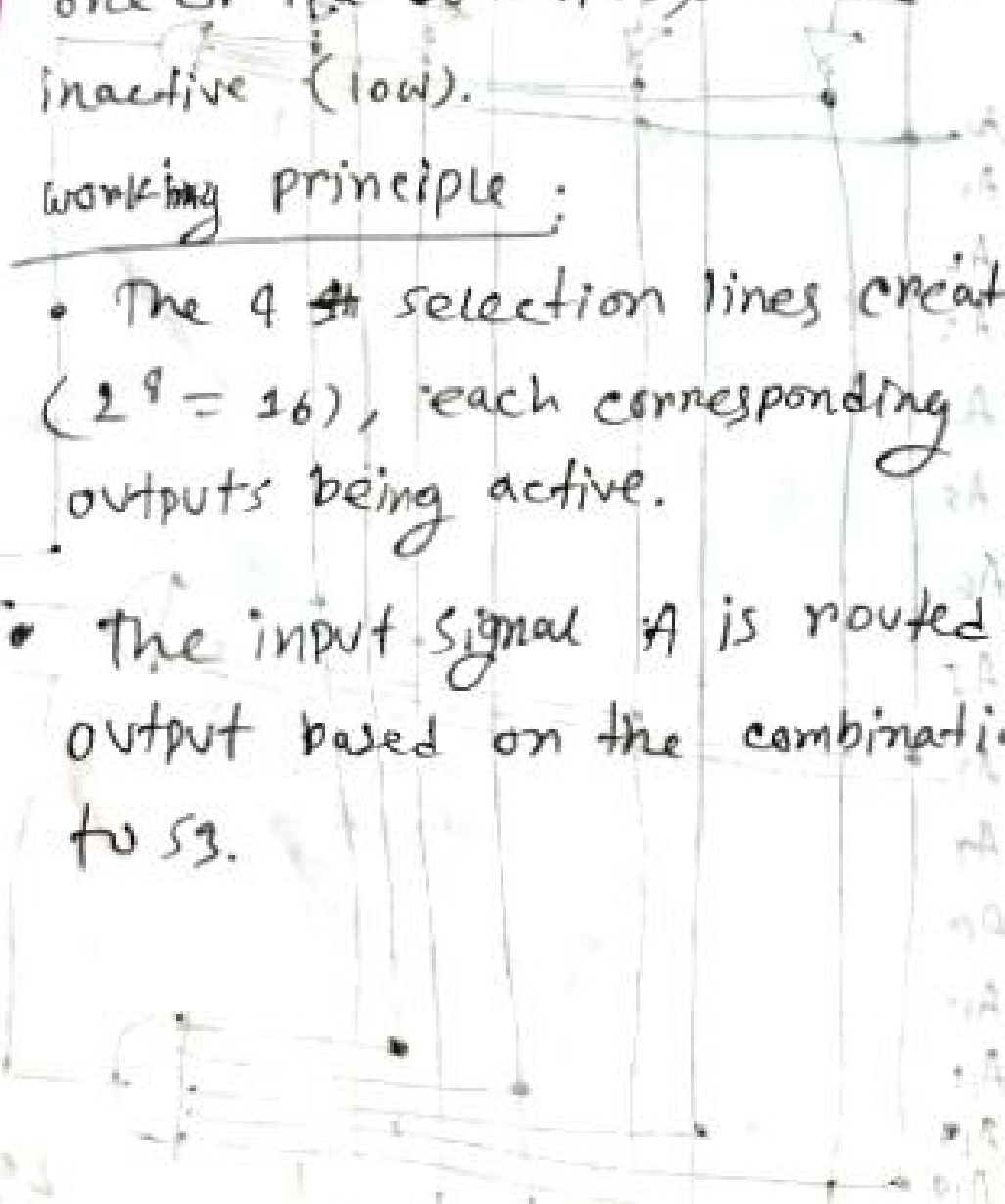


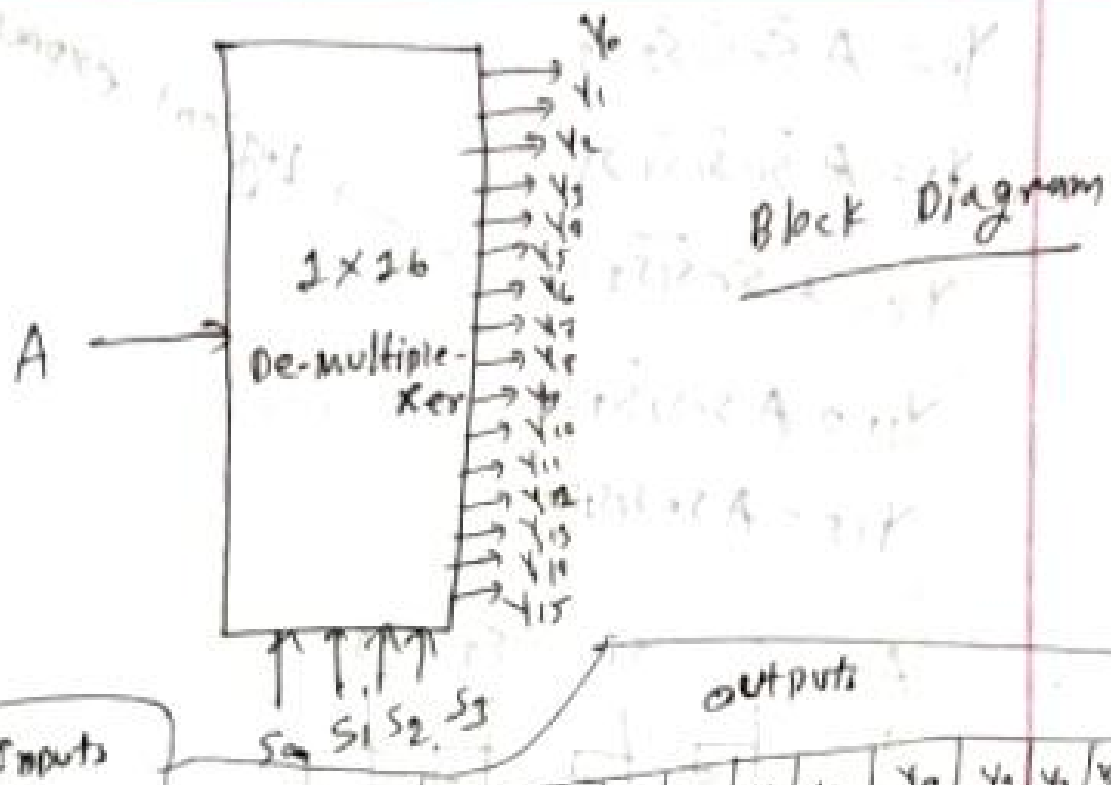
Q5) with appropriate diagram explain the working principle of a 1 line to 16 line Demultiplexer.

A 1-to-16 Demultiplexer has one input (A), 4 selection lines (S_0, S_1, S_2, S_3), and 16 outputs (Y_0 to Y_{15}). Based on the combination of selection lines, the input is routed to one of the 16 outputs, while all others are inactive (low).

Working principle:

- The 4 selection lines create 16 combinations ($2^4 = 16$), each corresponding to one of the outputs being active.
- The input signal A is routed to the selected output based on the combination of S_0 to S_3 .





truth table →

Inputs				Outputs																												
S ₃	S ₂	S ₁	S ₀	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇	Y ₈	Y ₉	Y ₁₀	Y ₁₁	Y ₁₂	Y ₁₃	Y ₁₄	Y ₁₅	Y ₁₆	Y ₁₇	Y ₁₈	Y ₁₉	Y ₂₀	Y ₂₁	Y ₂₂	Y ₂₃	Y ₂₄	Y ₂₅	A		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

$$Y_0 = A \bar{S}_0 \bar{S}_1 \bar{S}_2 \bar{S}_3$$

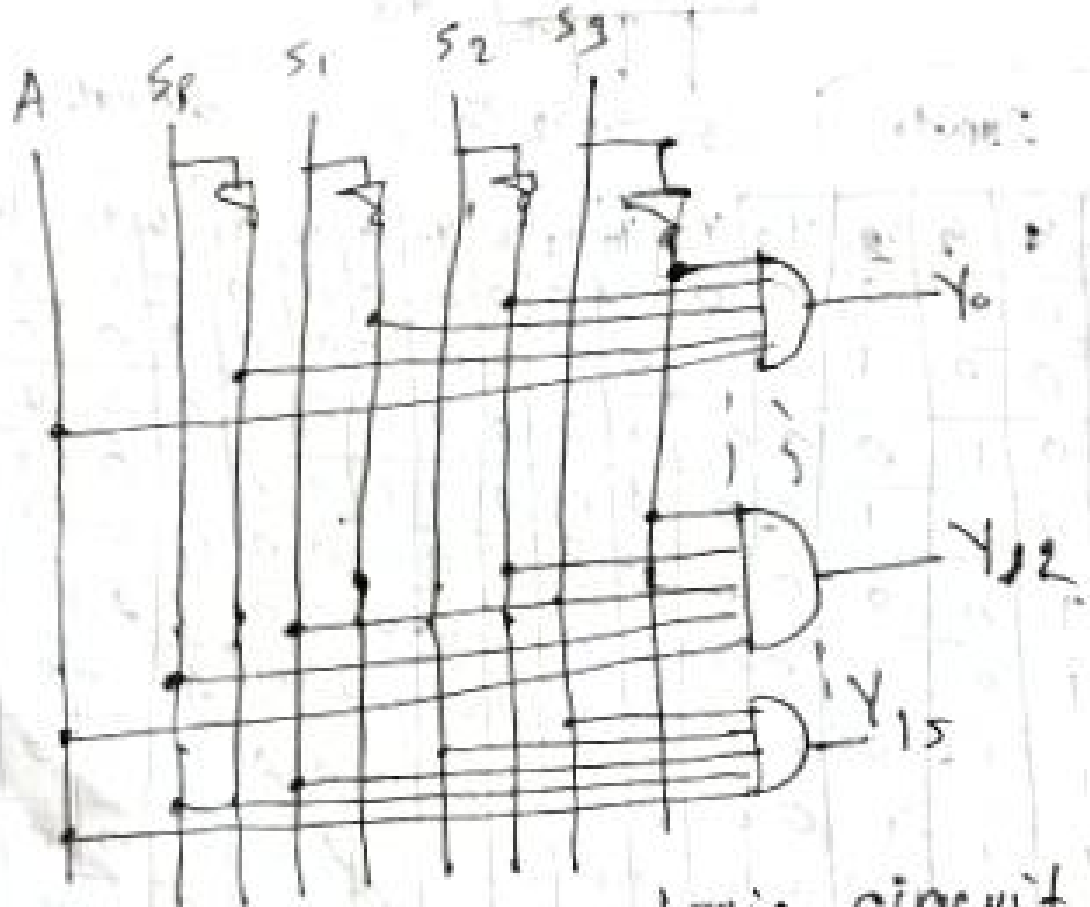
$$Y_1 = A \bar{S}_0 \bar{S}_1 \bar{S}_2 S_3$$

$$Y_2 = A \bar{S}_0 \bar{S}_1 S_2 \bar{S}_3$$

$$Y_3 = A \bar{S}_0 S_1 \bar{S}_2 \bar{S}_3$$

$$Y_4 = A \bar{S}_0 S_1 S_2 \bar{S}_3$$

Logical expression



Logic circuit

Q6) Draw the diagram and truth table of an octal to Binary encoder.

Inputs								Outputs		
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	A ₂	A ₁	A ₀
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

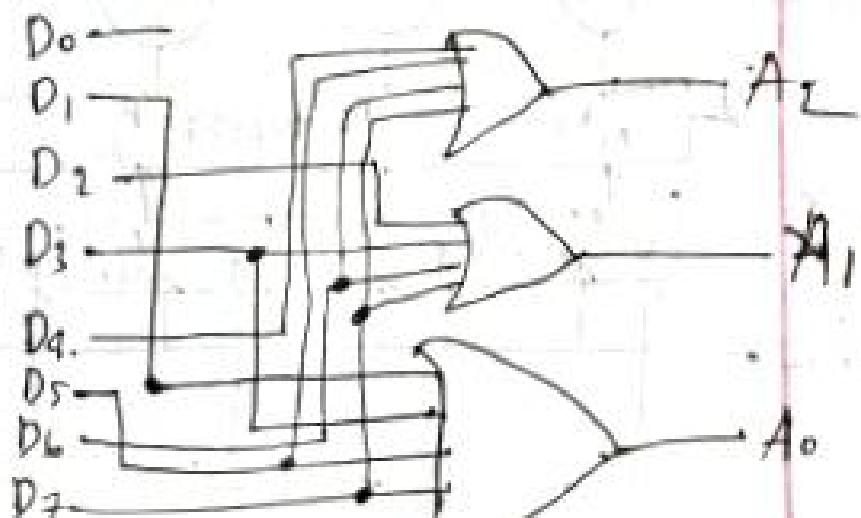
Truth table

$$A_0 = D_1 + D_3 + D_5 + D_7$$

$$A_1 = D_2 + D_3 + D_6 + D_7$$

$$A_2 = D_4 + D_5 + D_6 + D_7$$

Logic Diagram



selects one of many input signals and forwards it to a single output based on control signals.

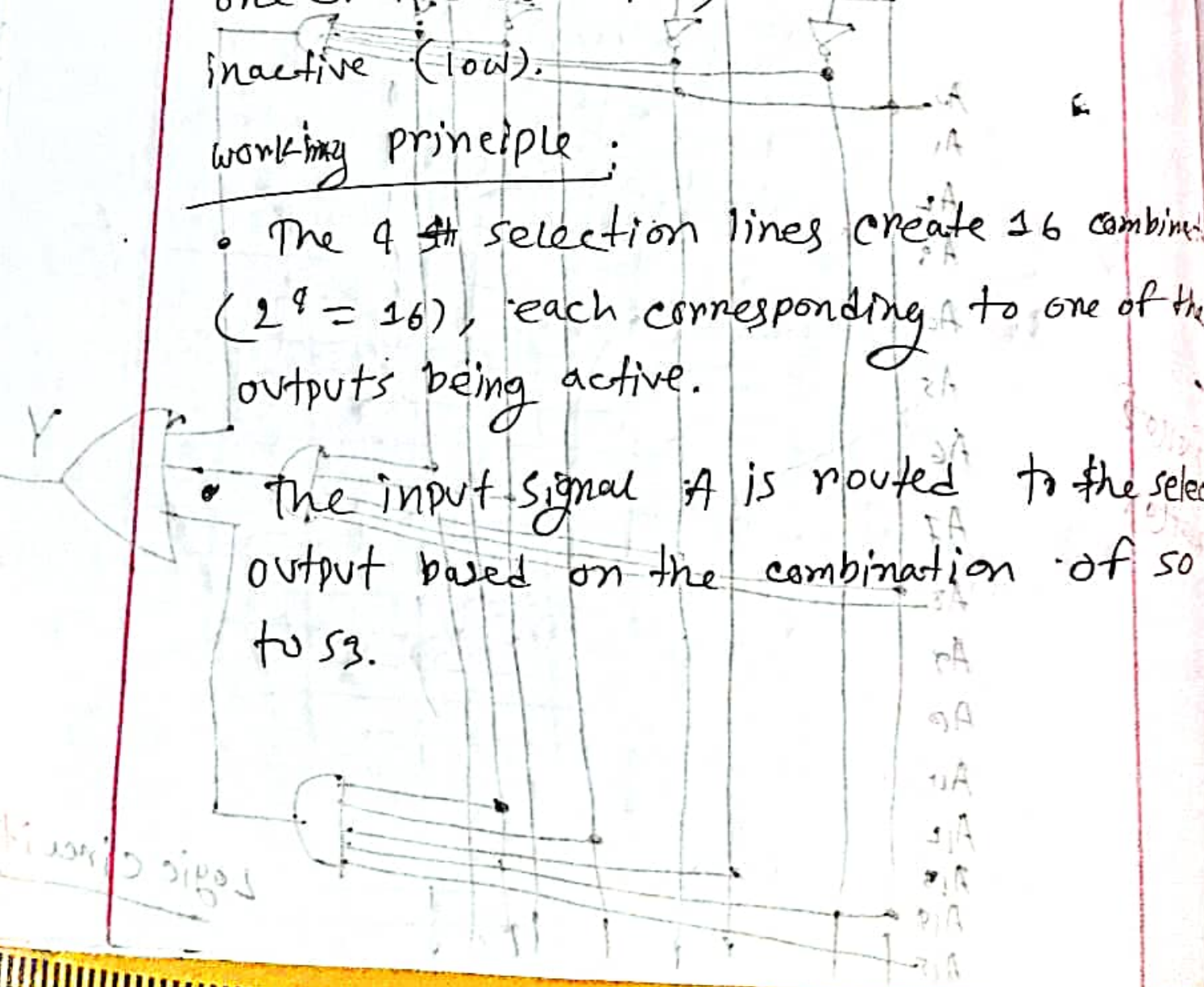
Multiplexer (MUX): A multiplexer is a digital switch that selects one of many input signals and forwards it to a single output line based on control signals (selection lines). It is also known as a data selector.

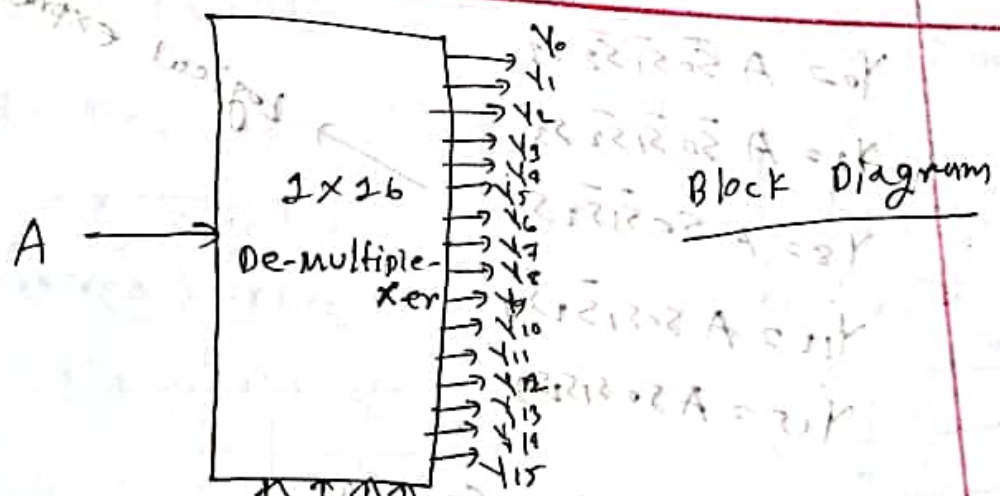
Q35) with appropriate diagram explain the working principle of a 1 line to 16 line Demultiplexer.

A 1-to-16 Demultiplexer has one input (A), 4 selection lines (S_0, S_1, S_2, S_3), and 16 outputs (Y_0 to Y_{15}). Based on the combination of selection lines, the input is routed to one of the 16 outputs; while all others are inactive (low).

Working principle:

- The 4 selection lines create 16 combinations ($2^4 = 16$), each corresponding to one of the outputs being active.
- The input signal A is routed to the select output based on the combination of S_0 to S_3 .





Block Diagram

truth table

Inputs				Outputs A																
S ₀	S ₁	S ₂	S ₃	Y ₁₅	Y ₁₄	Y ₁₃	Y ₁₂	Y ₁₁	Y ₁₀	Y ₉	Y ₈	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	A
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	A	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	A	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	A	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	A	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	A	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	A	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	A	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	A	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	A	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	A	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	A	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	A	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	A	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Demultiplexer (DEMUX): A demultiplexer takes a single input signal and routes it to one of many output lines based on control signals (selection lines). It is reverse operation of a multiplexer.

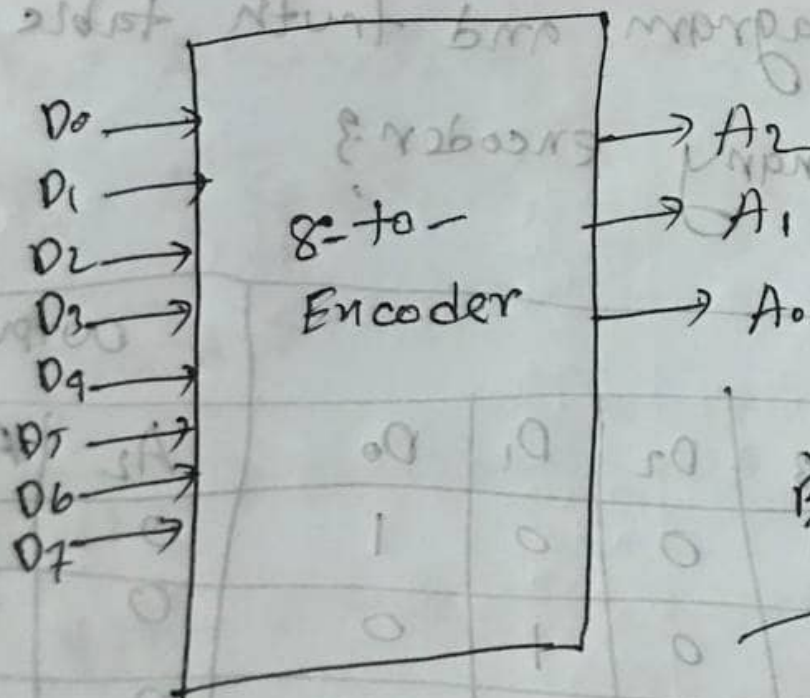
Exm: working principle of a 16-to-1 multiplexer?

A 16-to-1 multiplexer has 16 input lines (A_0 to A_{15}), 4 selection lines (S_0 to S_3), and output (Y). It selects one of the 16 inputs based on the combination of the 4 selection lines.

Working principle

- The 4 selection lines (S_0 to S_3) create 16 combinations ($2^4 = 16$), each selecting one of the 16 inputs.

	S_3	S_2	S_1	S_0
A_0	0	0	0	0
A_1	1	0	0	0
A_2	0	1	0	0
A_3	1	1	0	0
A_4	0	0	1	0
A_5	1	0	1	0
A_6	0	1	1	0
A_7	1	1	1	0
A_8	0	0	0	1
A_9	1	0	0	1
A_{10}	0	1	0	1
A_{11}	1	1	0	1
A_{12}	0	0	1	1
A_{13}	1	0	1	1
A_{14}	0	1	1	1
A_{15}	1	1	1	1



Block Diagram.

36) Draw the diagram and truth table of an octal to Binary encoder.

Inputs								Outputs		
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	A ₂	A ₁	A ₀
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	1
0	0	1	0	0	0	0	0	1	1	0
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

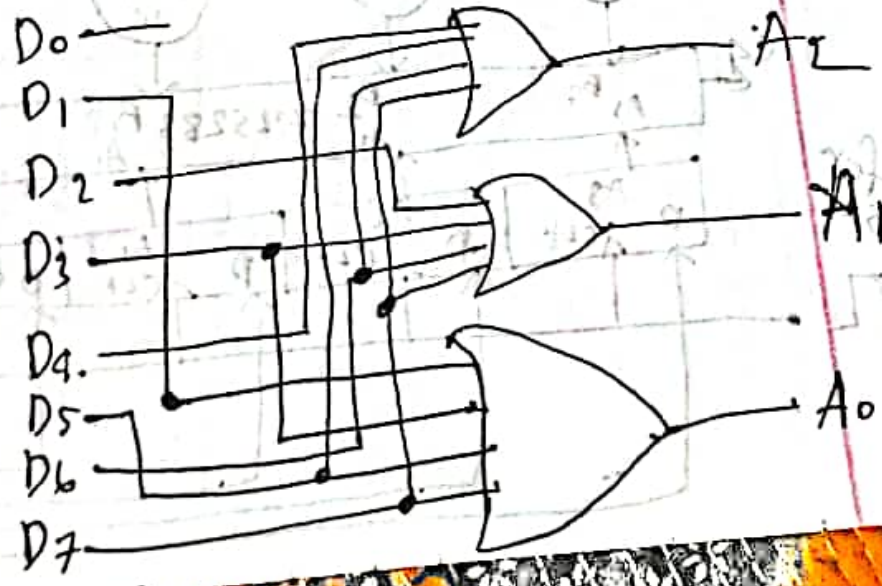
Truth table

$$A_0 = D_1 + D_3 + D_5 + D_7$$

$$A_1 = D_2 + D_3 + D_6 + D_7$$

$$A_2 = D_4 + D_5 + D_6 + D_7$$

Logic Diagram



$$Y_0 = A \bar{S}_0 \bar{S}_1 \bar{S}_2 \bar{S}_3$$

$$Y_2 = A \bar{S}_0 \bar{S}_1 \bar{S}_2 S_3$$

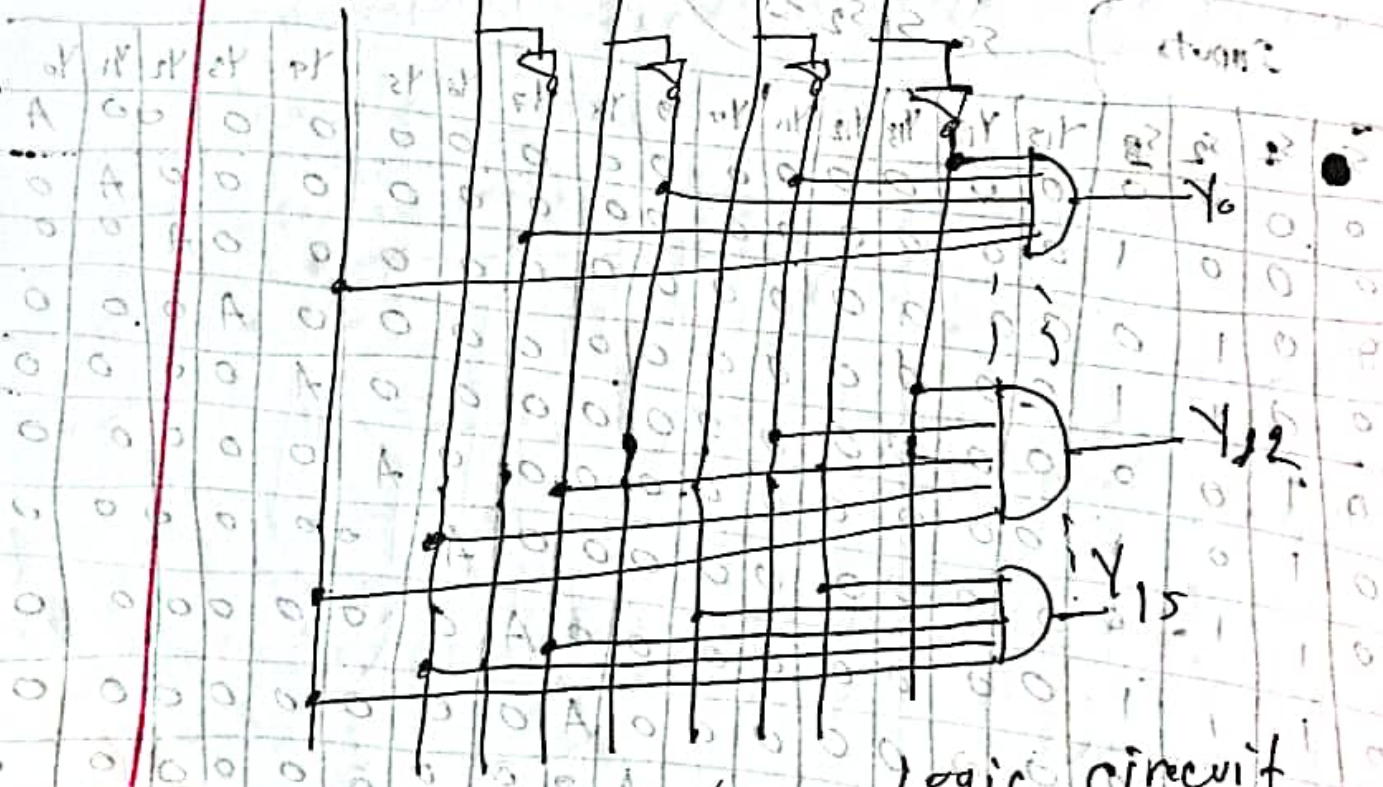
$$Y_8 = A \bar{S}_0 \bar{S}_1 S_2 \bar{S}_3$$

$$Y_{12} = A \bar{S}_0 \bar{S}_1 S_2 S_3$$

$$Y_{15} = A S_0 S_1 S_2 S_3$$

Logical expression

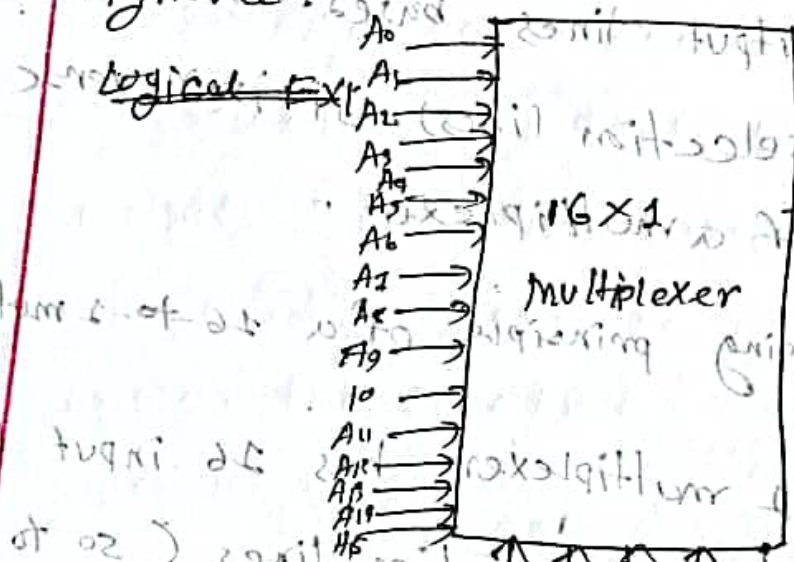
A S_0 S_1 S_2 S_3



Logic circuit

কিছু কিছু

The selected input is connected to the output (Y), while the other inputs are ignored.



Block Diagram

Input				Output
S ₀	S ₁	S ₂	S ₃	Y
0	0	0	0	A ₀
0	0	0	1	A ₁
0	0	1	0	A ₂
0	0	1	1	A ₃
0	1	0	0	A ₄
0	1	0	1	A ₅
0	1	1	0	A ₆
0	1	1	1	A ₇
1	0	0	0	A ₈
1	0	0	1	A ₉
1	0	1	0	A ₁₀
1	0	1	1	A ₁₁
1	1	0	0	A ₁₂
1	1	0	1	A ₁₃
1	1	1	0	A ₁₄
1	1	1	1	A ₁₅

truth table

Logical Expression

$$Y = A_0 \bar{S}_0 \bar{S}_1 \bar{S}_2 \bar{S}_3 + A_1 \bar{S}_0 \bar{S}_1 \bar{S}_2 S_3 + A_2 \bar{S}_0 \bar{S}_1 S_2 \bar{S}_3 + A_3 \bar{S}_0 \bar{S}_1 S_2 S_3 + A_4 \bar{S}_0 S_1 \bar{S}_2 \bar{S}_3 + A_5 \bar{S}_0 S_1 \bar{S}_2 S_3 + A_6 \bar{S}_0 S_1 S_2 \bar{S}_3 + A_7 \bar{S}_0 S_1 S_2 S_3 + A_8 S_0 \bar{S}_1 \bar{S}_2 \bar{S}_3 + A_9 S_0 \bar{S}_1 \bar{S}_2 S_3 + A_{10} S_0 \bar{S}_1 S_2 \bar{S}_3 + A_{11} S_0 \bar{S}_1 S_2 S_3 + A_{12} S_0 S_1 \bar{S}_2 \bar{S}_3 + A_{13} S_0 S_1 \bar{S}_2 S_3 + A_{14} S_0 S_1 S_2 \bar{S}_3 + A_{15} S_0 S_1 S_2 S_3$$

02/10/2021

