TOPIC NAME : _____ DAY : _____

TIME : DATE : / /

Chapter - 8

Digital IC

- A chip is a small piece of semiconductor material
- Using advance photographic, miniature circuits can be produced on the surface of the chip.
- The components (resistors, diode, transistor) are an integral part of the chip.

Level of Integration:

Digital IC's can be classified according to the number of gates on a chip, this is referred as level of integration.

IC classification	Number of gates on a chip
Small scale integration (SSI)	Less than 12
Medium " " (MSI)	12 to 99
Large " " (LSI)	100 to 999
very large scale " (VLSI)	1000 to 9999
Ultra " " (ULSI)	10,000 or more

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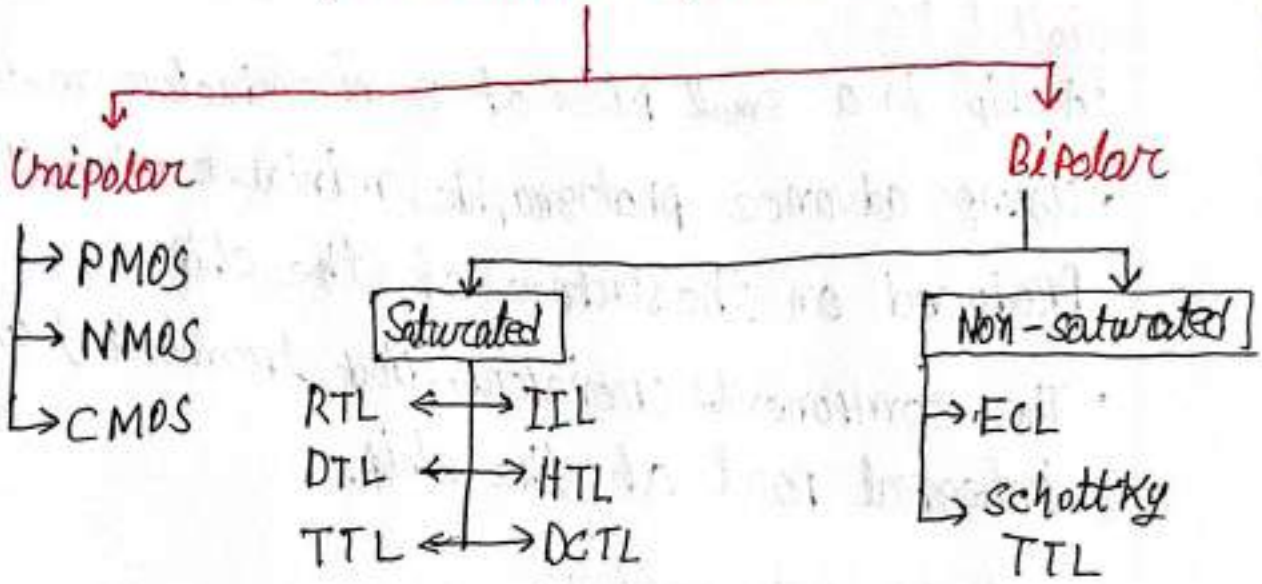
TOPIC NAME : _____ DAY : _____

TIME : DATE : / /

Semiconductor Digital IC's



Logic Family

→ Unipolar Logic Family :

↳ In unipolar logic families, unipolar devices are the key element.

↳ MOSFET (Metal oxide semiconductor Field Effect Transistor) is a unipolar devices, in which the current flows because of only one type of charge carriers

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TOPIC NAME : _____ DAY _____

TIME : DATE : / /

→ Bipolar Logic Family :

↳ Transistors and diodes are bipolar devices, in which the current flown because of both the charge carriers (electrons and holes).

↳ In bipolar logic families, transistors and diodes are used as key element.

- PMOS : P- channel MOSFET family
- NMOS : N- " " "
- CMOS : Complementary " "
- RTL : Resistor transistor logic
- DCTL : Direct coupled " "
- IIL : integrated injection logic
- DTL : Diode transistor logic
- HTL : High threshold logic
- TTL : Transistor transistor logic
- ECL : Emitter coupled logic

TOPIC NAME : _____ DAY : _____

TIME : DATE : / /

Characteristics of IC's

1. Propagation Delay (speed)
2. Power dinipation
3. figure of merit
4. Fan-in / Fan-out
5. current and voltage parameters
6. Noise Immunity
7. operating Temperature

1. Propagation Delay (speed)

- The propagation delay is defined as "the time required to change the output from one logic ~~sate~~ state to other logic sate after input is applied."
- Manufacturer specifies the speed of digital family in terms of propagation delay.
- practically propagation delay is calculated by measuring the two propagation delays.

1. t_{PHL}: Delay required to change from ~~a~~ high to low sate

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TOPIC NAME : _____ DAY : _____

TIME : DATE : / /

2. t_{PLH}: Delay required to change from low to heigh

- Higher is the propagation delay. lower is the speed.

2. Power Dissipation:

- It is indirectly related with propagation delay.
- Low power dissipation is desirable because it generates less heat and therefore it avoids cooling, power supply and cost problem.
- Low power dissipation means it should operate with minimum voltage within minimum current.
- The required current can be adjusted by increasing the resistance but it increases the time because $T = R \times C$
- For example, a gate takes 2mA current and it is operated with 5V supply then its power dissipation per gate is calculated as

power dissipation $= 2mA \times 5V = 10mW$

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TOPIC NAME : _____ DAY : _____

TIME : DATE : / /

3. Figure of Merit

- This characteristics indicates the total performance or quality of a family.
- If resistance of the circuit is increased to reduce the current or power dissipation then the propagation delay increases.
- In opposite way, if we reduce the propagation delay to make it faster by reducing the resistance then more current is drawn by the gate which increases the power dissipation
- It is defined as "the product of propagation delay and power dissipation" of the gate
- Figure of merit is measured in terms of "pJ"

$$\text{figure of merit} = F.M = t_p \times P_D$$
$$= 1 \text{ns} \times 1 \text{mW}$$
$$= 1 \text{pJ}$$

- The lowest figure of merit indicates the best performance

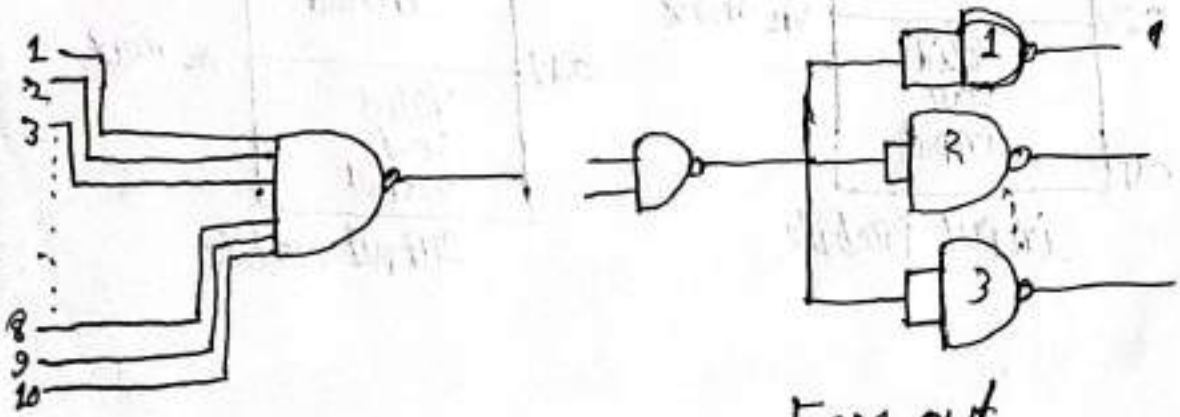
TOPIC NAME : _____ DAY : _____

TIME : DATE : / /

4. Fan In - Fan out

The capacity of driving the loads of a gate is expressed in terms of fan out.

- Fan in is the "number of inputs to a gate".
- Fan out is also known as loading factor.
- E.g. in case of TTL fan in and fan out is 10 that is maximum 10 TTL gates can be connected to the output terminal of a TTL gate.



Fan-in

Fan out

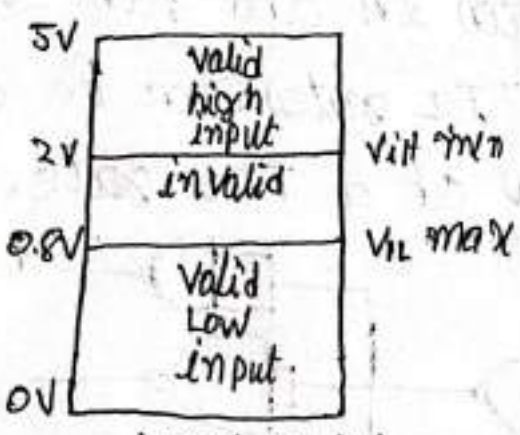
~~5. Manufacturer Specifics~~.

TOPIC NAME : _____ DAY : _____

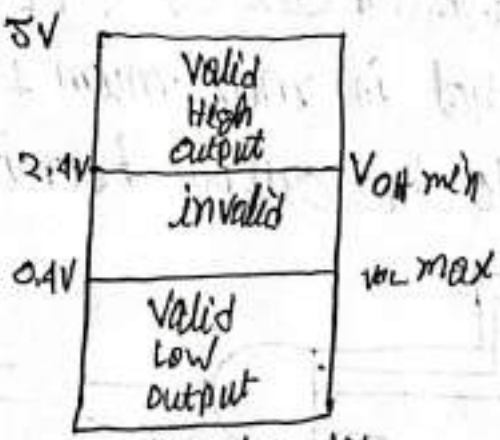
TIME : DATE : / /

5. Current and voltage parameters

- Manufacturer specifies these parameters in the data book, which are useful in designing of digital circuits.
- This is also known as worst case current and voltage parameters.



input Profile



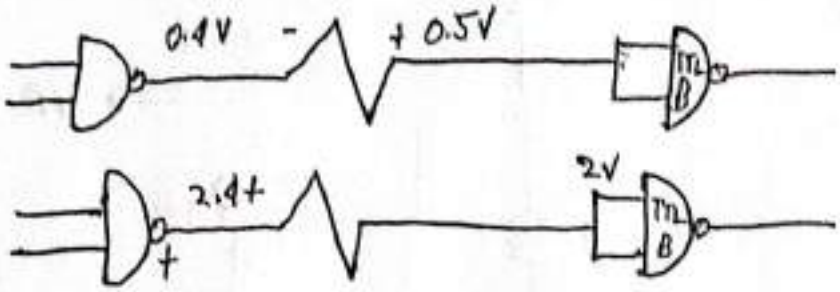
Output Profile

TOPIC NAME : _____ DAY _____

TIME : DATE / /

6. Noise Immunity (Noise Margin)

- The maximum noise voltage a device can withstand without making a false change in output
- The noise may be an external signal generated by vehicle ignition, signal generator.



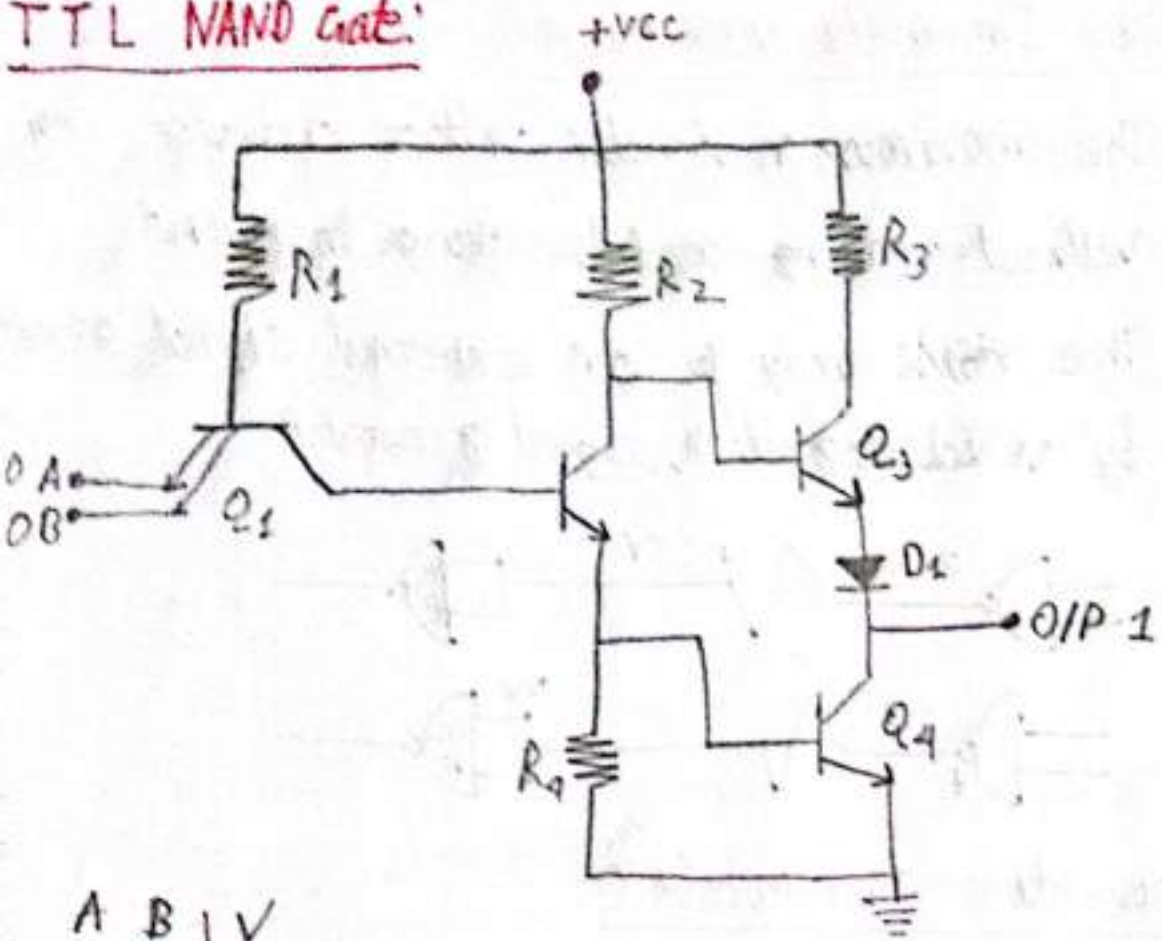
7. Operating Temparature

- Manufacturer specifies the temparature range in which the device operates properly.
- For industrial and consumer application the temparature range is 0 to 70°C
- For military applications it is 55 to 125°C
- In case of, TTL, 74XX series it for industrial and consumer applications while 54XX series is for military application.

TOPIC NAME _____ DAY _____

TIME _____ DATE :

TTL NAND Gate:

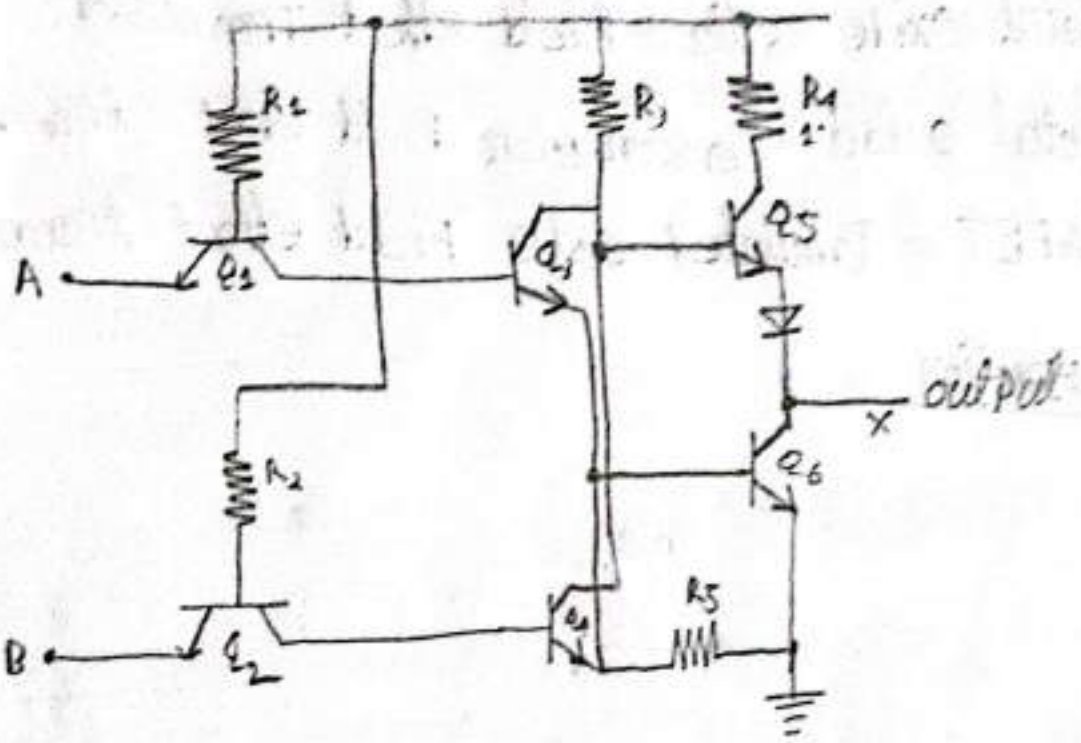


A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

TOPIC NAME : _____ DAY _____

TIME : DATE / /

TTL NOR Gate:



Q_5 = ON = output = High(1)

Q_6 = ON = output = Low(0)

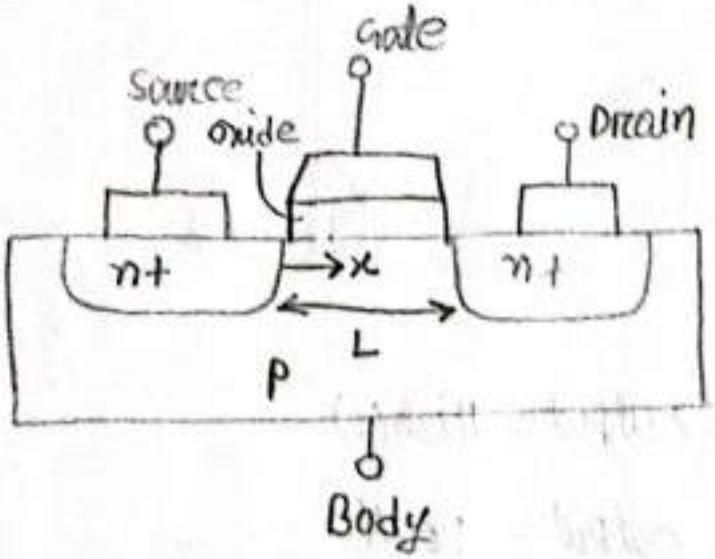
A	B	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Y
0	0	ON	ON	OFF	OFF	ON	OFF	1
0	1	ON	OFF	OFF	ON	OFF	ON	0
1	0	OFF	ON	ON	OFF	OFF	ON	0
1	1	OFF	OFF	ON	ON	OFF	ON	0

TOPIC NAME ..... DAY .....
TIME ..... DATE ..... / ..... / .....

~~Mos.fet~~
MOSFET

- Metal oxide silicon Field effect Transistor
- Metal oxide Semiconductor Field effect transistor
- IGFET = Insulated Gate Field effect transistor

Construction



- Four-terminal device having source(S), gate(G), drain(D) and body(B) terminals.
- An oxide layer is deposited on the substrate & the gate terminal is connected to it.
- This oxide layer acts as an insulator

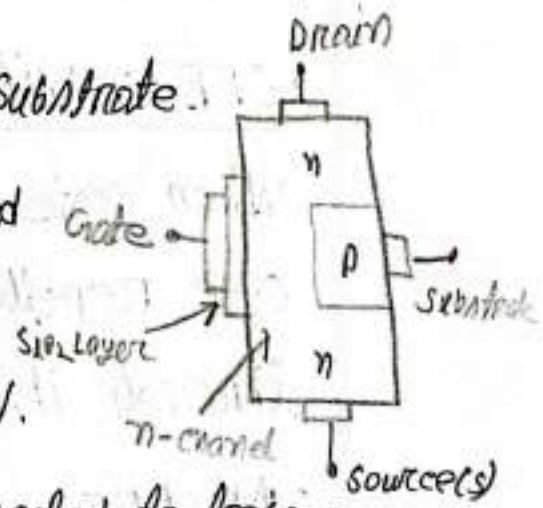
TOPIC NAME : _____ DAY : _____

TIME : DATE : / /

- In the construction of MOSFET, a lightly doped substrate, is diffused with a heavily doped region.
- Depending upon the substrate used, they are called as P-type and N-type MOSFETs.

N channel MOSFET

- N channel bar
- P type material is doped as a substrate.
- ON condition: When gate is connected to logic 1, electrons flow from source to drain & NMOS turns ON.



- OFF condition: When gate is connected to logic 0, electrons are repelled & can't flow from source and drain, current becomes zero.
- MOSFET is in cutoff region.

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TOPIC NAME : _____ DAY : _____

TIME : DATE : / /

P channel MOSFET

- P channel bar.
- N type meterial is doped as a substrate.
- **ON condition:** When gate is connected to logic 0, holes attracted towards gate & then flow drain.
- MOSFET is in saturation region.
- **OFF condition:**

When gate is connected to logic 1, high voltage holes are repelled by gate hence current can't flow through it.

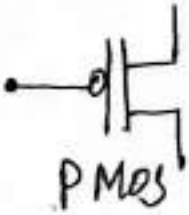
- MOSFET is in cutoff region.

Remember

Switching condition:

Input	N channel	P channel
$V_{in} = 0$	OFF	ON
$V_{in} = 1$	ON	OFF

NMos



PMos

TOPIC NAME : CMOS

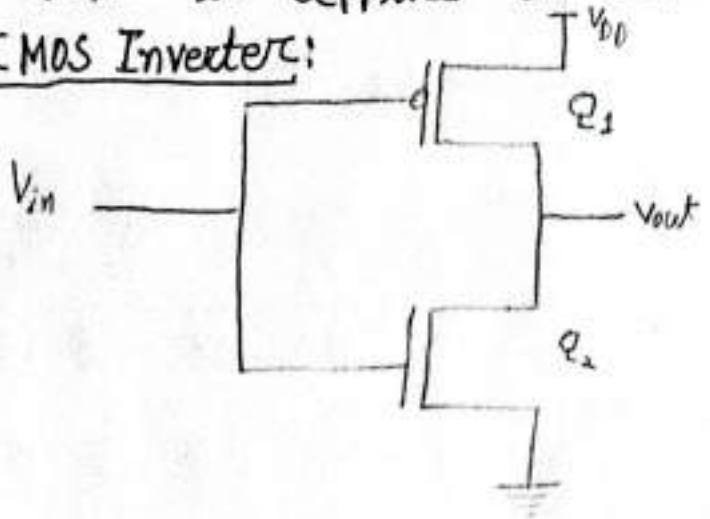
DAY :

TIME : DATE : / /

CMOS Logic

- P channel and N channel MOSFET are connected in series
- output is taken from common point of Drain.
- Input is applied at common point of Gate.

CMOS Inverter:



V_{in}	Q_1	Q_2	V_{out}
0	on	off	1
1	off	on	0

Q_1 = PMOS (on = 0)

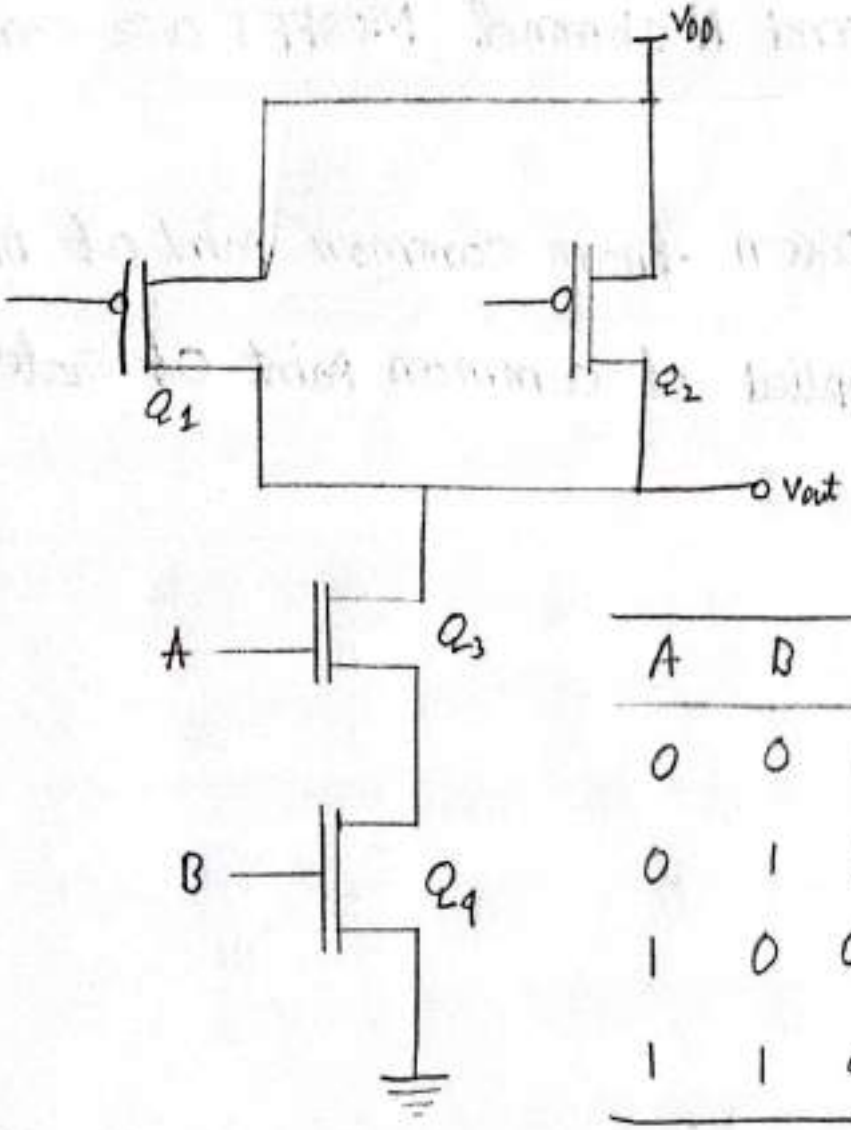
Q_2 = NMOS (on = 1)

CMOS NAND

TOPIC NAME : _____ DAY : _____

TIME : DATE : / /

CMOS NAND



A	B	Q_1	Q_2	Q_3	Q_4	Vout
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	1

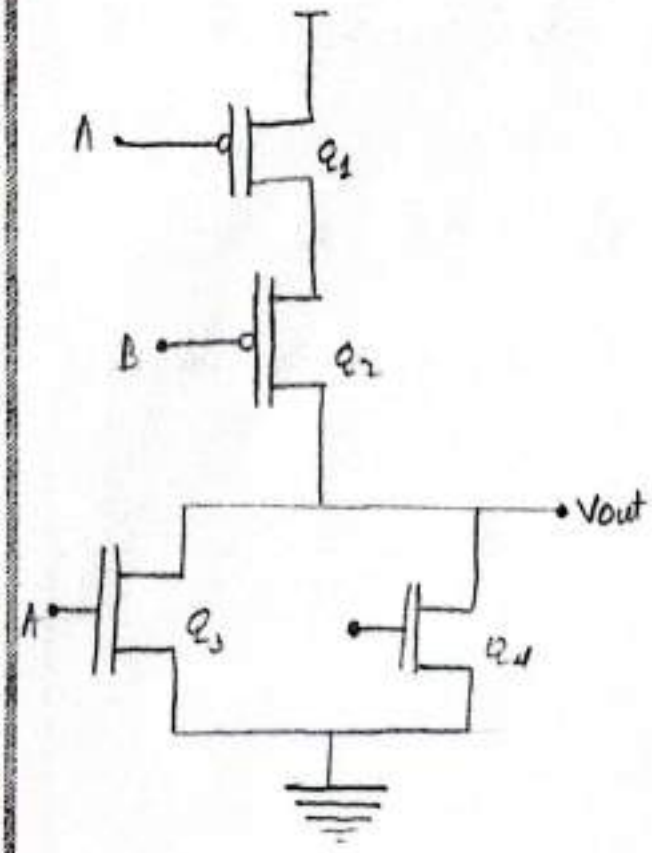
Q_1, Q_2 = PMOS (on = 0)

Q_3, Q_4 = NMOS (on = 1)

TOPIC NAME : _____ DAY : _____

TIME : DATE : / /

CMOS NOR



A	B	Q_1	Q_2	Q_3	Q_4	V_{out}
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

Q_1, Q_2 = PMOS (on = 0)

Q_3, Q_4 = NMOS (on = 1)

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DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

UNIVERSITY OF BARISAL

Final Examination

Course Title: Digital Logic Design

Course Code: CSE-2103

2nd Year 1st Semester

Session: 2020-21 (Admission Session 2019-20)

Time: 3 hour **Marks:** 60

Answer any five Questions from the followings.

1. a) Implement the Boolean function [3]

$$F = xy + x'y' + y'z$$

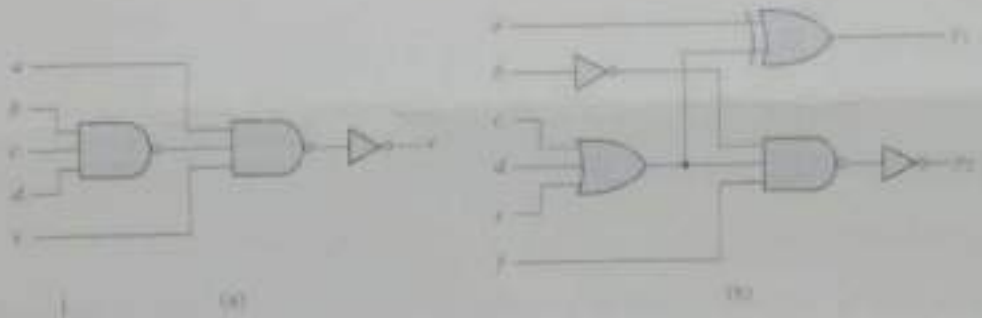
i. With AND, OR, and inverter gates,

ii. With NOR and inverter gates,

iii. With NAND and inverter gates.

b) Show that a positive logic NAND gate is a negative logic NOR gate and vice versa. [3]

c) Write Boolean expressions and construct the truth tables describing the outputs of the circuits described by the following logic diagrams: [6]



2. a) Express the following function as a sum of minterms and as a product of maxrerms: [2]

$$F(A,B,C,D) = B'D + A'D + BD$$

b) Simplify the following Boolean functions, using *Karnaugh* maps: [6]

$$F(w,x,y,z) = \sum(2,3,12,13,14,15)$$

$$F(A,B,C,D) = \sum(0,2,4,5,6,7,8,10,13,15)$$

c) Implement the following Boolean function F, together with the don't-care conditions d, using no more than two NOR gates: [4]

$$F(A,B,C,D) = \sum(2,4,6,10,12)$$

$$d(A,B,C,D) = \sum(0,8,9,13)$$

Assume that both the normal and complement inputs are available.

3. a) Explain how a NAND/NOR latch store a bit. Mention their limitations. [3]

b) What is the limitation of S-R flip-flop? Explain how the limitation can be resolved. [4]

c) Define race-around condition in J-K flip-flop. How can you overcome the problem? Explain with an appropriate figure and waveforms. [5]

4. a) What is the limitation of a parallel adder? Using 74LS83 ICs, draw a 16 bit parallel Adder. [3]

b) Explain how 2's complement system can facilitate arithmetic operations in digital computing. [3]

c) Draw a parallel adder/subtractor using 2's-complement system and explain its operations. [6]

5. a) Draw a Mod-14 and a Decade ripple counter with their state transition diagram. [4]

b) Show how to wire the 74293 IC as a MOD-6 counter. [2]

c) Explain the operation of a Synchronous up/down MOD-8 counter with an appropriate diagram. [6]

6. a) Write short notes on the followings: [5]

I) Fan-Out

II) Noise Immunity

III) Propagation delay

IV) Characteristics of TTL logic gate.

b) Design and explain the working principle of a TTL NOR gate. [5]

c) A certain TTL IC output is rated at $I_{OH}(max) = 800\ \mu A$ and $I_{OL} = 48$ mA. Express the IC's fan-out in terms of unit loads. [consider 1UL = 40 μA in the HIGH state and 1.6 mA in the LOW state] [2]

7. a) Design a 1 of 8 decoder using logic gates. [4]

b) Use 74LS138 ICs to design a 1 of 32 decoder. [5]

c) Draw the internal diagram of a 8:1 encoder. [3]

8. a) What is Multiplexer? Design an 8-input MUX and explain its operation. [4]

b) How can you use a 74138 IC as a DEMUX? Explain with diagram. [4]

c) Draw the logic diagram for the 7442 BCD to decimal decoder. [4]

6. a) Write short notes on the followings: [5]

I) Fan-Out

II) Noise immunity

III) Propagation delay

IV) Characteristics of TTL logic gate.

b) Design and expiain the working principie of a TTL NOR gate. [5]

c) A certain TTL IC output is rated at $I_{OH}(max) = 800\ \mu A$ and $I_{OL} = 48$ mA. Express the IC's fan-out in terms of unit loads. [consider 1UL = 40 μA in the HIGH state and 1.6 mA in the LOW state] [2]

I) Fan-Out

- **Definition**: Fan-out is the maximum number of inputs that a digital logic gate output can drive without degradation in performance.
- **Explanation**: It represents the load capacity of a gate; higher fan-out means it can connect to more subsequent gates.
- **Importance**: Essential for ensuring signal integrity across connected components in a circuit.

ii) Noise Immunity

- **Definition**: Noise immunity is a measure of a circuit's ability to tolerate external electrical noise without malfunctioning.
- **Explanation**: High noise immunity ensures that signals remain unaffected by minor fluctuations or interference in voltage.
- **Importance**: Critical for reliable performance in environments with electrical interference, as it prevents data corruption and errors.

iii) Propagation Delay

- **Definition**: Propagation delay is the time taken for a signal to pass from the input to the output of a gate.
- **Explanation**: It measures the speed of a gate and affects the overall speed of digital circuits.
- **Importance**: Lower propagation delays allow for faster data processing in digital systems.

IV) Characteristics of TTL Logic Gate

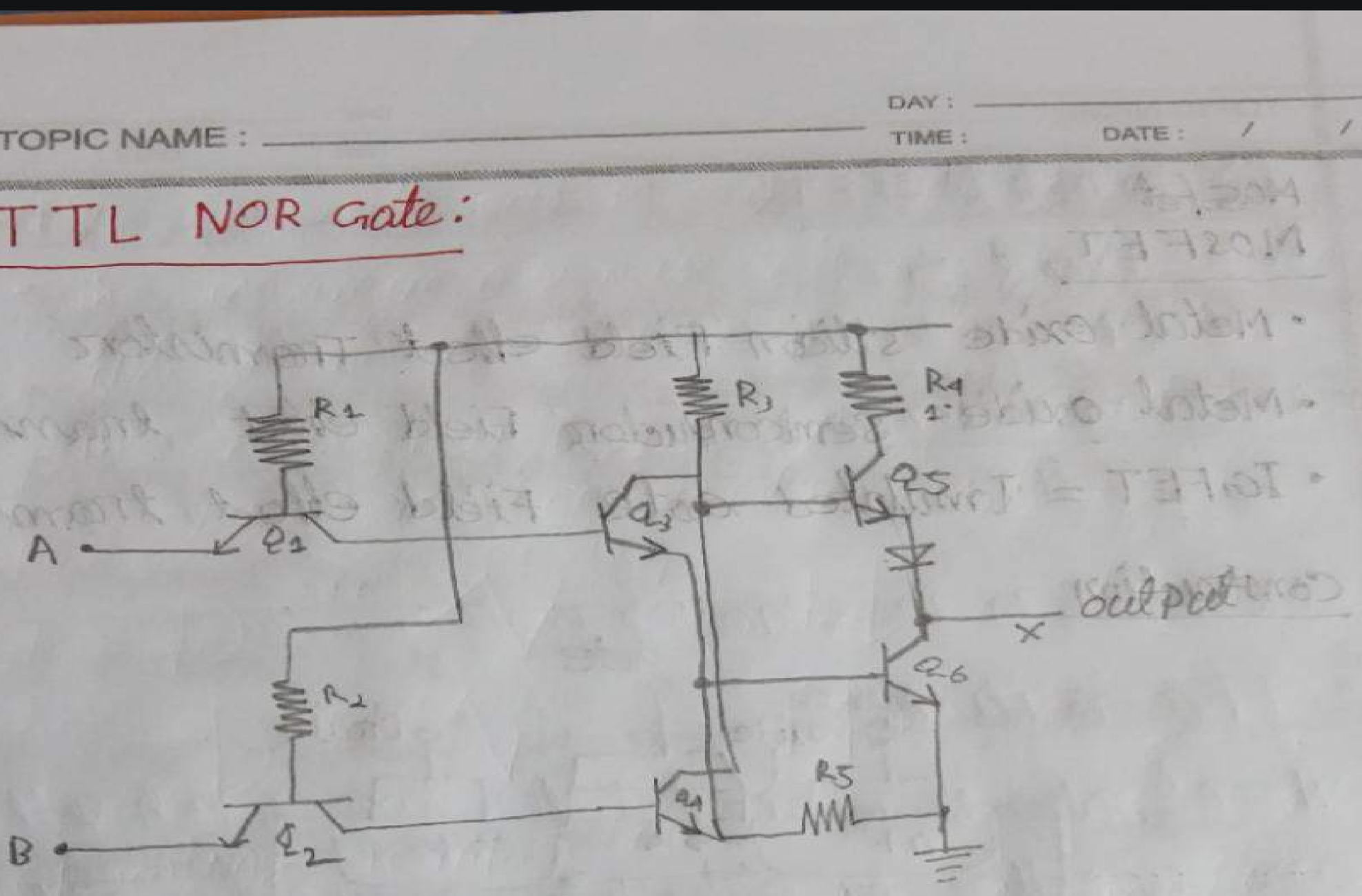
- **Speed**: TTL (Transistor-Transistor Logic) gates are relatively fast, with moderate propagation delay.
- **Power Consumption**: TTL circuits consume more power than some other logic families, like CMOS, but less than older logic types.
- **Noise Immunity**: TTL has moderate noise immunity, making it suitable for most general-purpose applications.
- **Fan-Out**: TTL logic gates usually have a fan-out of 10, meaning they can drive up to 10 standard TTL inputs.
- **Voltage Levels**: TTL operates typically at a 5V power supply with a distinct logic 0 (0V) and logic 1 (~5V).

b)

TOPIC NAME : _____ DAY : _____

TIME : DATE : / /

TTL NOR Gate:



Q_5 = ON = output = High (1)

Q_6 = ON = output = Low (0)

A	B	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Y
0	0	ON	ON	OFF	OFF	ON	OFF	1
0	1	ON	OFF	OFF	ON	OFF	ON	0
1	0	OFF	ON	ON	OFF	OFF	ON	0
1	1	OFF	OFF	ON	ON	OFF	ON	0

A TTL NOR gate outputs a low (0) when any input is high (1) and outputs a high (1) only when all inputs are low (0).

Working Principle:

1. The gate uses a multi-emitter transistor for the inputs. If any input is high, this transistor conducts and keeps the output low (0).
2. When all inputs are low, no current flows in the input transistor, allowing the output to go high (1).

This structure provides the NOR logic, where the output is only high if all inputs are low.

c) Given data

$I_{OH(max)} = 800\,\mu A$

$I_{OL(max)} = 48\,mA$

In the high state, 1 UL = 40 μA

" " Low " , 1 UL = 1.6 mA

$$\text{Fan-out}_{(high)} = \frac{I_{OH}}{1\,UL} = \frac{800}{40} = 20\,UL$$

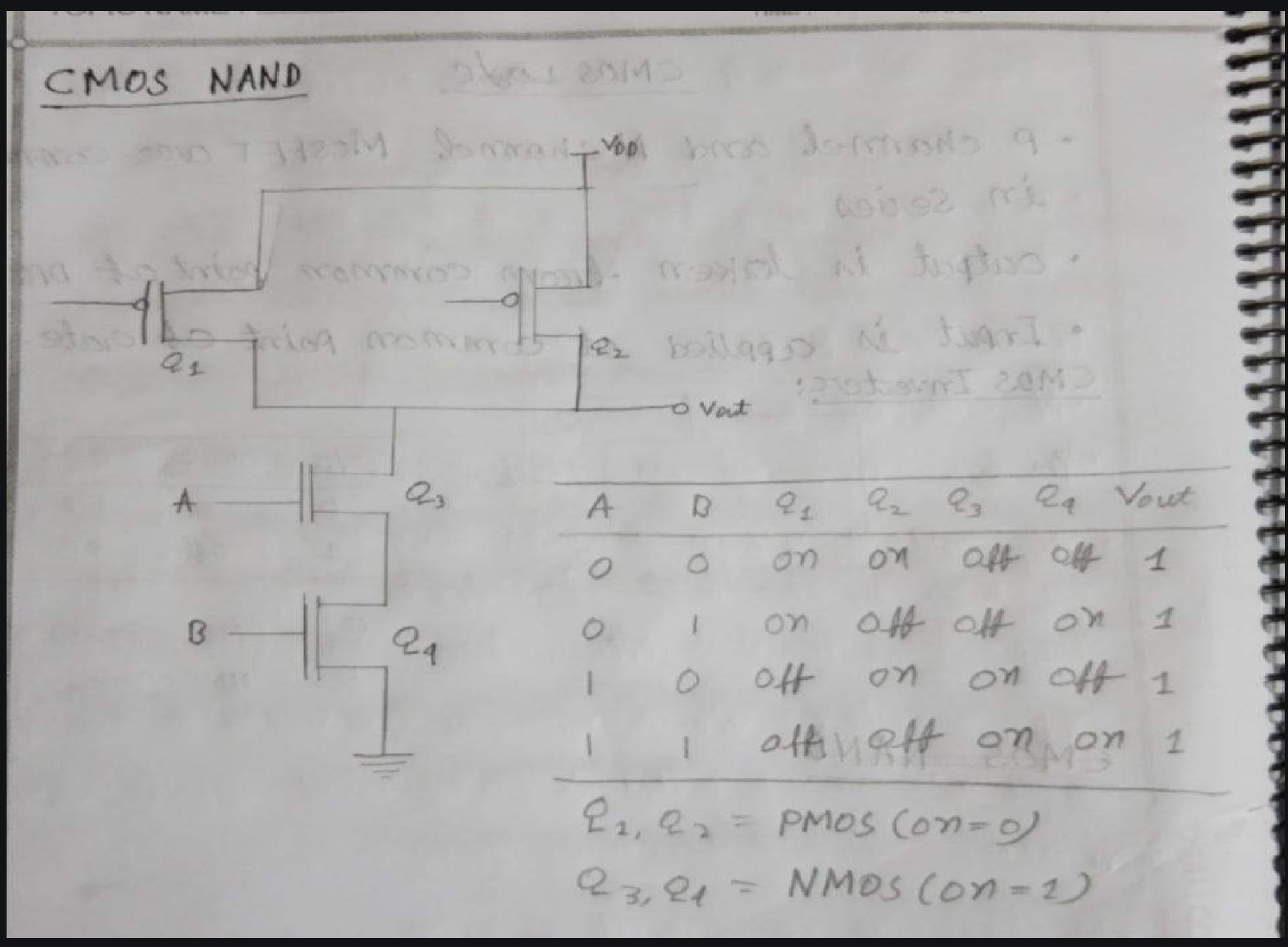
$$\text{Fan-out}_{(low)} = \frac{I_{OL}}{1\,UL} = \frac{48}{1.6} = 30\,UL$$

6. a) Explain the working principle of CMOS NAND and NOR gates.

   b) Draw the circuit diagrams of TTL NAND and NOR gates.

   c) Compare various characteristics of TTL and CMOS logic gate.

a)



A	B	Q_1	Q_2	Q_3	Q_4	Vout
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	1

Q_1, Q_2 = PMOS (on = 0)

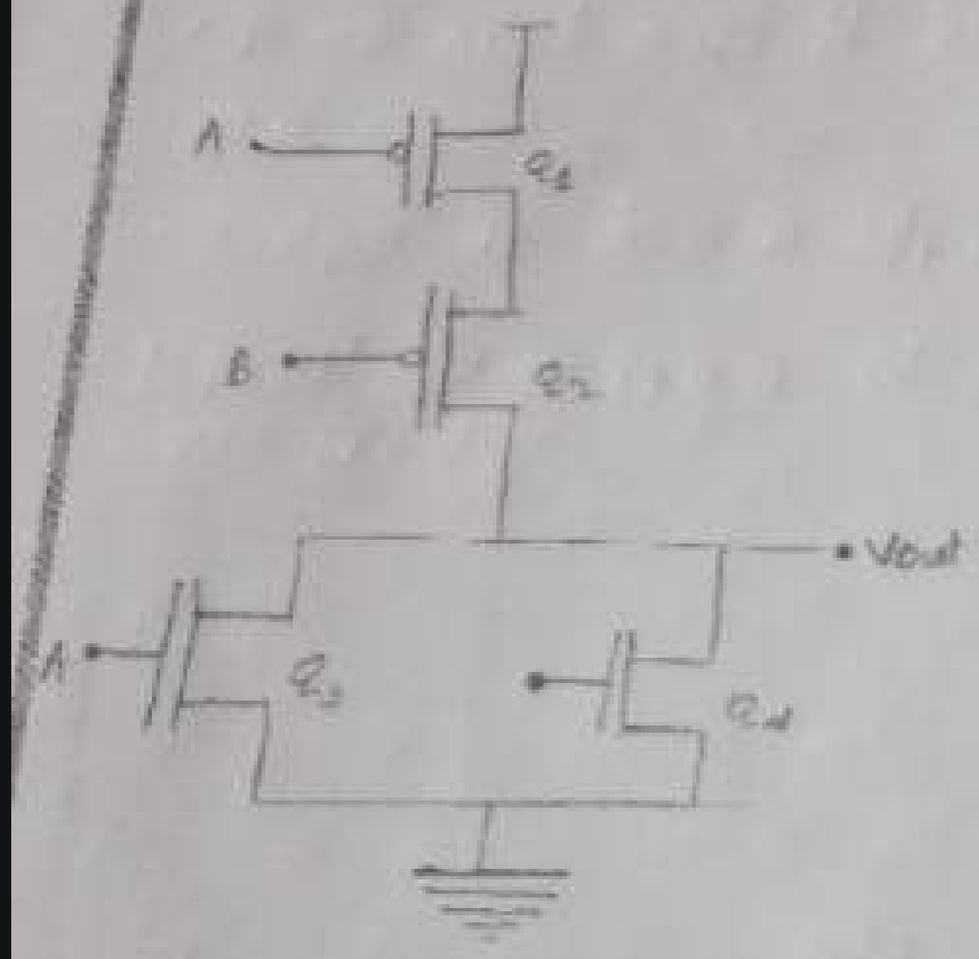
Q_3, Q_4 = NMOS (on = 1)

Working Principle:

- **When both inputs (A and B) are high (logic 1)**:
  - Both nMOS transistors conduct, creating a direct path to ground, pulling the output to low (logic 0).
  - Both pMOS transistors are off, so no current flows from V_DD to the output.
- **When either or both inputs are low (logic 0)**:
  - At least one pMOS transistor is on, connecting the output to V_DD, so the output becomes high (logic 1).
  - At least one nMOS transistor is off, breaking the path to ground.

TOPIC NAME : DAY TIME DATE

CMOS NOR



A	B	Q_1	Q_2	Q_3	Q_4	V_{out}
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

Q_1, Q_2 - PMOS (on = 0)

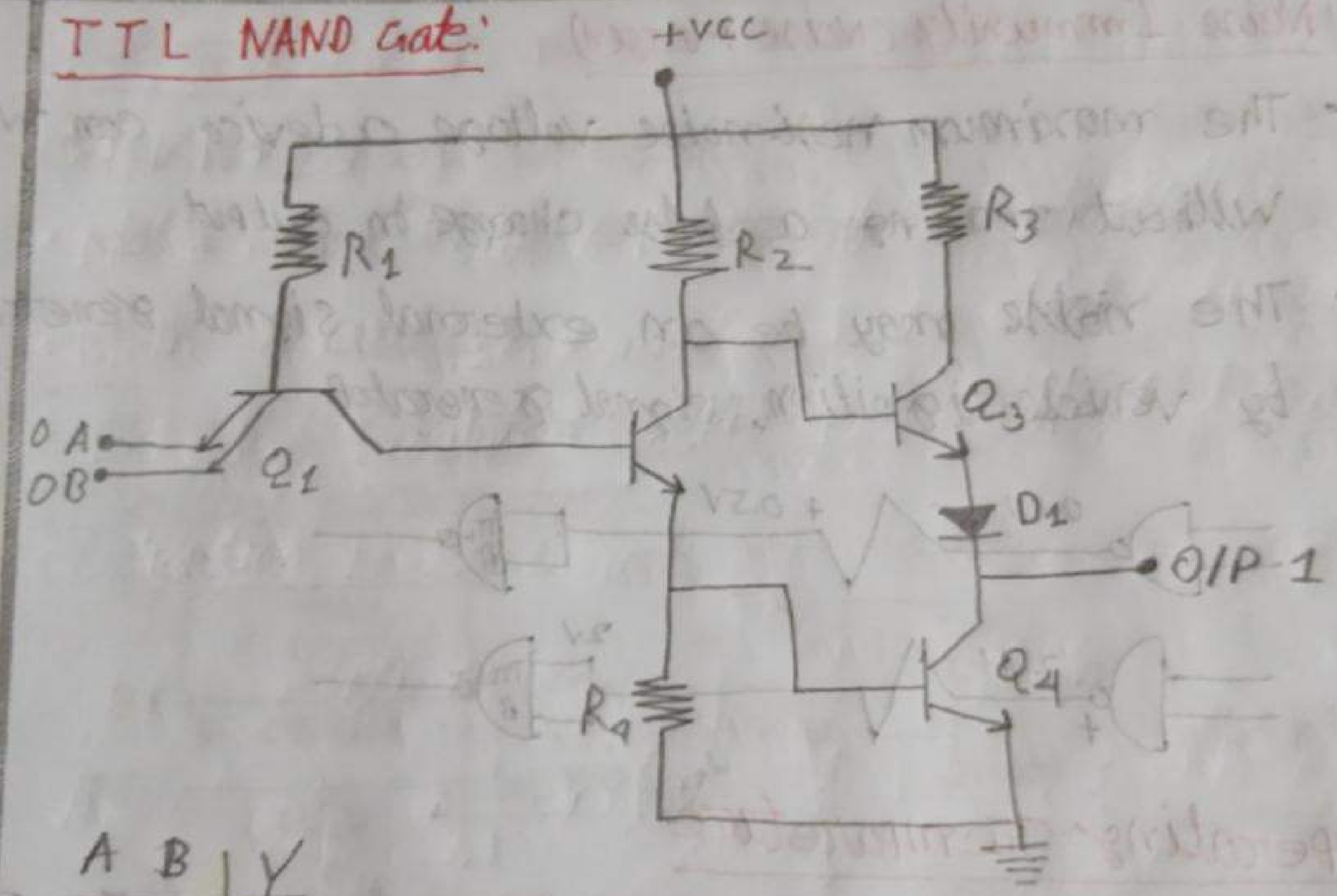
Q_3, Q_4 = NMOS (on = 1)

Working Principle:

- **When both inputs (A and B) are low (logic 0)**:
  - Both pMOS transistors conduct, creating a direct path from V_DD to the output, pulling it to high (logic 1).
  - Both nMOS transistors are off, so no current flows to ground.
- **When either or both inputs are high (logic 1)**:
  - At least one nMOS transistor conducts, creating a path to ground, so the output is pulled low (logic 0).
  - At least one pMOS transistor is off, breaking the path to V_DD.

b)

TTL NAND Gate:

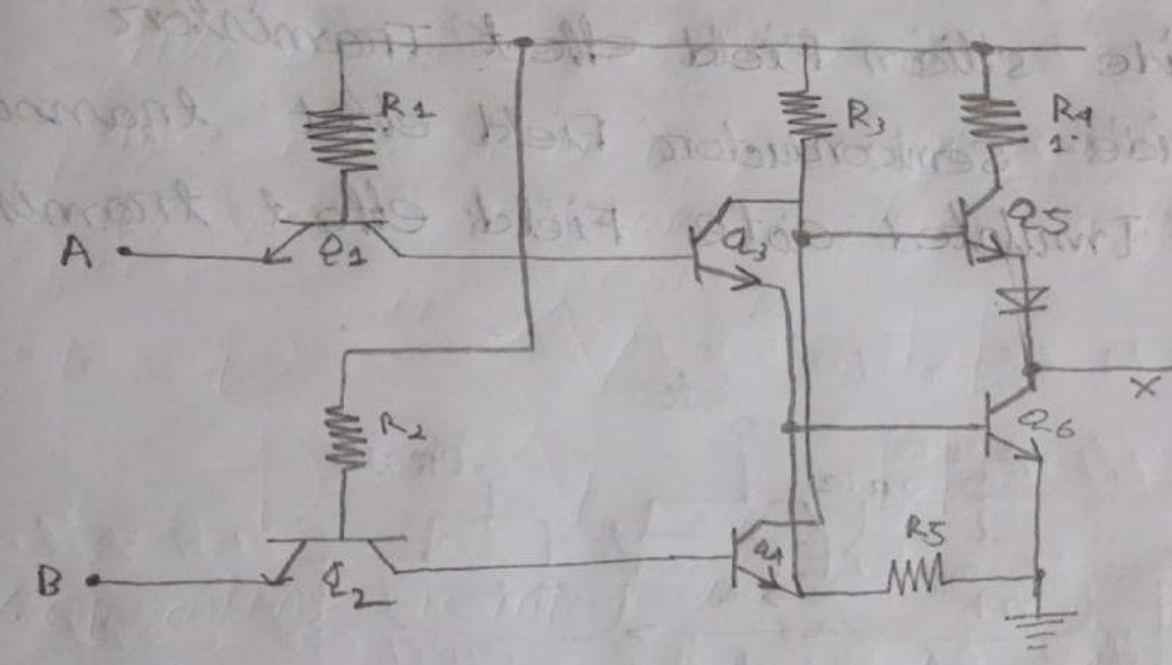


A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

TOPIC NAME : _____ DAY : _____

TIME : DATE : / /

TTL NOR Gate:



Q_5 = ON = output = High (1)

Q_6 = ON = output = Low (0)

A	B	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Y
0	0	ON	ON	OFF	OFF	ON	OFF	1
0	1	ON	OFF	OFF	ON	OFF	ON	0
1	0	OFF	ON	ON	OFF	OFF	ON	0
1	1	OFF	OFF	ON	ON	OFF	ON	0

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এটা Apply করা হেতে পারে NAND গেট মতো বসে

c)

TTL (Transistor-Transistor Logic) and CMOS (Complementary Metal-Oxide-Semiconductor) logic gates differ mainly in power usage, speed, and noise resistance. TTL has higher power consumption and faster switching but limited noise immunity and fan-out. CMOS uses less power, has higher noise immunity, and can work over a wider voltage range, making it ideal for battery-powered and complex digital circuits.

Characteristic	TTL	CMOS
Power Consumption	High	Low
Switching Speed	Fast	Initially slower but now fast
Fan-Out Capability	Limited (~10)	High
Noise Immunity	Lower	Higher
Input Impedance	Low	Very High
Supply Voltage Range	Typically 5V	3V-15V (varies)
Cost	Higher for high density	Lower, scalable
Temperature Stability	Moderate	Better due to low power

↳ প্রশ্নগুলো mandatory না সে বাড়ী মনে থাকে লেখবি