Chapter 7

counter:-

A counter is a device which stores (displays) the number of timer particular event or process has occurred, often in relationship to a clock signal.

- It is design by flip-flop (J-K)
- The main properties of counter are timing, sequencing and counting.
- counter works on two mood
  - → up counter
  - → down counter
- counter two categories
  - → Asynchronous counter (Ripple counter)
  - → synchronous counter

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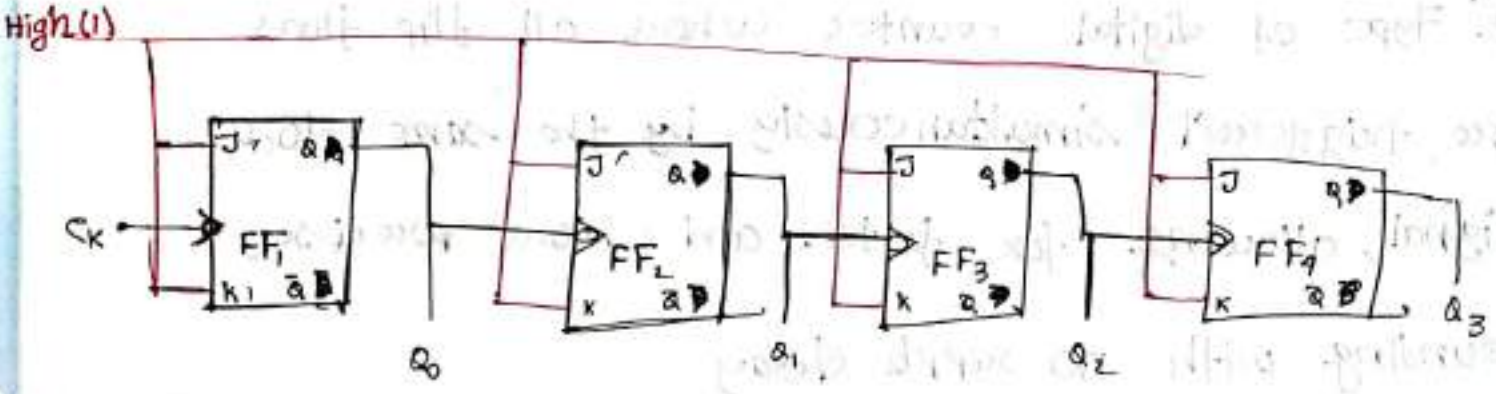
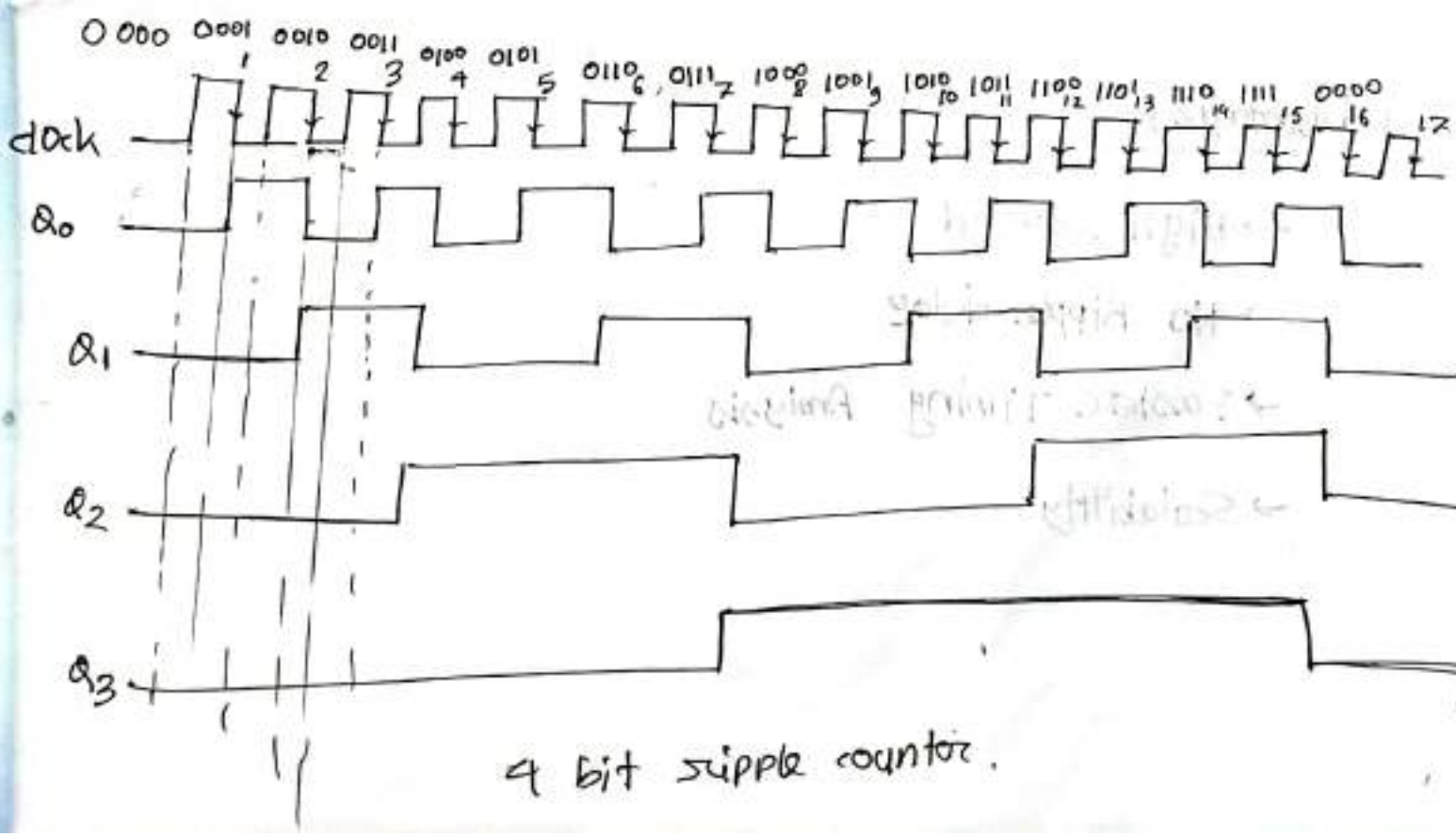
⊛ Asynchronous (Ripple) counter

In Asynchronous counter we don't use universal clock. only first flip flop is driven by main clock and the clock input of rest of the following flip flop is driven by output of previous flip flops. We can understand it by following diagram-





4 bit ripple counter.

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Definition :- An asynchronous counter is a type of digital counter where the each flip flop is triggered by the output of the previous one. It is also ripple counter.

Synchronous (parallel) counter : A synchronous counter is type of digital counter where all flip flops are triggered simultaneously by the same clock signal, allowing for faster and more precise counting with no ripple delay

advantages

- → High speed
- → No Ripple delay
- → Easier Timing Analysis
- → Scalability

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disadvantages

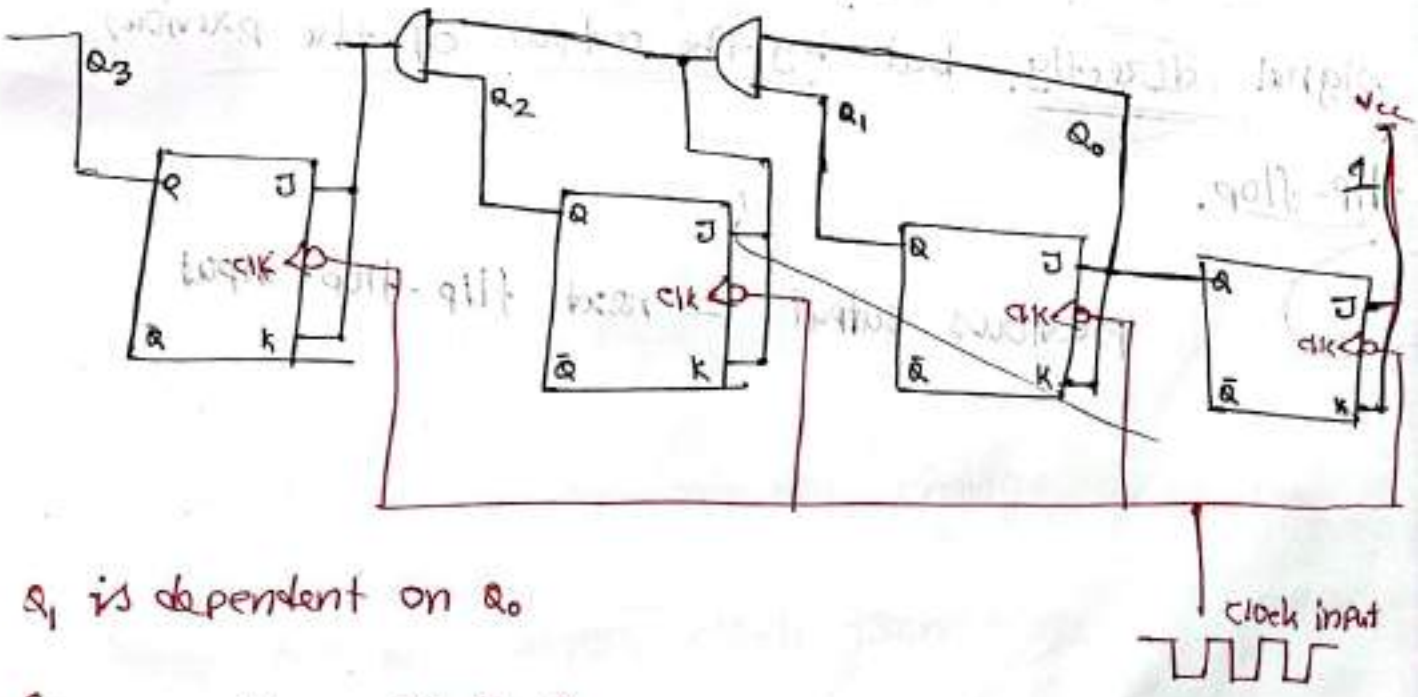
→ complexity

→ Higer cost

→ Larger circuit size

(ii) Functionality

Synchronous counter has one global clock which drives each flip-flop so ouput changes in parallel.



Q_1 is dependent on Q_0

Q_2 " " on Q_0, Q_1

Q_3 " " on Q_0, Q_1 and Q_2

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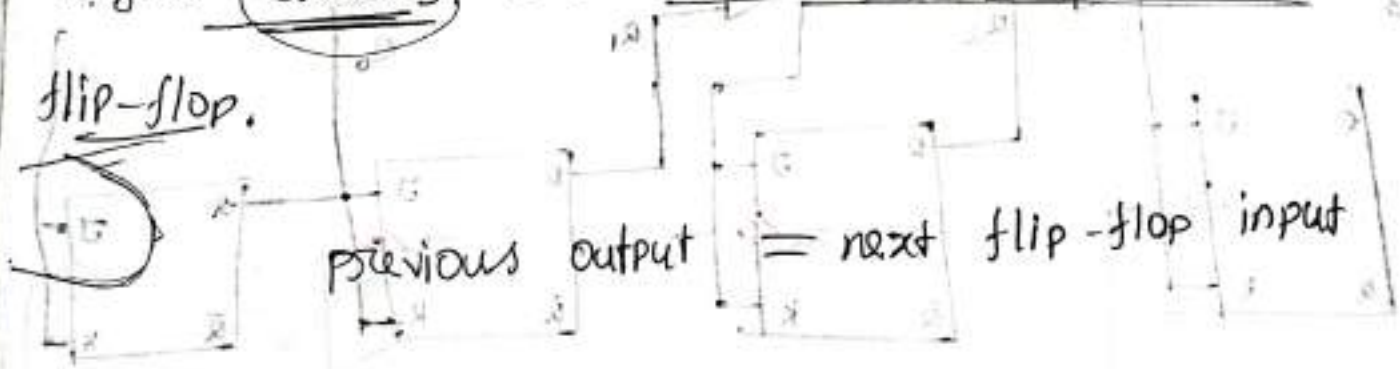
Timing diagram is same as asynchronous

⊛ Propagation Delay in Ripple counters

It refers to the time it takes for a change in the input (clock pulse) to be reflected in the output of the counter.

This delay occurs because, in a ripple counter, each flip flop is triggered not by the clock signal directly but by the output of the previous flip-flop.



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each flip-flop triggered by the output of the preceding flip-flop.

→ Because of inherent propagation delay time (t_d) of each flip-flop

this means the 2nd FF_2 will not respond untill a time t_{pd} after the FF_1 active

the FF_3 will not respond untill time equl $2t_{pd}$ after the clock transition.

Overall The propagation delays of the FF accumulate so that N th Flip Flop can not change until time equal $N \times t_{pd}$ after clock transition.

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max. frequency

$$f_{max} = \frac{1}{N\, t_{pd}}$$

t_{pd} = propagation delay

N ← number of FF

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MOD number

It represents the total count of distinct output values the counter can produce.

⇒ A counter with mod number of N will count 0 to N-1 before resetting back to 0.

→ example 3 bit binary counter has MOD number is $2^3 = 8$, it counts through 8 states 0 to 7,

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Synchronous

(i) The operation is faster

(ii) It is also known as parallel counter

(iv) less error

(vi) Desigen is complex

Asychronous

(i) The operation is lower

(ii) It is also known as ripple counter

(iv) more error

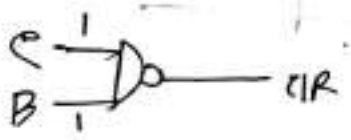
(vi) Desigen is simple

(*) counter with mod numbers $< 2^n$

Stat mod 6 counter

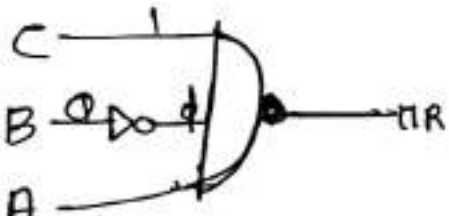
6 9 21

mod 6



count	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

mod 5



	D	C	B	A	
8	1	0	0	0	
9	1	0	0	1	

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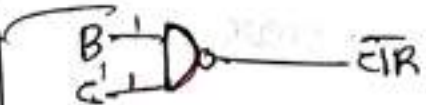
$2^4 = 16$

count	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16				

mod 6 → Temp state



mod → 10 Temp state

mod (13)

mod 14 → Temp state

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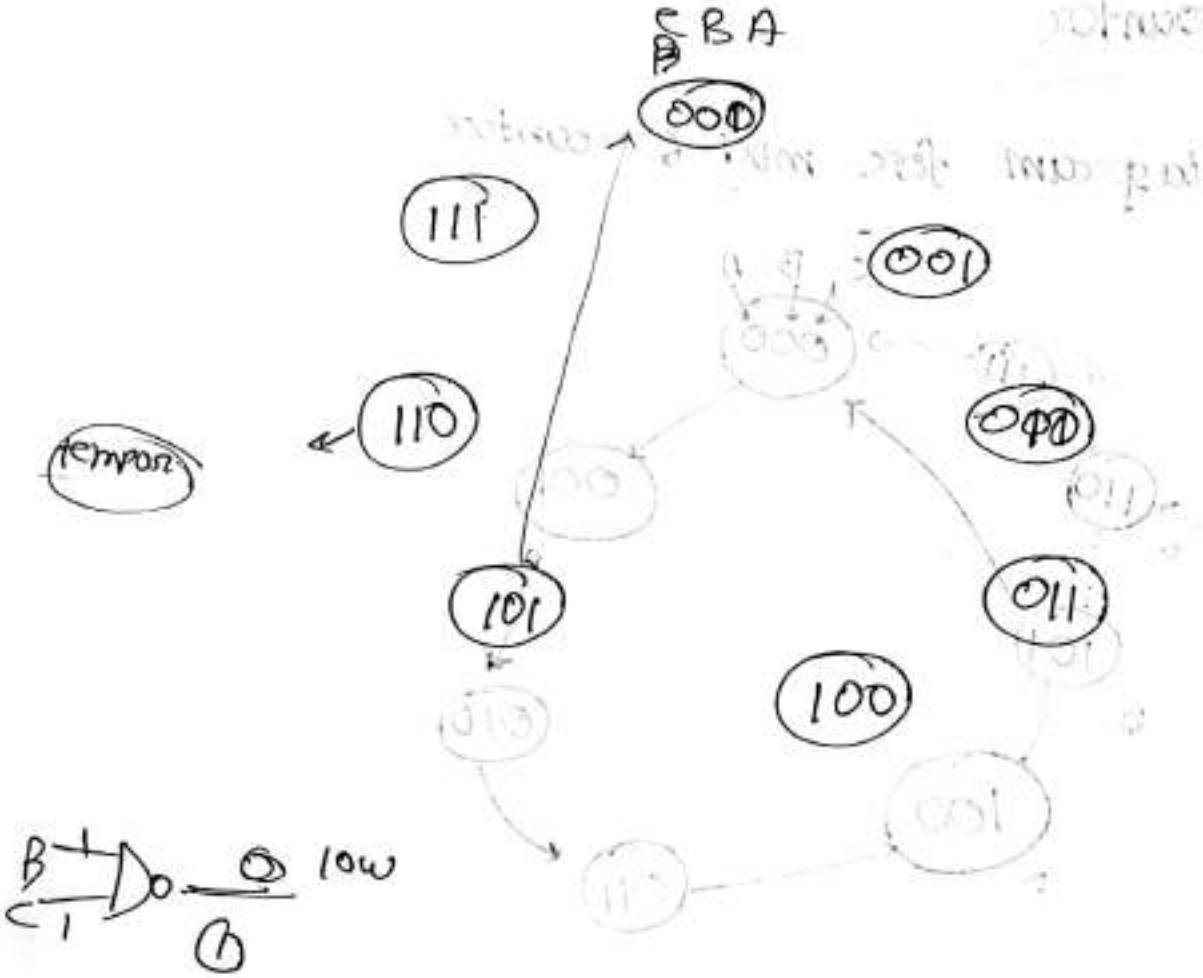

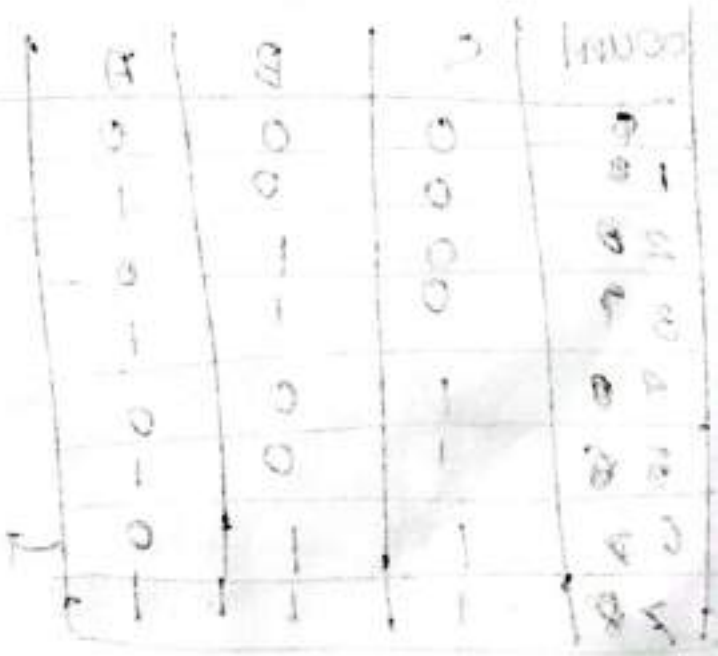

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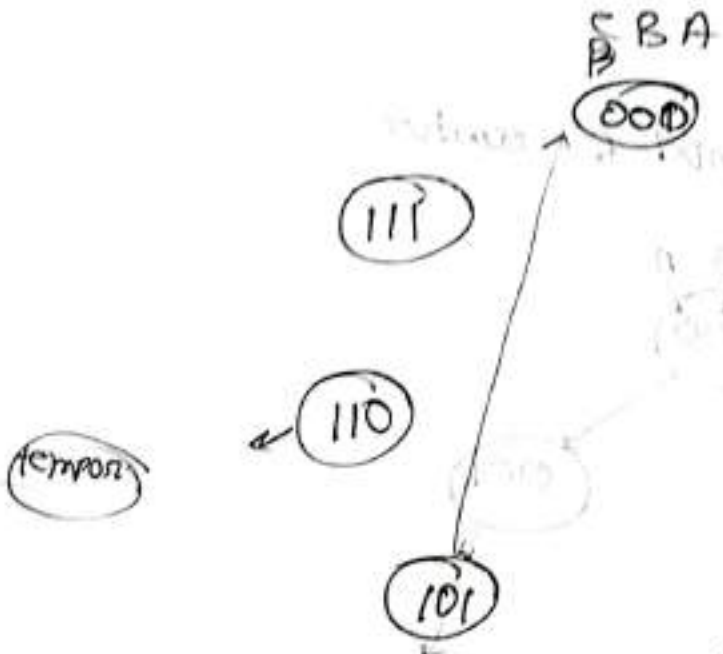

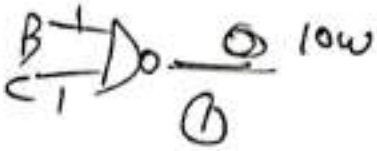

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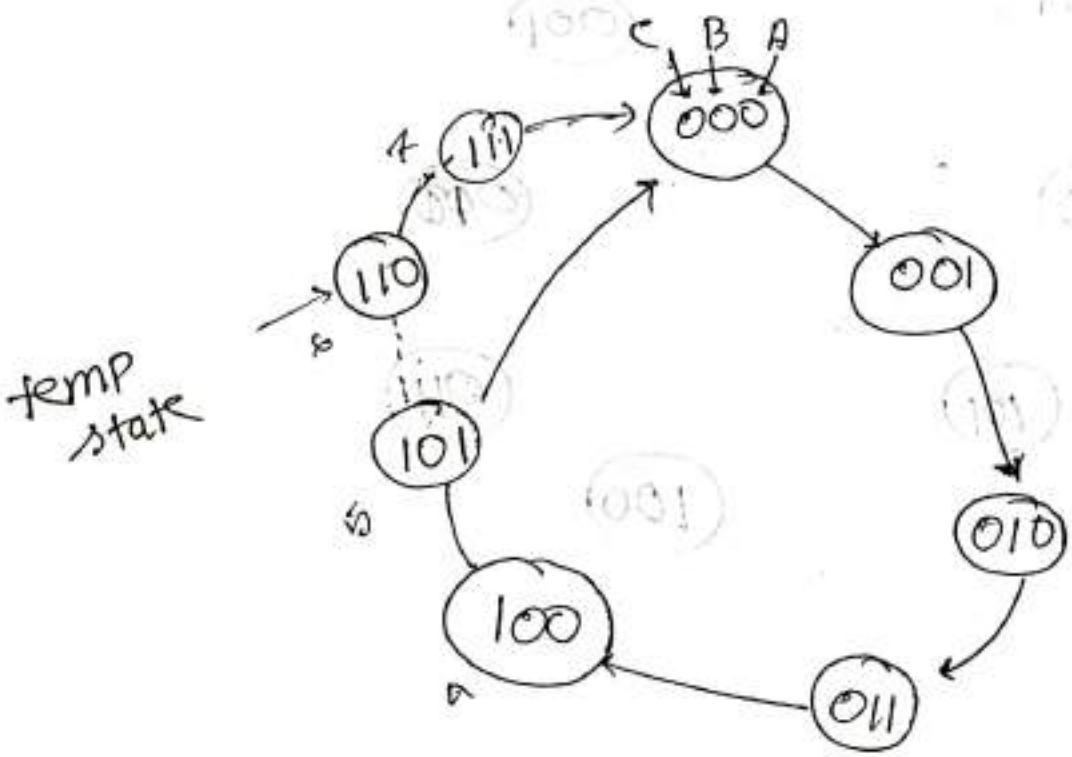
MOD 6 counter

Stat diagram for mod 6 counter



count	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

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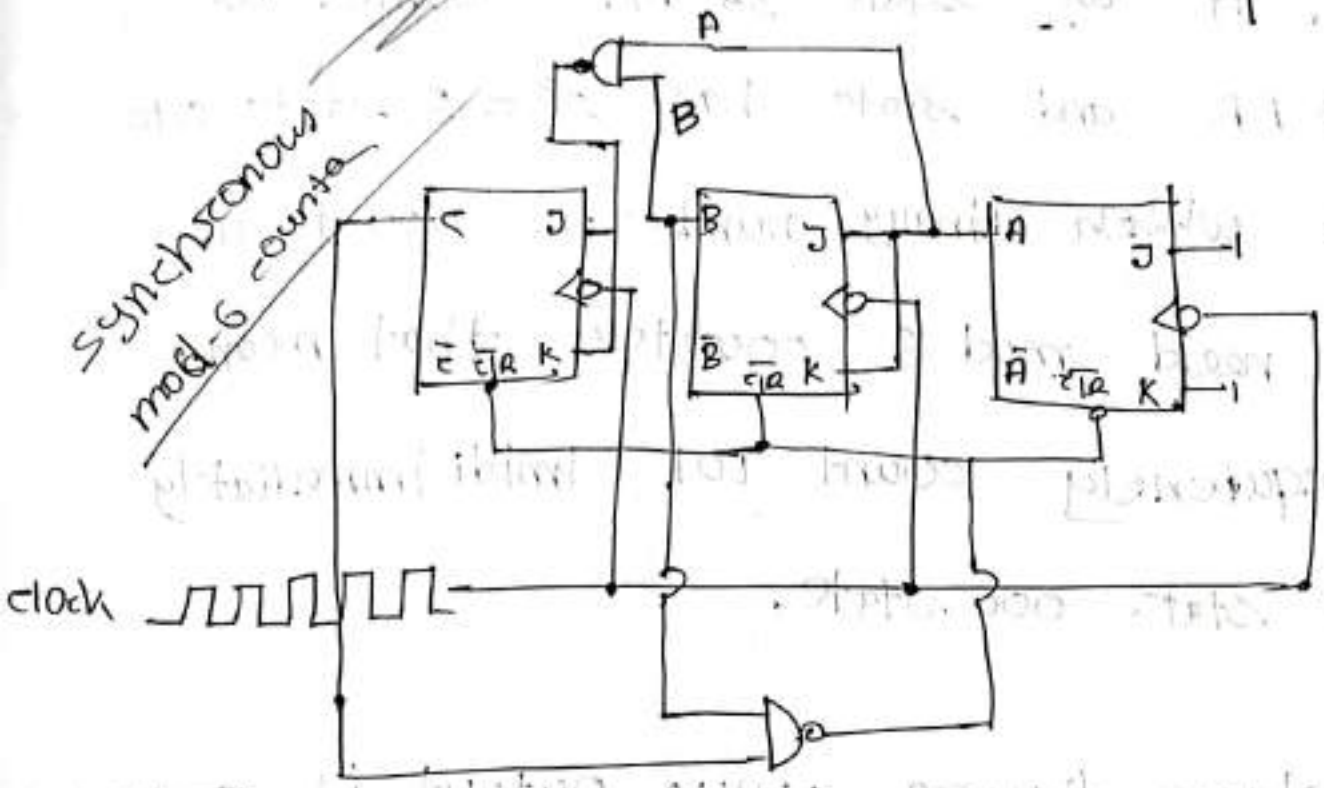
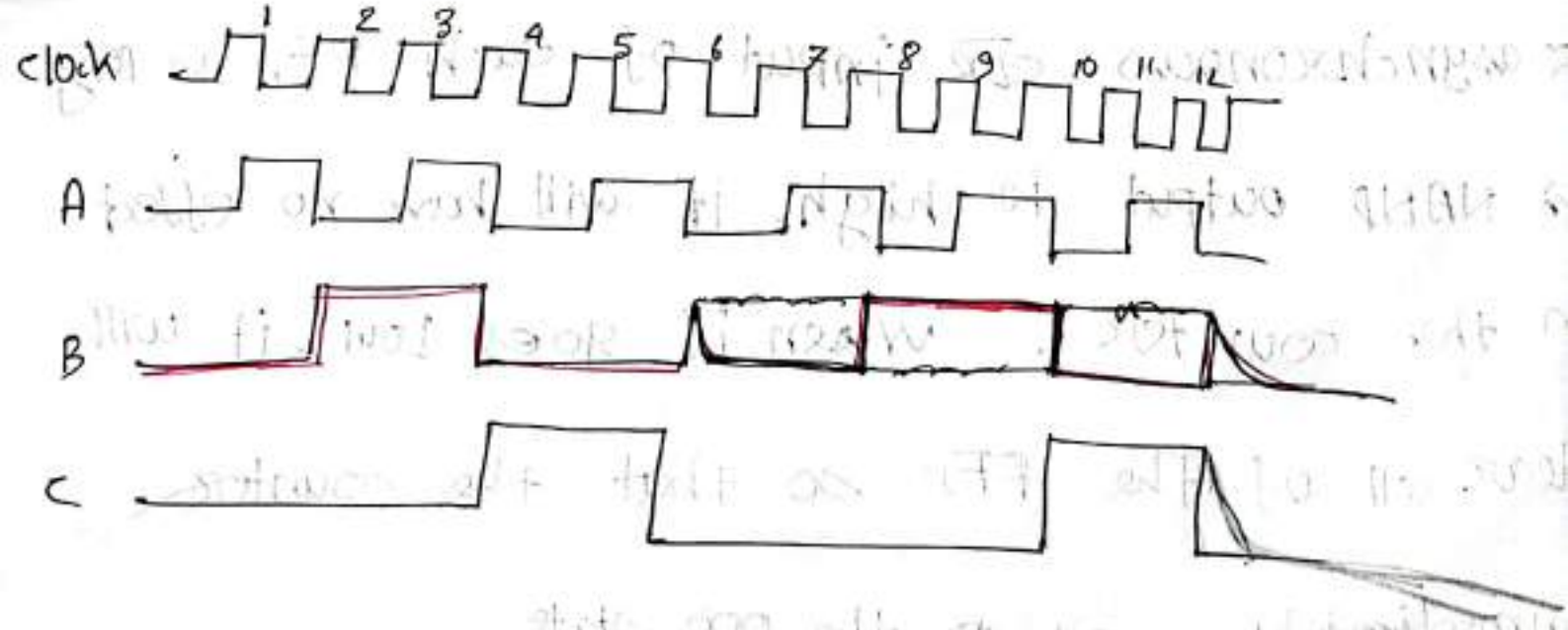
Synchronous mod-6 counter





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The basic counter has 2^N ~~whe~~ state whe N is FF. if we ~~state~~ build 3 bit counter we need 3 FFs and state has $2^3 = 8$ state 0 to 7 decimal which binary number is 000 to 111. But we need mod 6 counter that means after sequenely count 101. ~~imidi~~ immediakly goes to stat 000 state.

In the above figure NAND output is connecte ~~as~~ asynchronous $\overline{CLR}$ input of each FF. As long as NAND output is high, it will have no effect on the counter. When it goes low, it will clear all of the FFs so that the counter immediately goes to the 000 state.

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The input of NAND gate is outputs of FF B and C.

so NAND gate output is low whenever B=C=1.

This condition is occure when the counter goes ~~to the~~ from 101 state to the 110 state.

The the NAND ~~out~~ LOW output clear to the counter and immediately (within few sec) goes to the 000 state. This 110 state in counter is called temporary state it's needed to clear counter.

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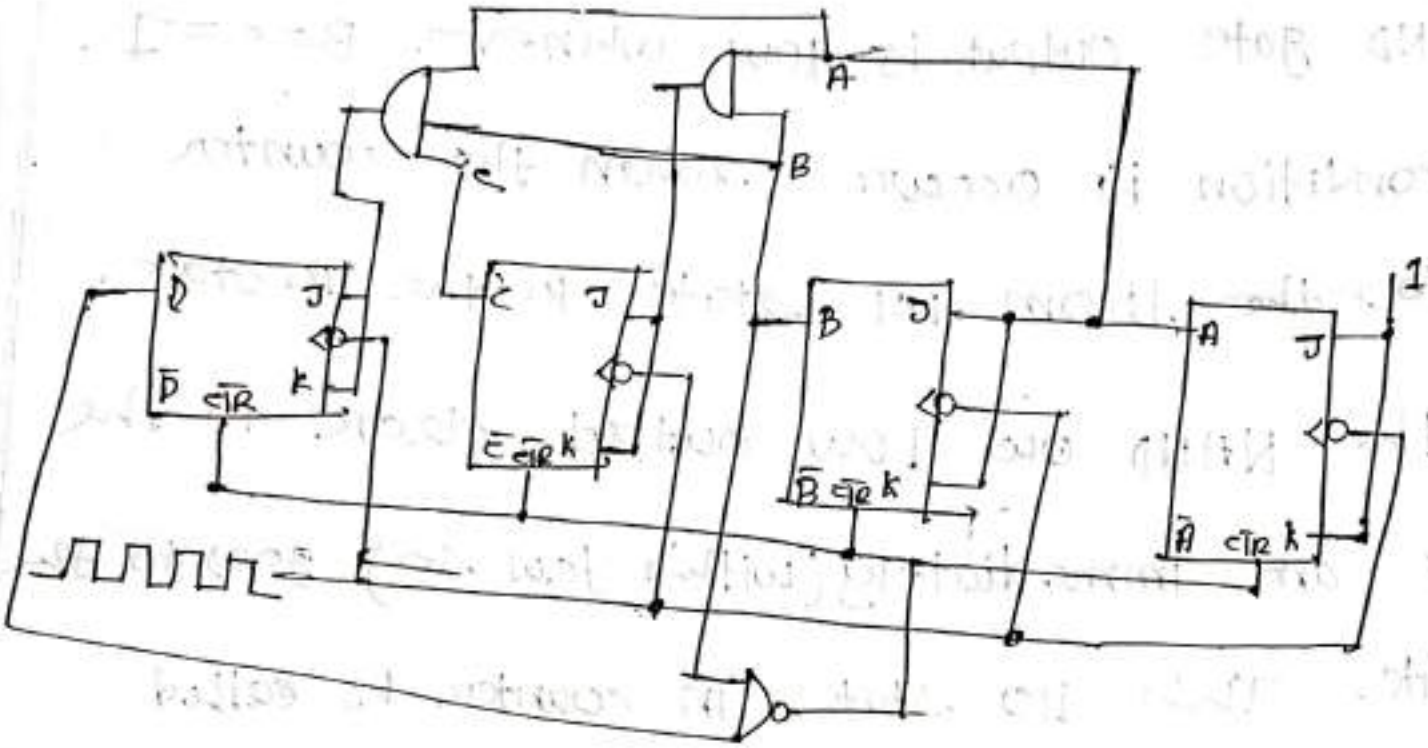
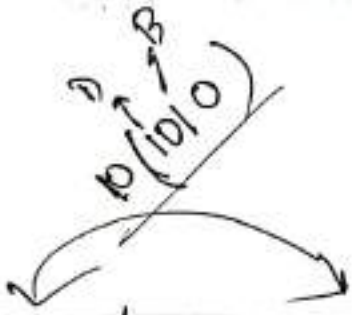
⊛ MOD (10) Decade counter.





count	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0

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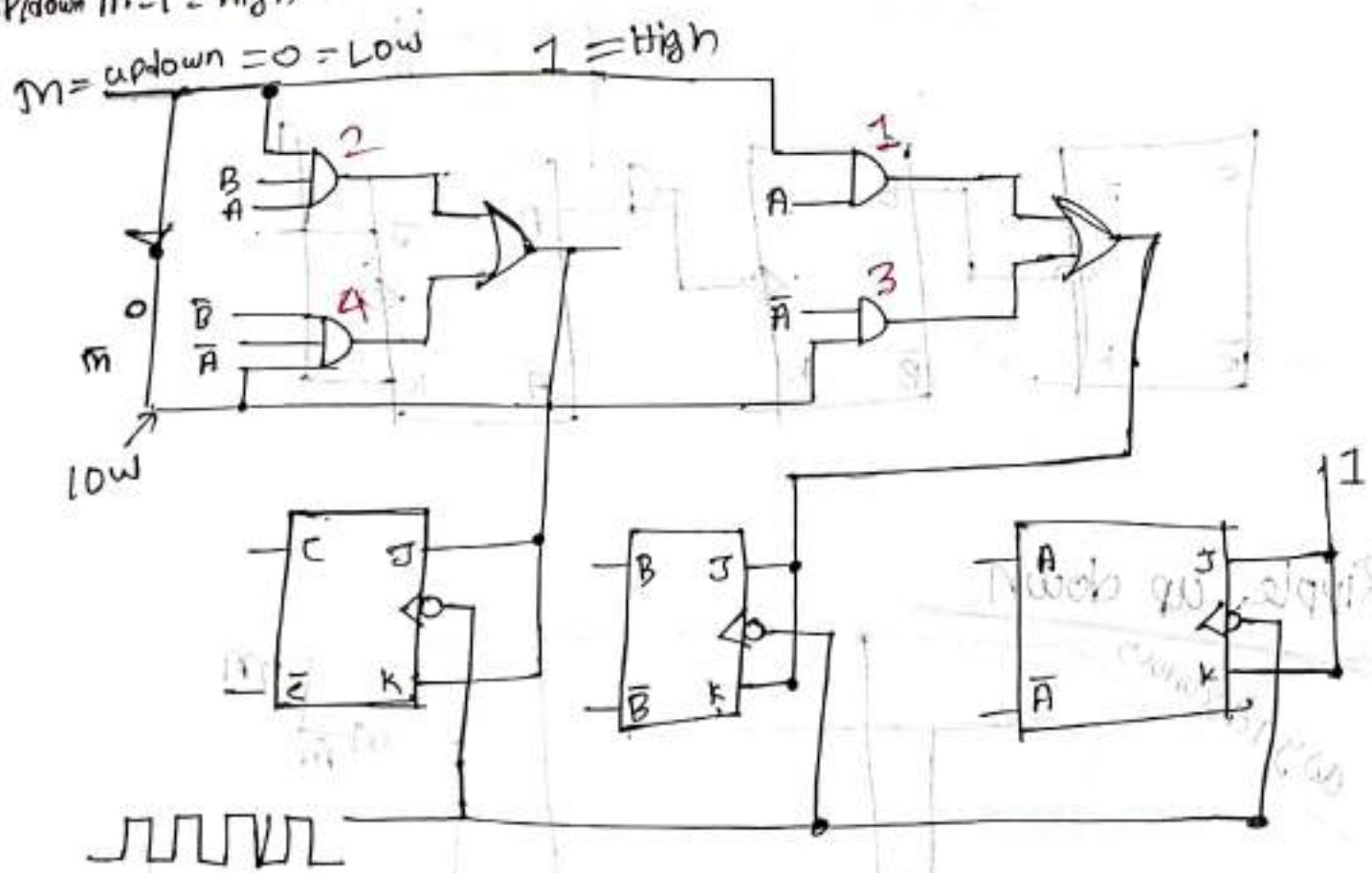
- updown m=1 = High



if updown is high.

→ AND gate 1, 2 enable and 3, 4 gate are disable.

→ This allows A and B outputs gates 1 and 2 control the J and K inputs of FFs B and C

→

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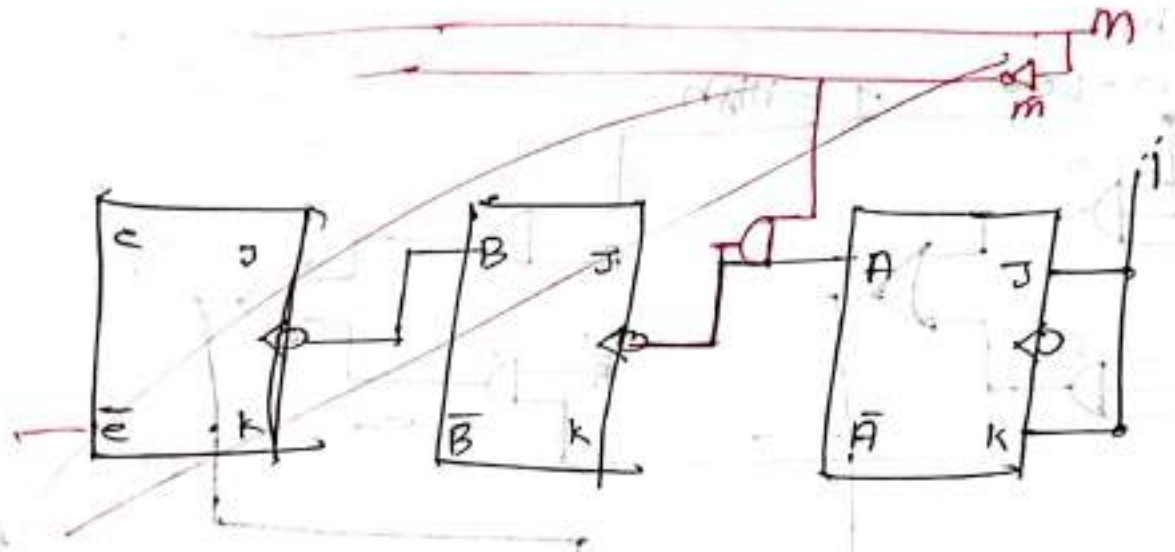
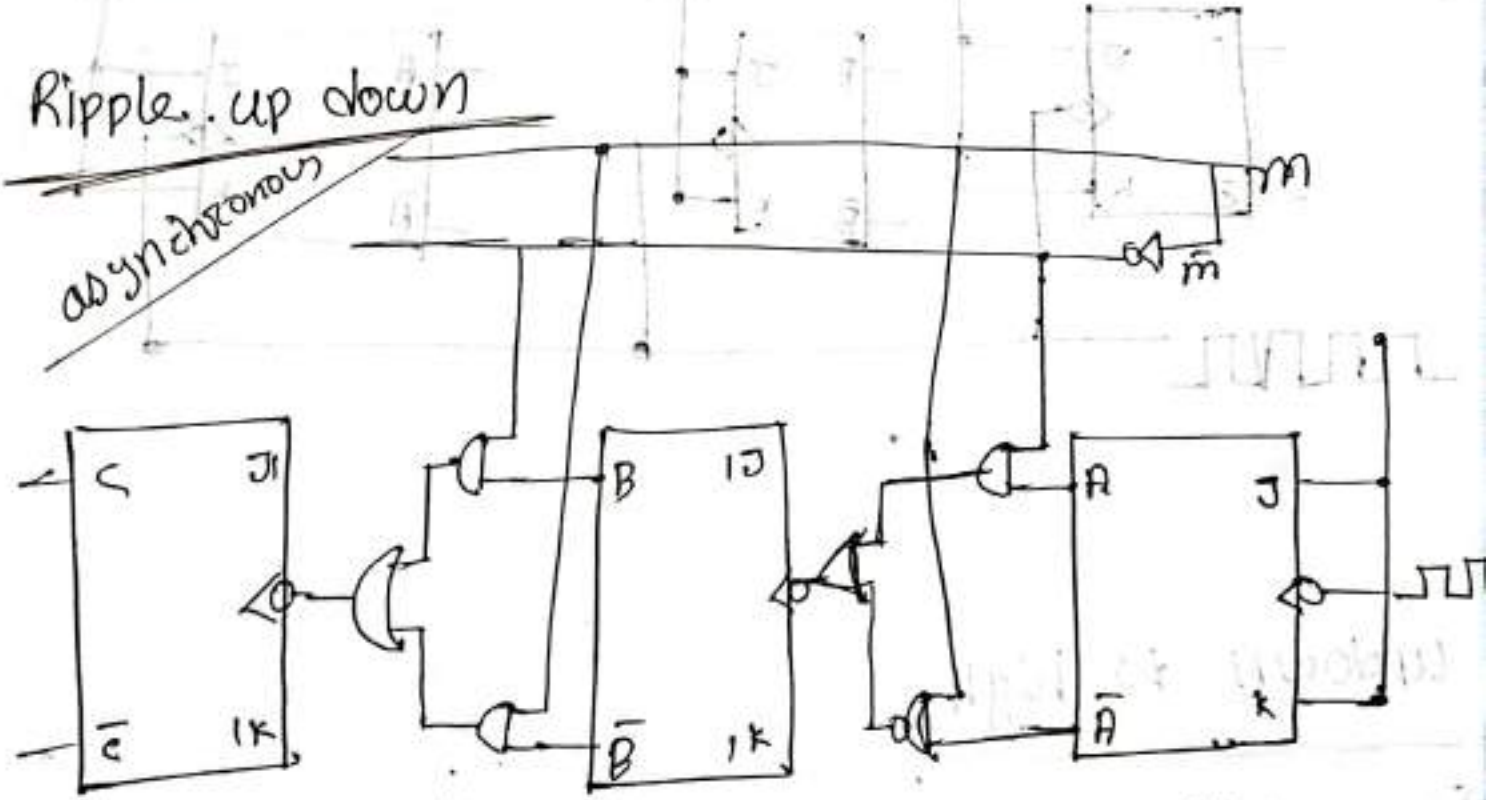


Ripple up down

asynchronous



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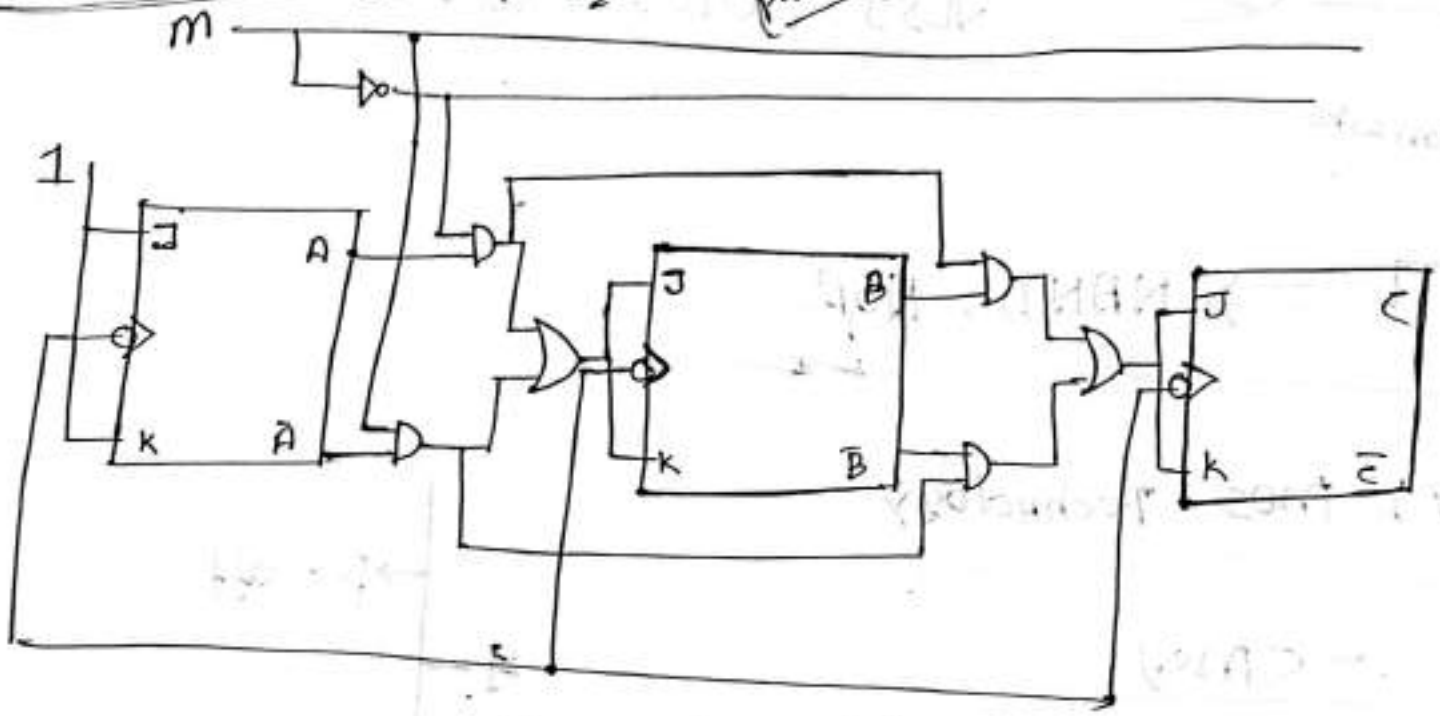
Synchronous up down

parallel



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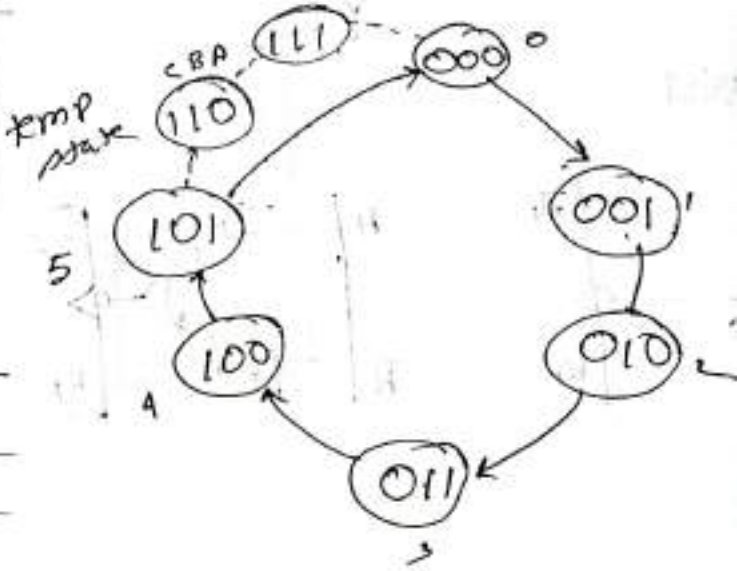
MOD-6 Asynchronous (Ripple) counter

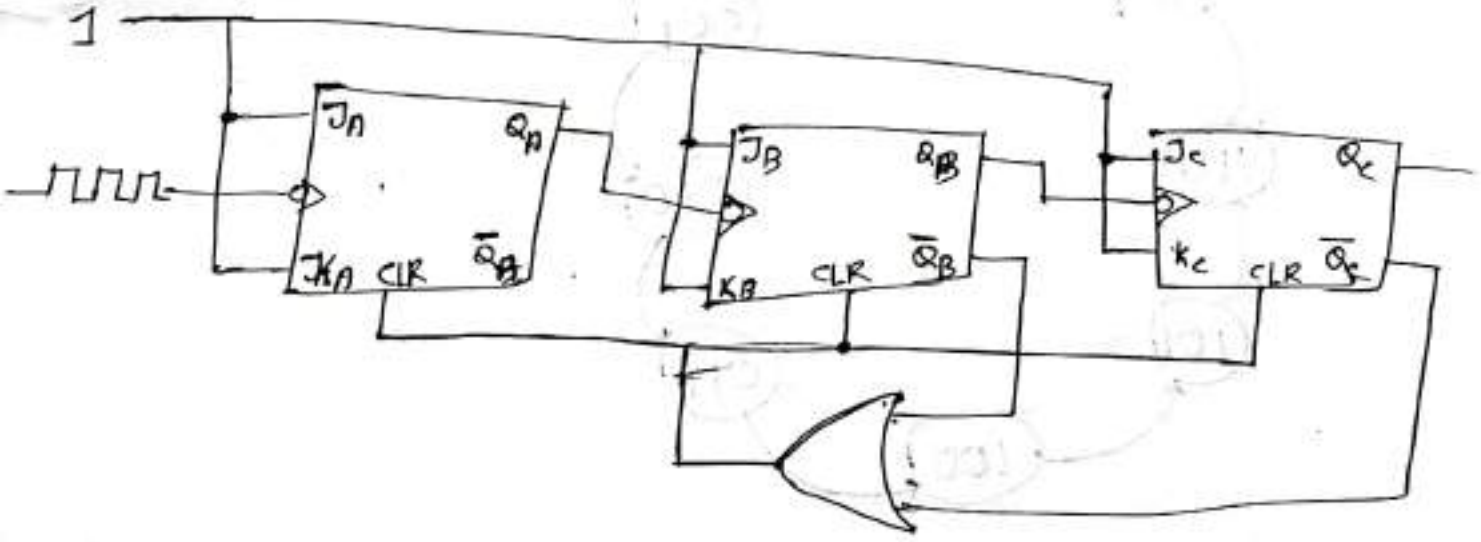
count	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

mod 6 →

temp state



A B C



Same as another counter.

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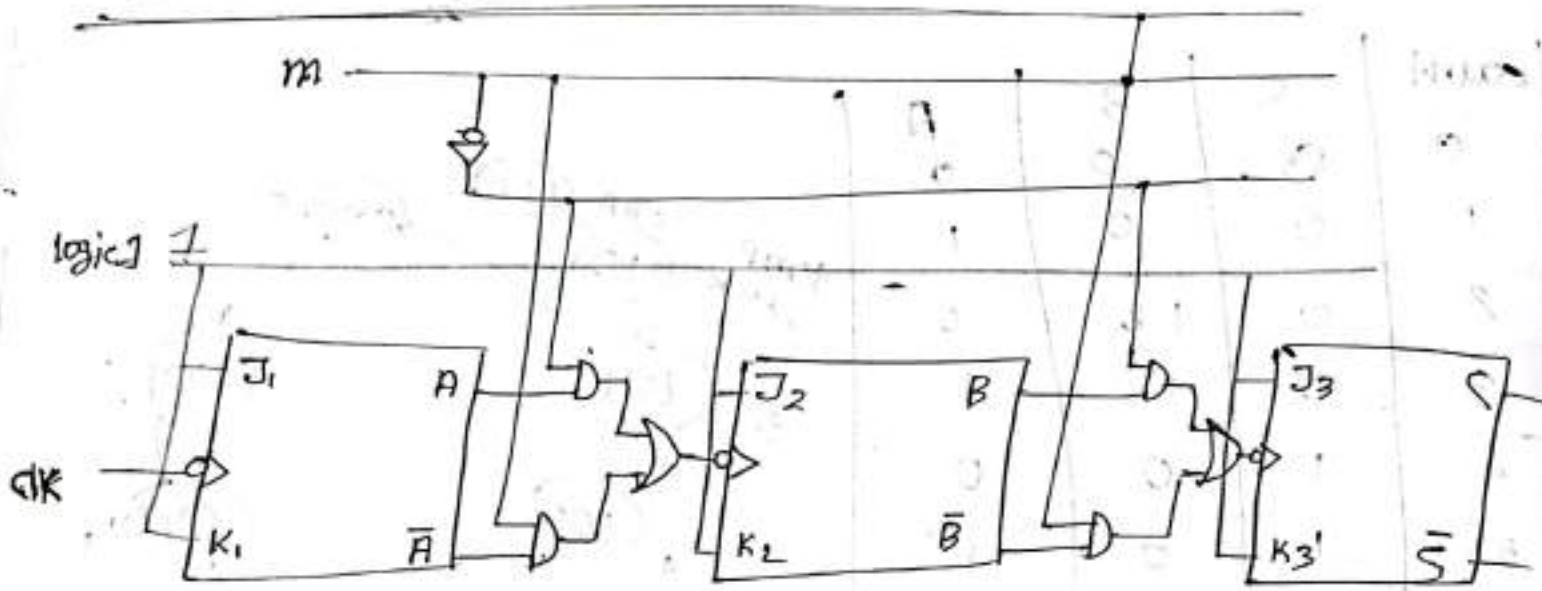
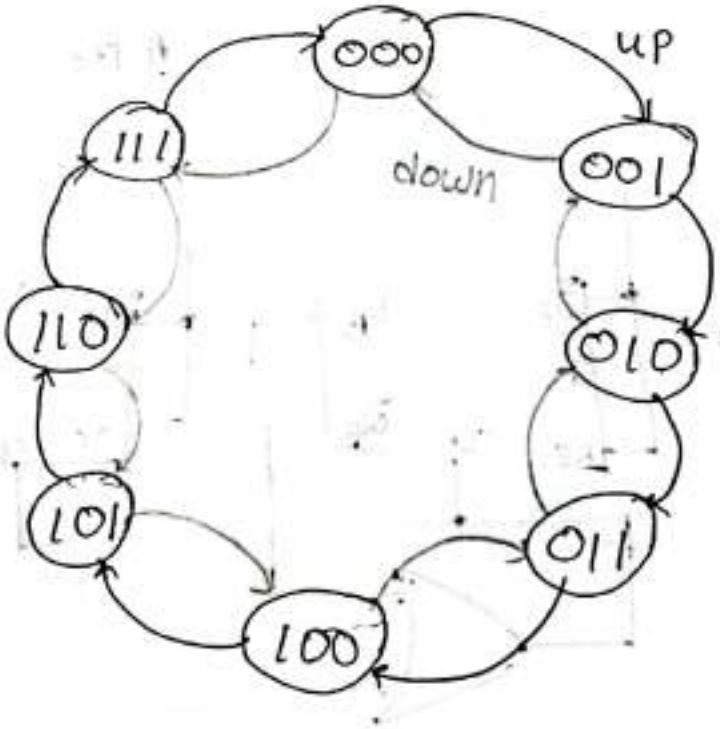
Synchronous ~~Ripple~~ up/down counter





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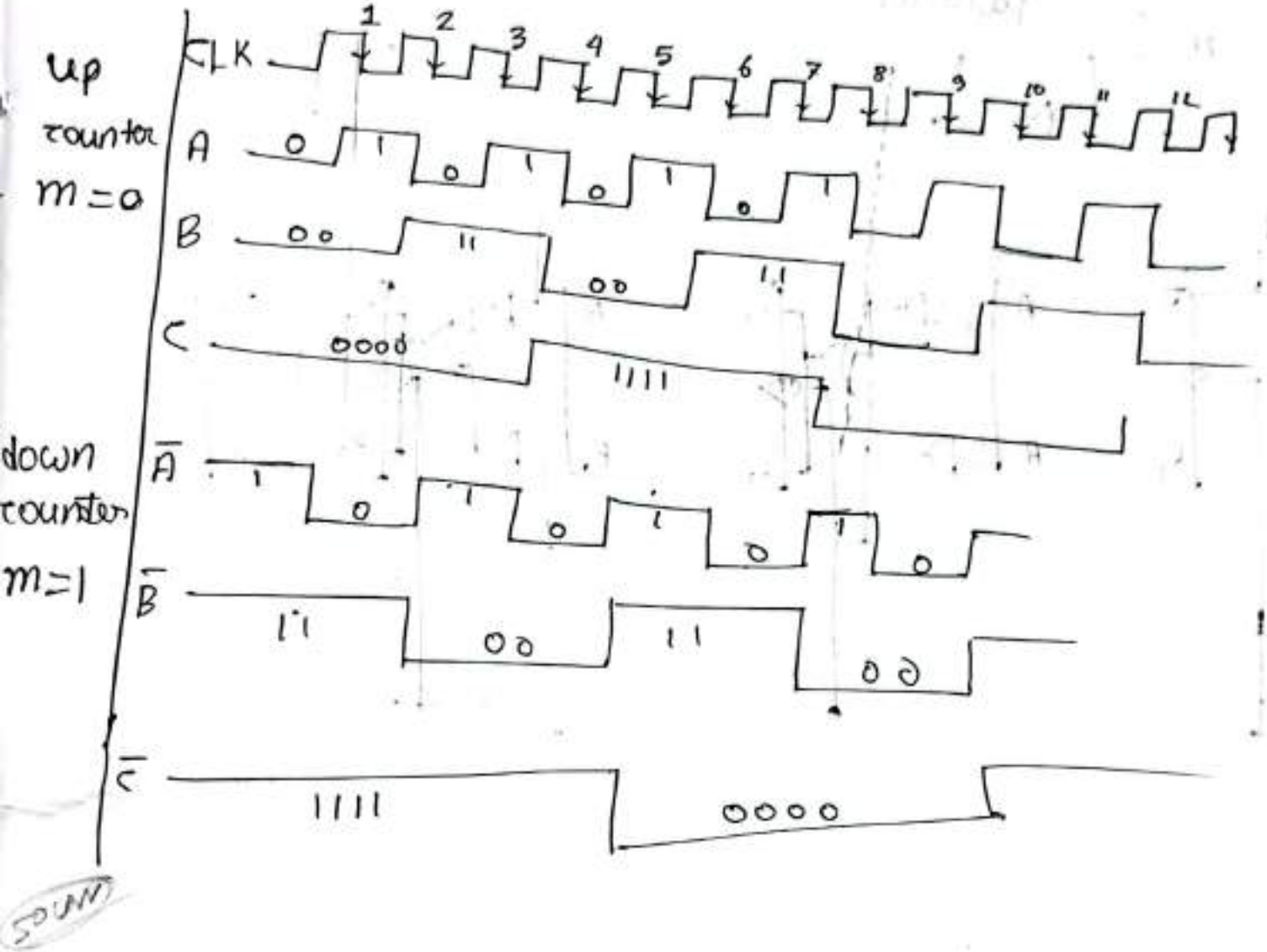
Timing diagram



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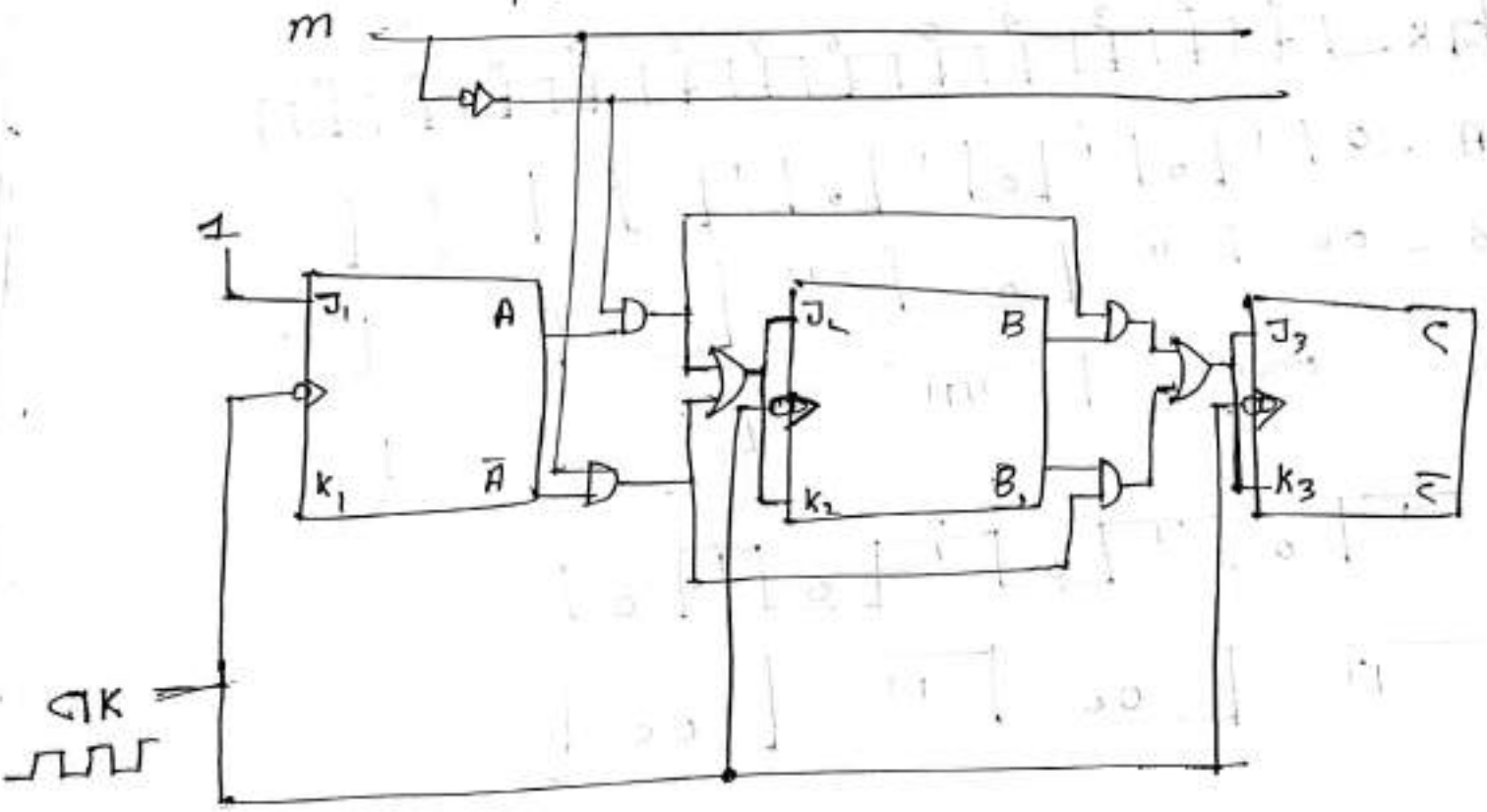
: synchronous / up and down counter

parallel



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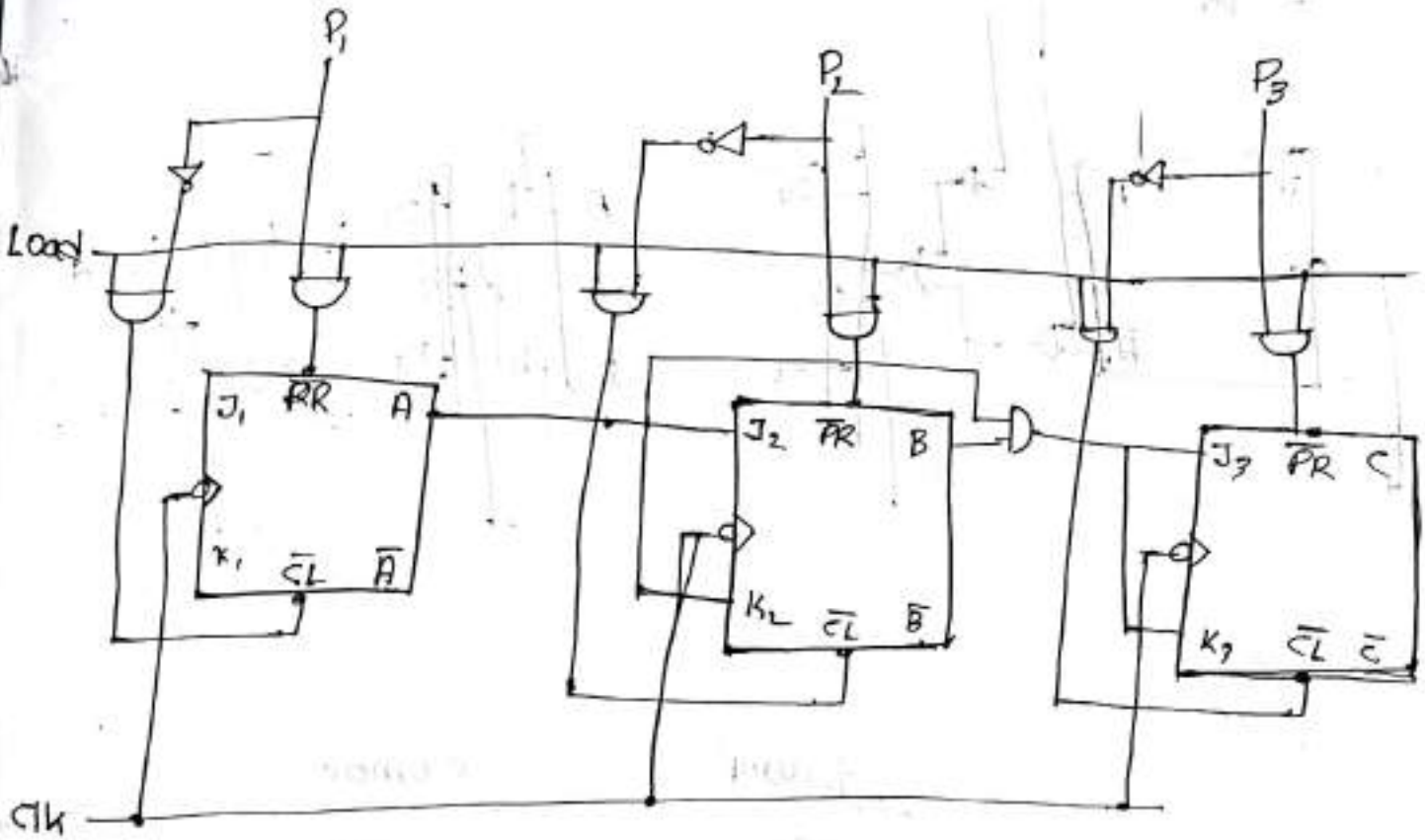
Presettable counter



Synchronous counter with asynchronous parallel load

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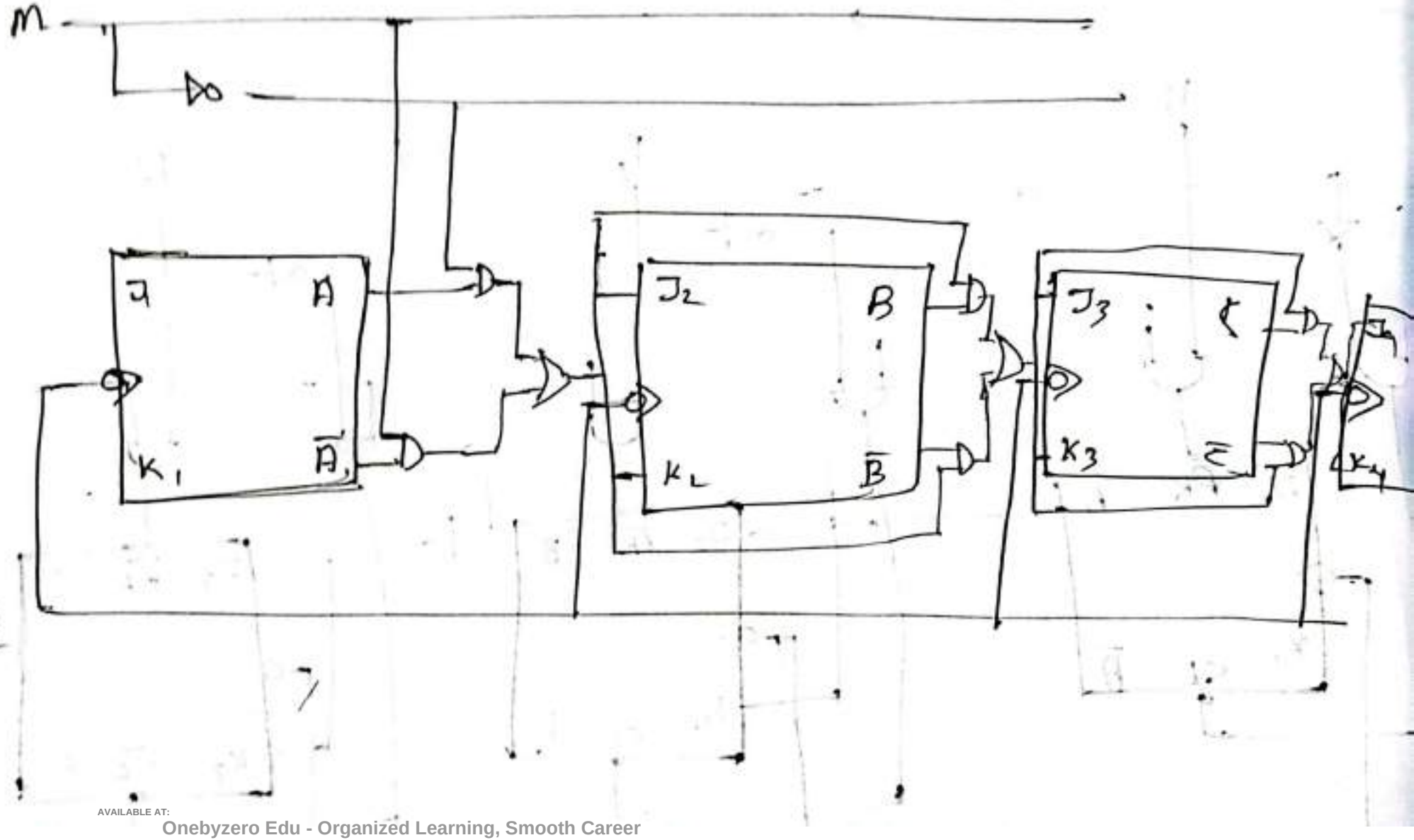
Synchronous up/down mod 16 counter:—



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Explain the working principle of a Synchronous up down Mod-8 counter with appropriate diagram.

A Synchronous up/down Mod-8 counter counts in both up and down directions based on a control signal. Here is an explanation of its working principle:

Control Signal (Up/down): This determines the direction of counting. When the control signal is HIGH (Up/down = 1) the counter counts up and when the control signal is LOW (Up/down = 0) the counter counts down.

AND (gates): It controls which signals (normal or inverted) are fed to the J and K inputs of the flip-flops (FFs).

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- When Up > Down = 1 : Normal outputs are fed through enabled AND gates, allowing upward counting.
- When Up > Down = 0 : Inverted outputs are fed through enabled AND gates, enabling downward counting.

State Transition: The counter moves between state on the negative edge of the clock pulse. The direction of the state transition is based on the control input.

Mod-8: Since it is a Mod-8 counter, it can count from 0 to 7 and then warps around.

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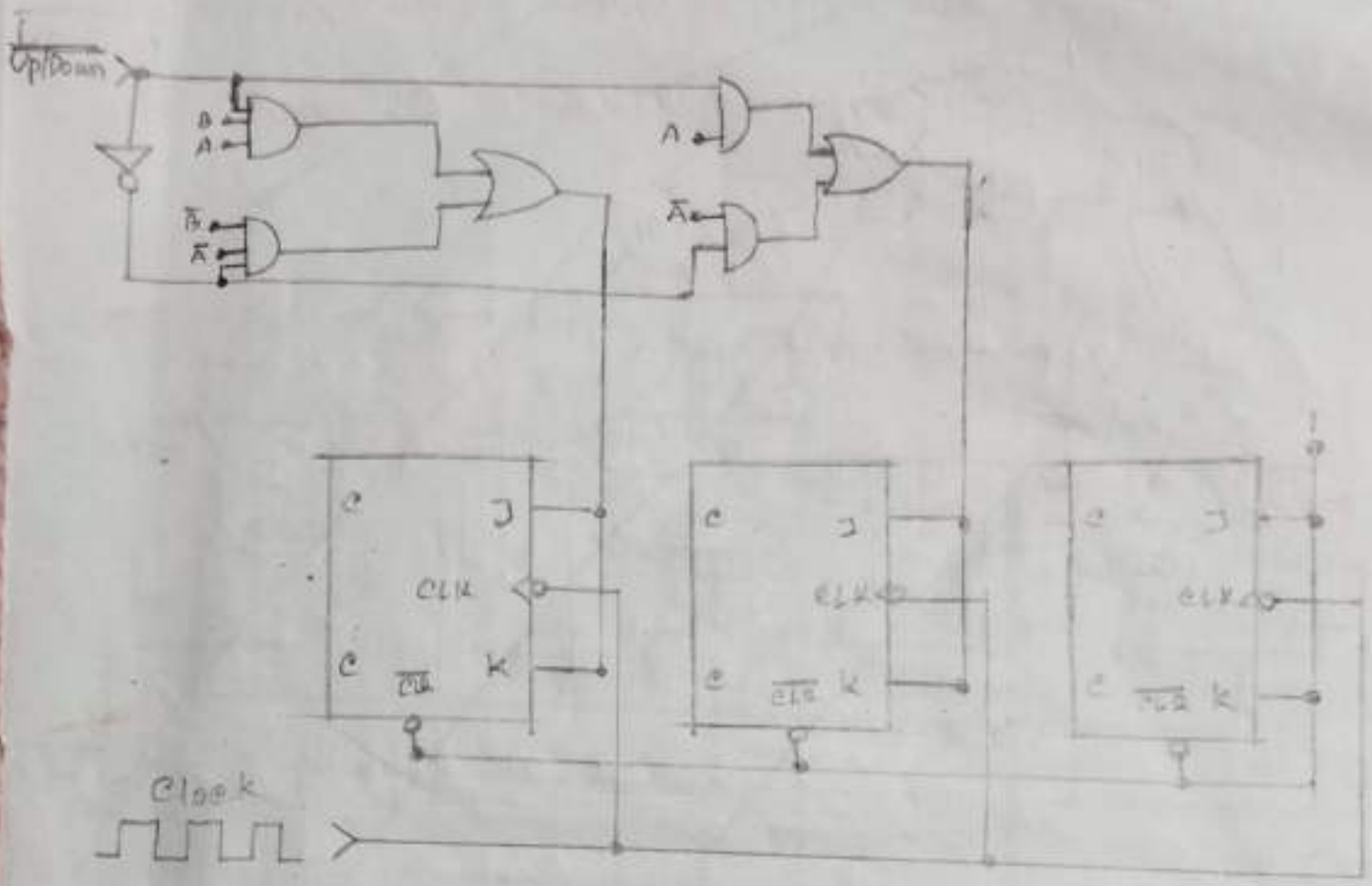
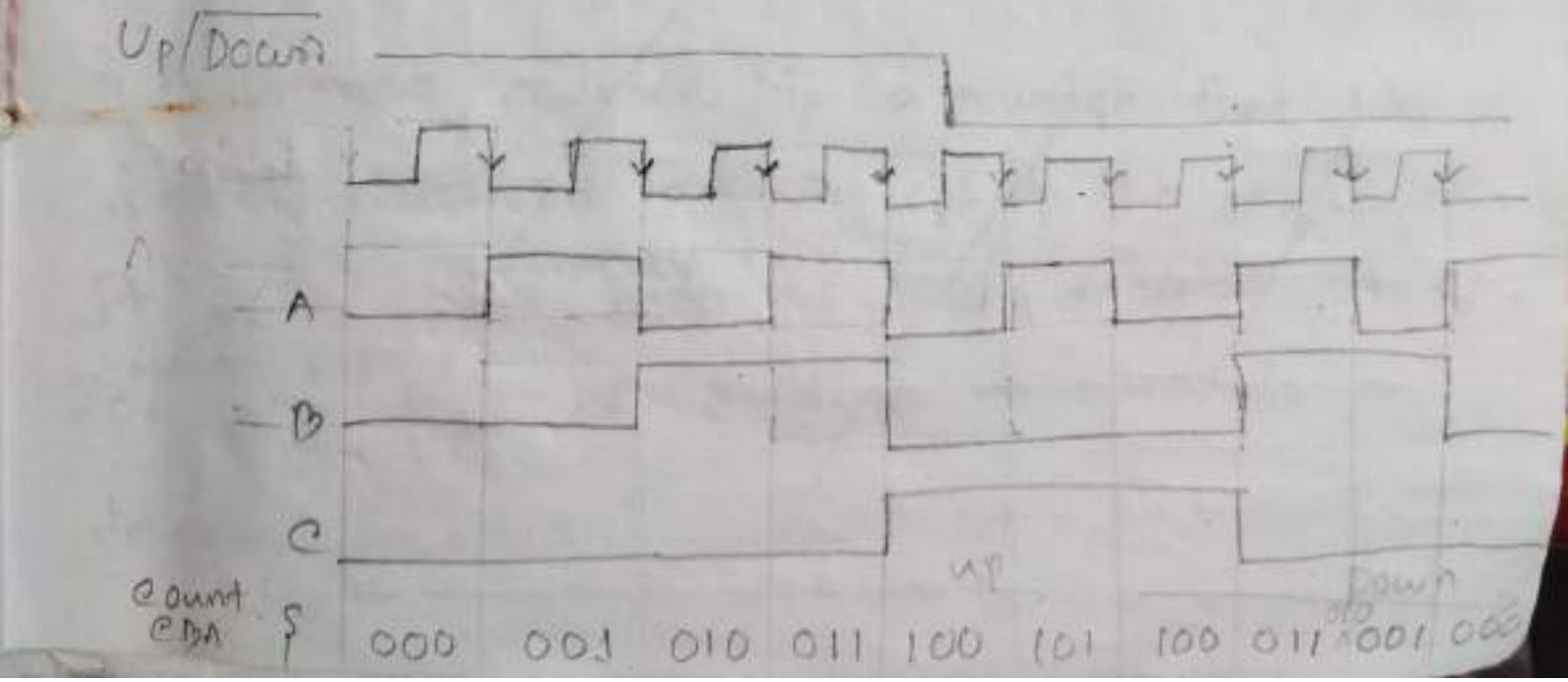


Fig: Schematic synchronous Mod-8 up/down counter



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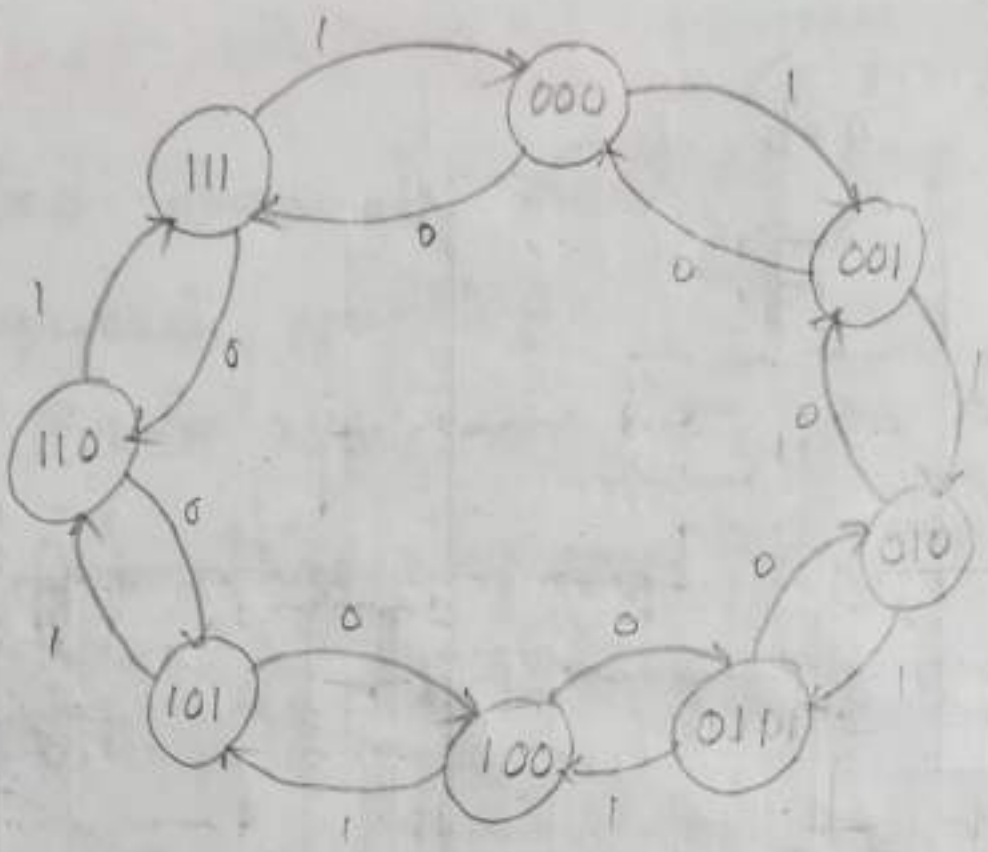

state diagram

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R_1 = Decentralization / hash

R_2 = Volatility / valuation

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[4]. Explain 3-bit/4-bit asynchronous (ripple) counter.

A 3-bit/4-bit asynchronous (ripple) counter operates using four flip flops (A, B, C, D) each represents one bit of a binary number. The D flip-flop is MSB and the A flip-flop is LSB.

3-bit counters can count 000 to 111 (decimal 0 to 7)
4-bit " " 0000 to 1111 " 0 to 15)

Cloking Mechanism:

① The clock pulses are applied only to flip-flop A. This toggles (change state) on every negative edge (HIGH to LOW transition) of the clock.

② Flip-flop A's output is the input for flip-flop B. and similarly B's output is input for C and C's output is input for D flip-flop.

③ Each subsequent flip-flop toggles when the previous goes from 1 to 0.

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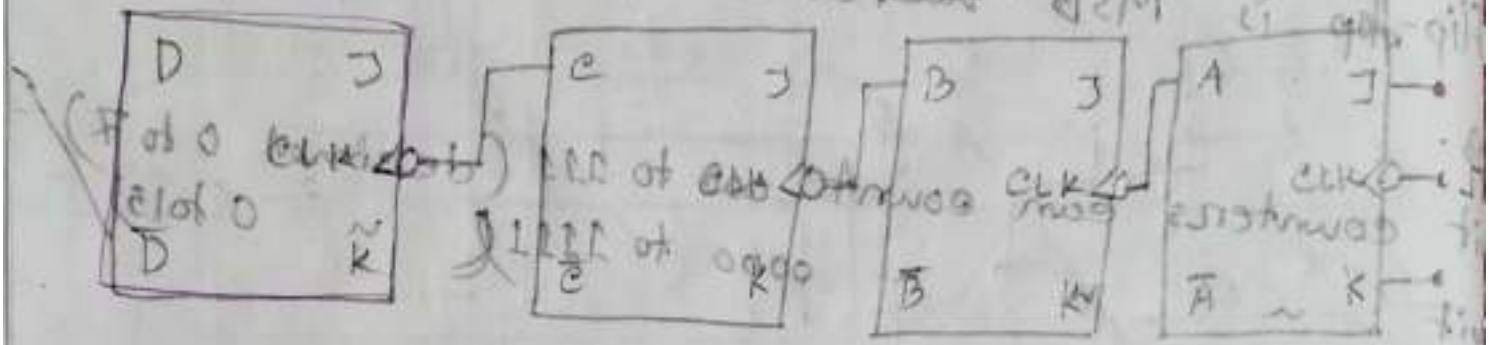
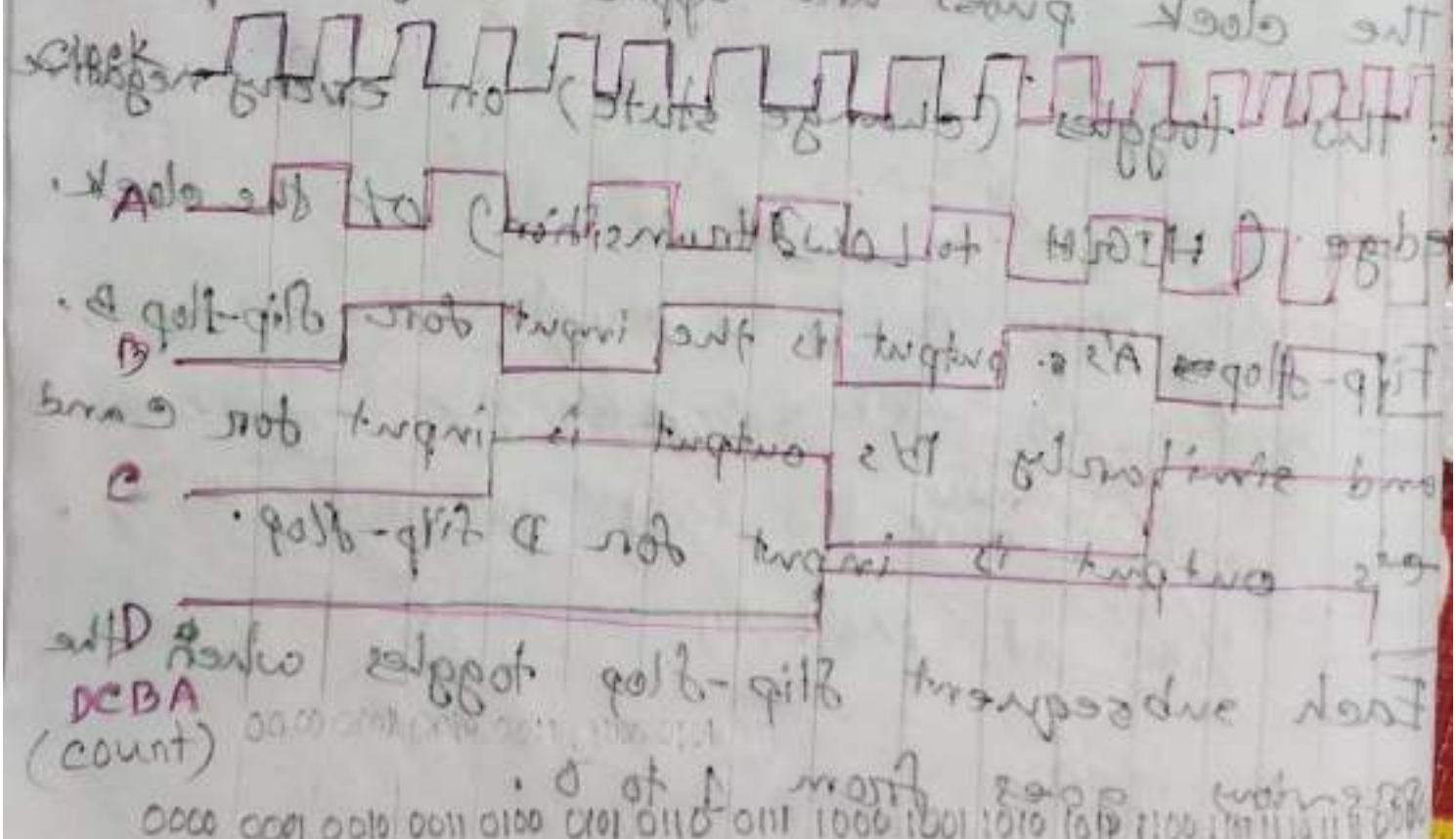
(9) After reaching 1111 (15) the next clock pulse brings the counter back to 0000. It happens when complete 8/16 clock pulse.



All J and K input assumed to be 1.



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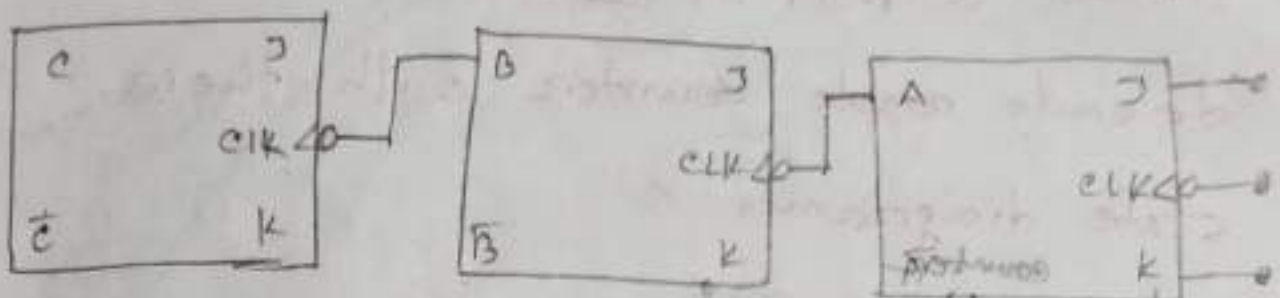
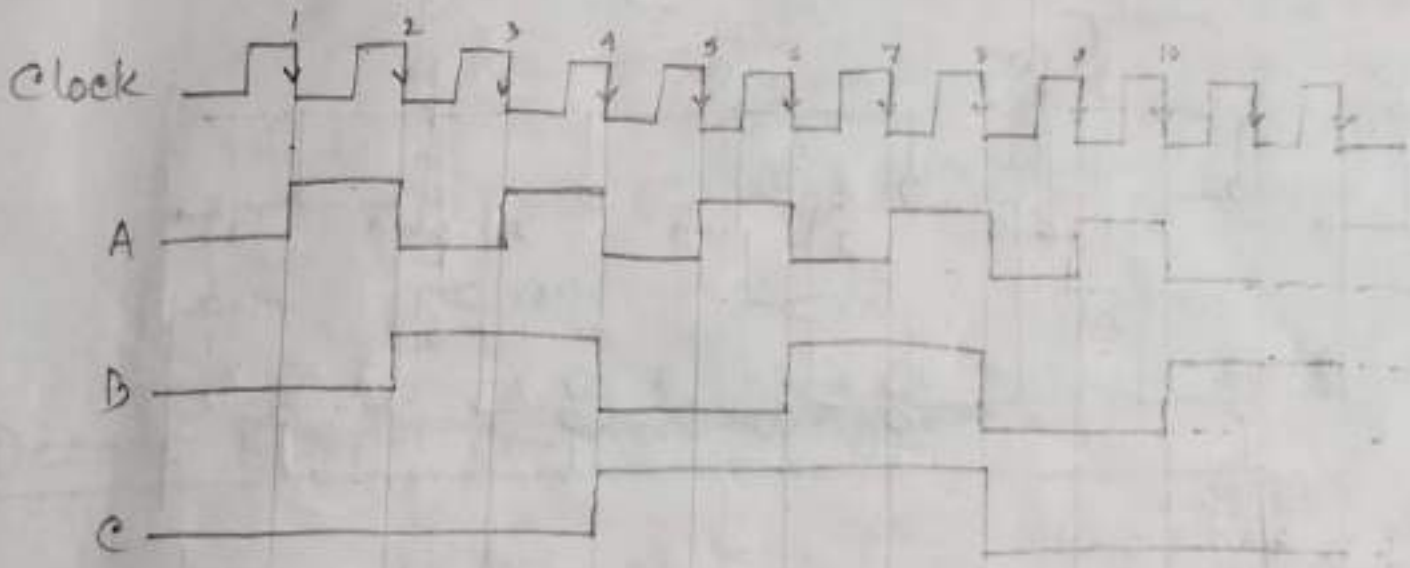


All inputs J and K are assumed to be 1



C B A (count)	000	001	010	011	100	101	110	111	000	001

→ recycle to 000

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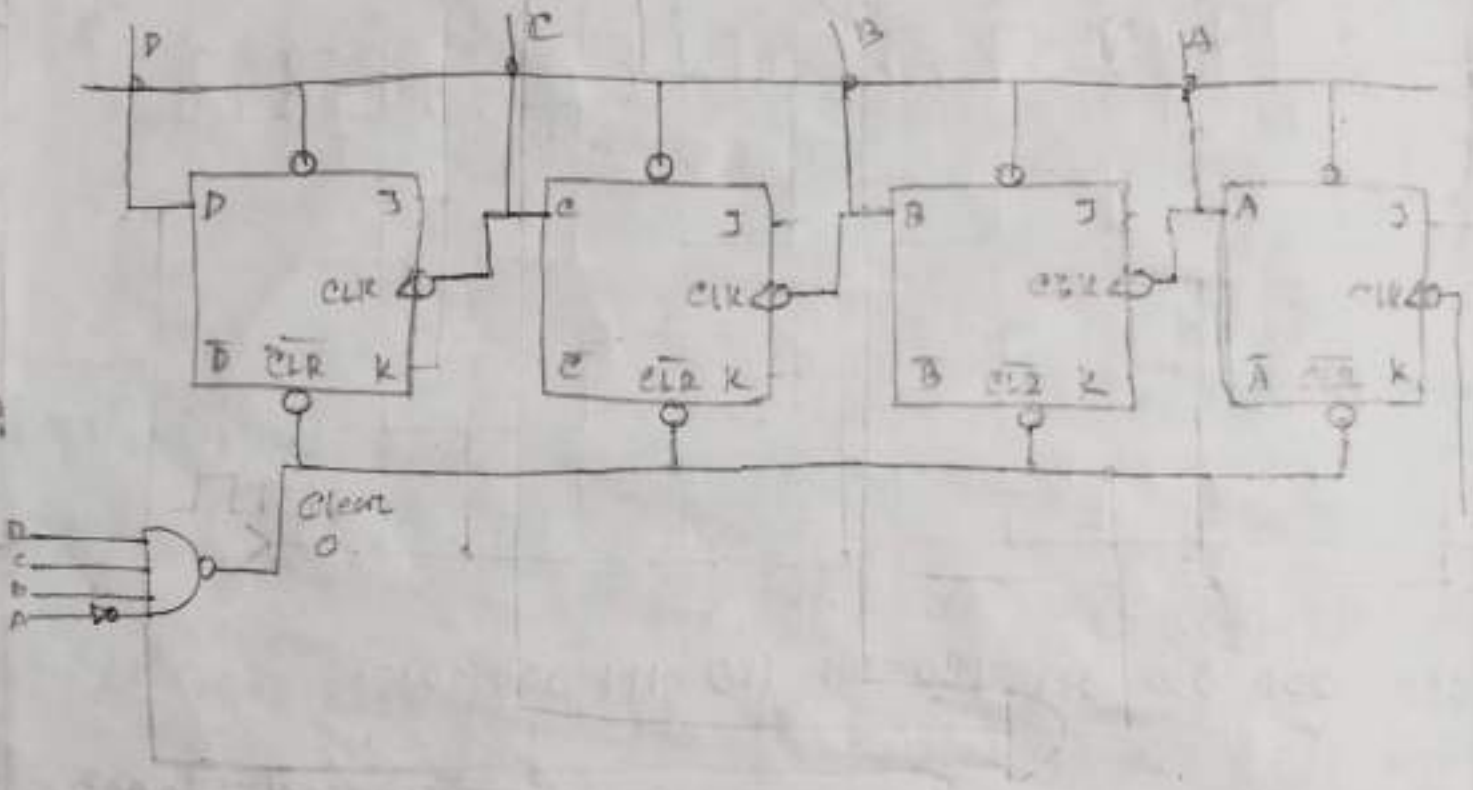
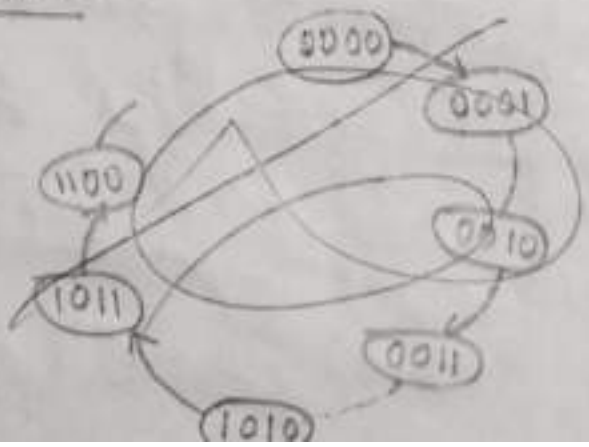
[14] Draw a Mod-14 ~~counter~~ and a decade ripple counter with their state diagram.

Mod-14 counter diagram:



Mod-14

State transition Diagram:



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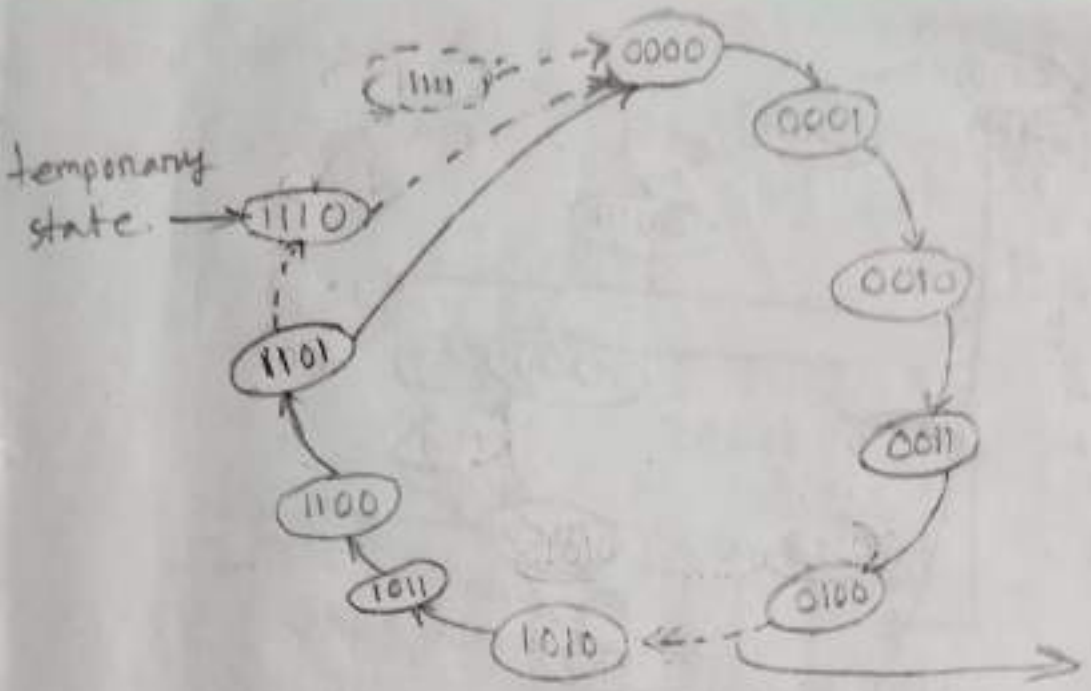
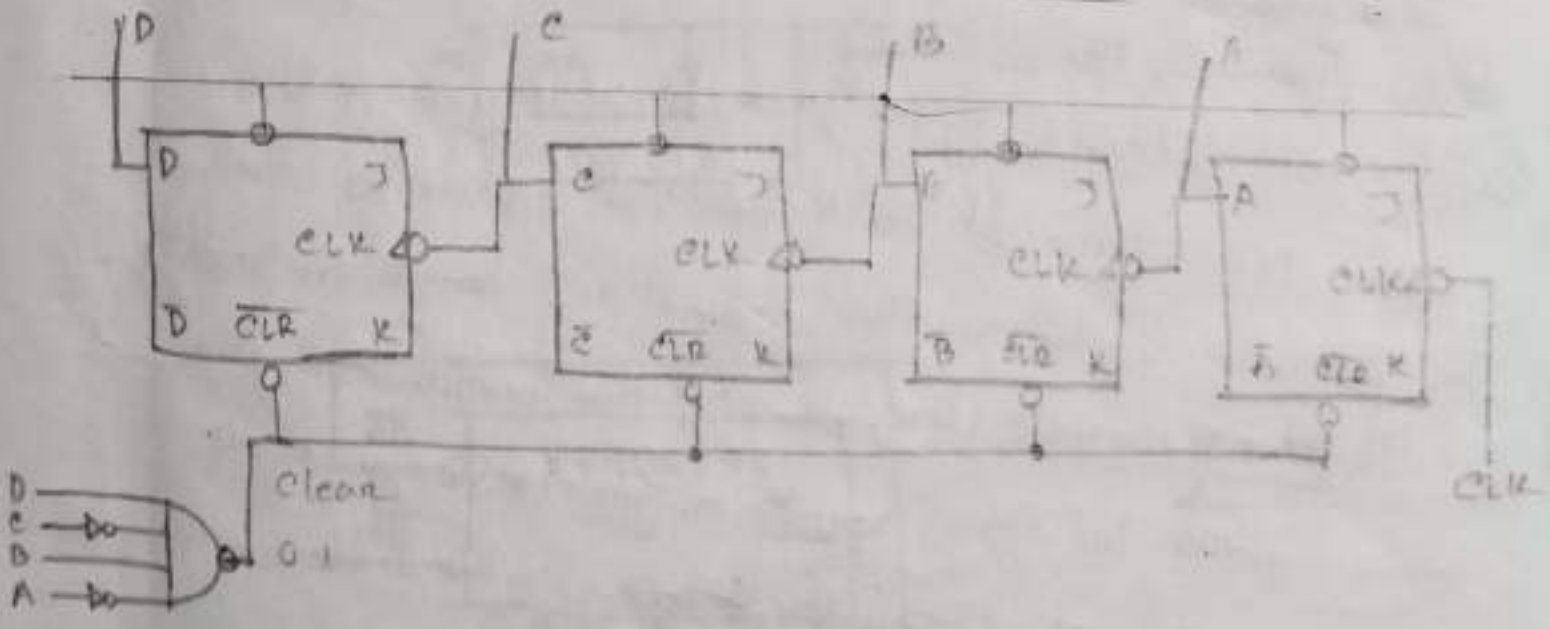


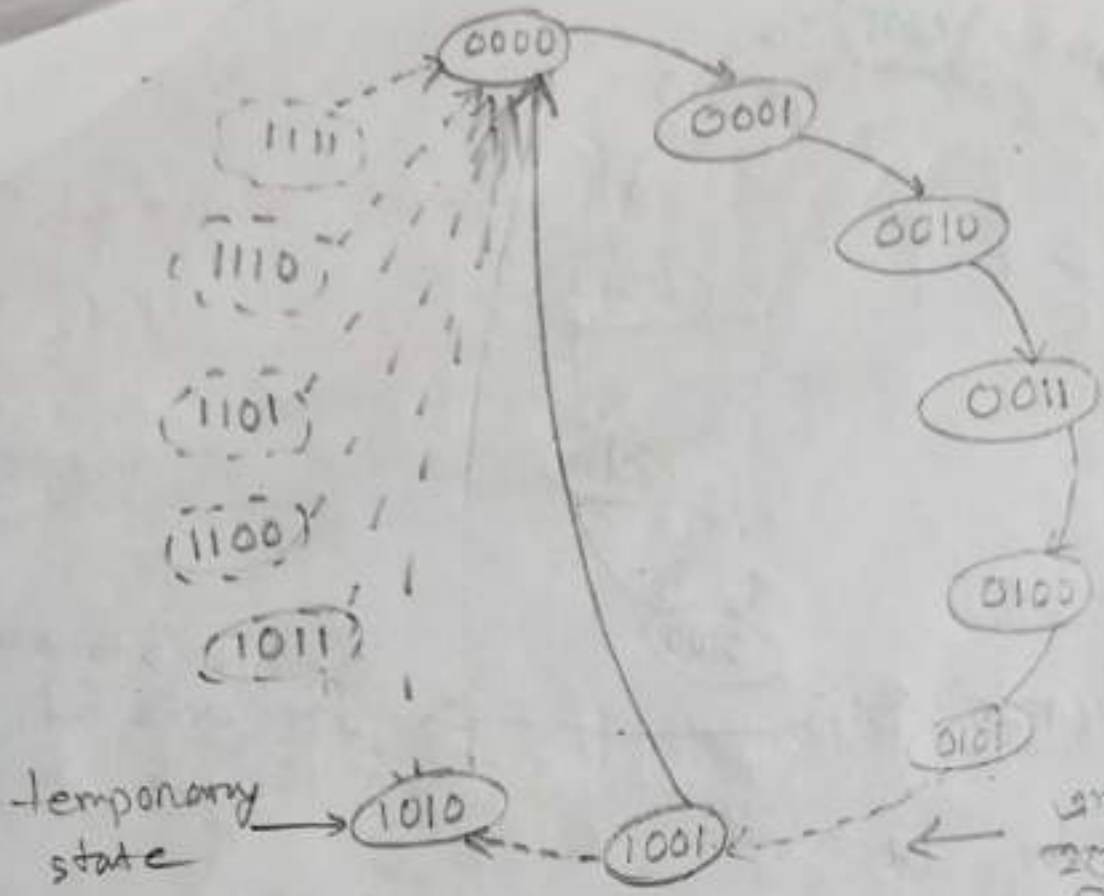
State transition diagram of Mod-14

Decade Ripple counter diagram:



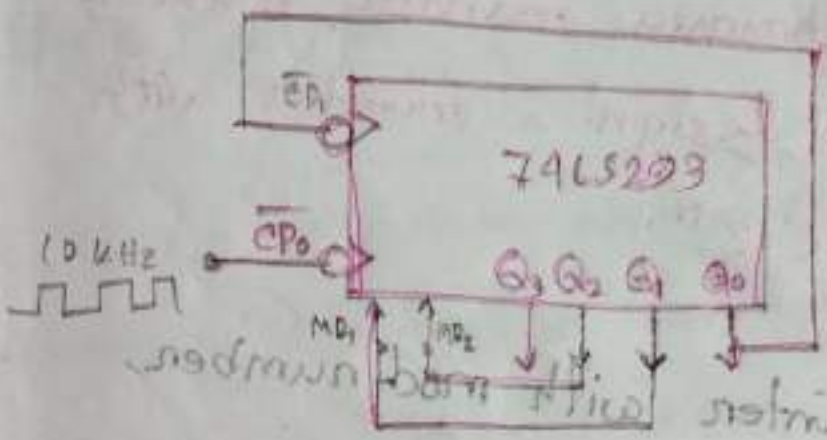
Decade counter can counts binary 0000 to 1001.

Decade counter can counts binary 0000 to 1001. For this any Mod-10 counter is to be a decade counter

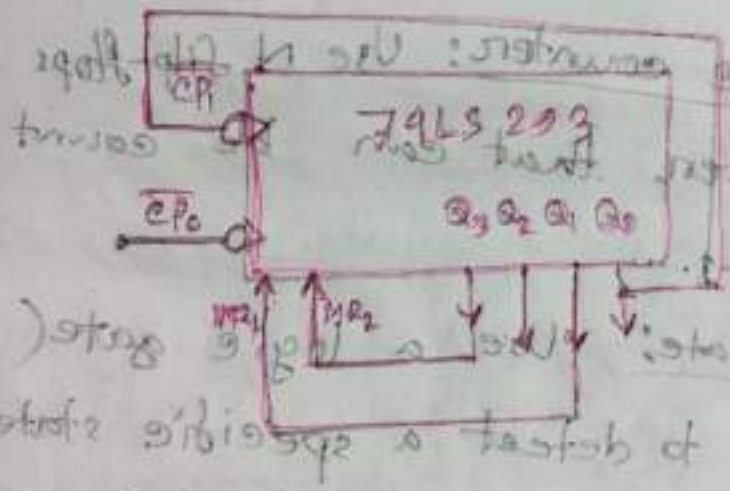


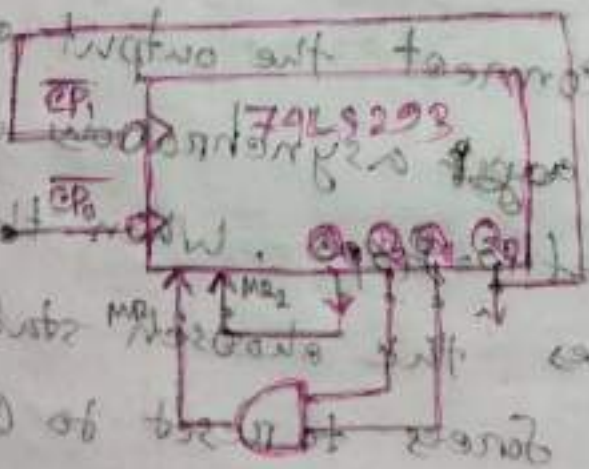
state transition of decade (Mod-10) Ripple counter diagram

How to wire the 74LS293/74293 as a Mod-6 counter? / Mod-10 / Mod-14.



Mod 6





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What is Mod number? What is ripple counter? What is decade counter? What is synchronous counter? What is the method to design a counter with mod no number $< 2^N$.

To design a counter with mod number, follow these steps:

① Start with a basic counter: Use N flip-flops to create a counter that can be count from 0 to $2^n - 1$.

② Add a logic gate: Use a logic gate (like NAND gate) to detect a specific state in count where the counter back to reset.

③ Trigger reset: Connect the output of the logic gate to the asynchronous clear (CLR) inputs of the flip-flops. When the counter reaches the choosen state, the logic gate forces to reset to 000.

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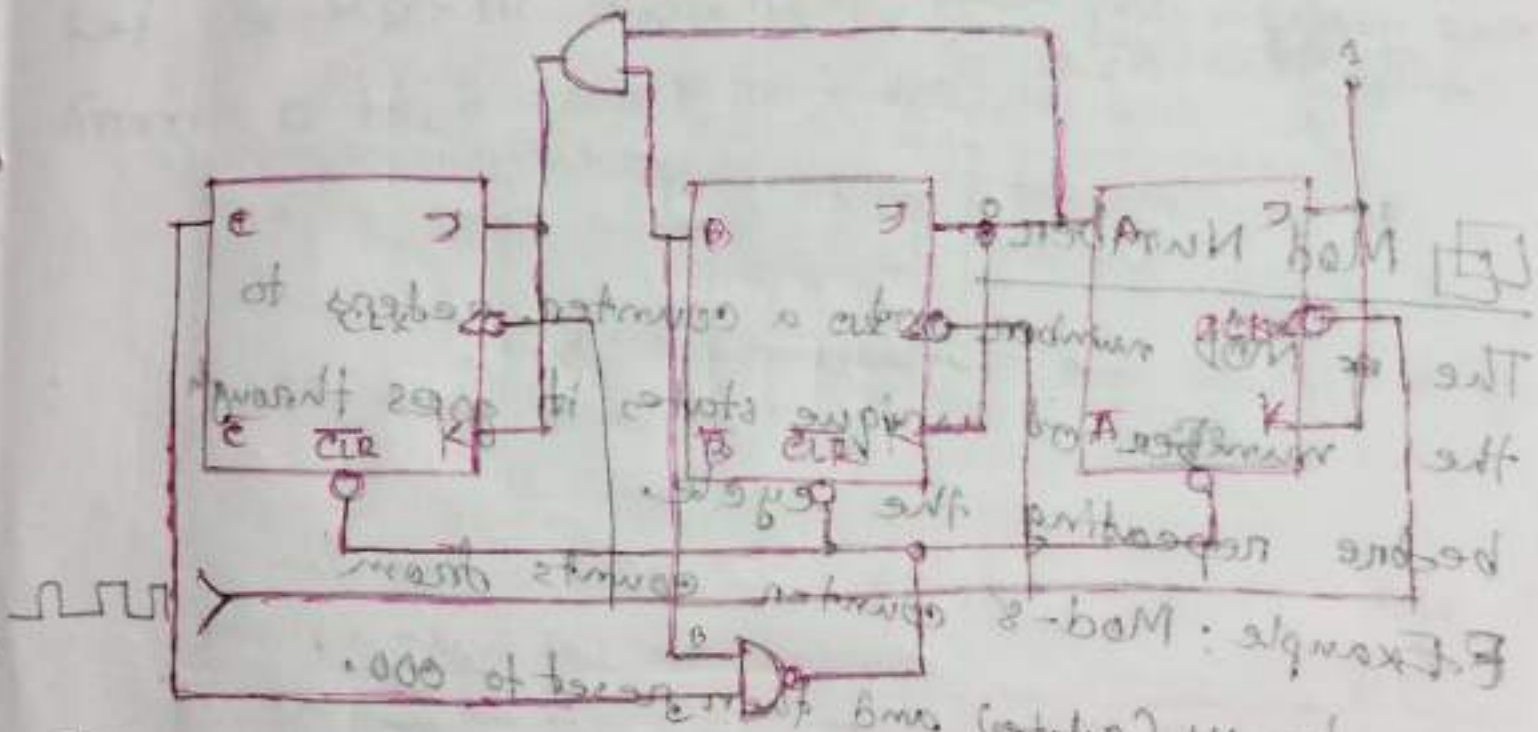
2. Skip certain states: By resetting early, the counter skips next steps and reducing the Mod number. Example 3-bit counter can be modified as Mod-6 counter by resetting at state 110.

Here is a diagram of Mod-6 counter produced by clearing a MOD-8 counter when it count of six (110).



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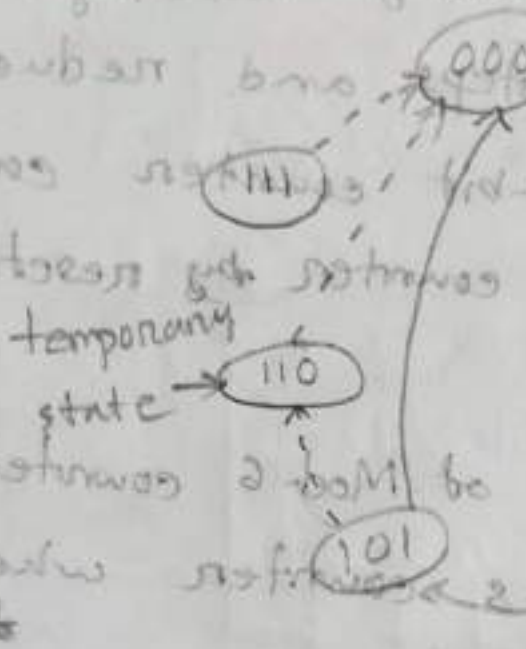
B	A
0	0
0	1
1	0
1	1
0	0
1	0
1	1
0	0



temporary state needed to clear counter

Mod Number:

The MOD number of a counter refers to the number of unique states it goes through before repeating the cycle.

Example: Mod-8 counter counts from 000 to 111 (8 states) and then reset to 000.

Ripple Counter:

A ripple counter is an asynchronous counter where the clock signal applied only to the first flip-flops (FF). Each subsequent flip-flops clock is driven by the output of

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previous flip-flop.

Synchronous counter:

A synchronous counter is a counter where all flip-flops are triggered simultaneously by the same clock signal.

Decade Counter:

A decade counter is a type of counter that has a MOD-10 sequence, meaning that it counts from 0 to 9 (0000 to 1001) and then resets to 0000.