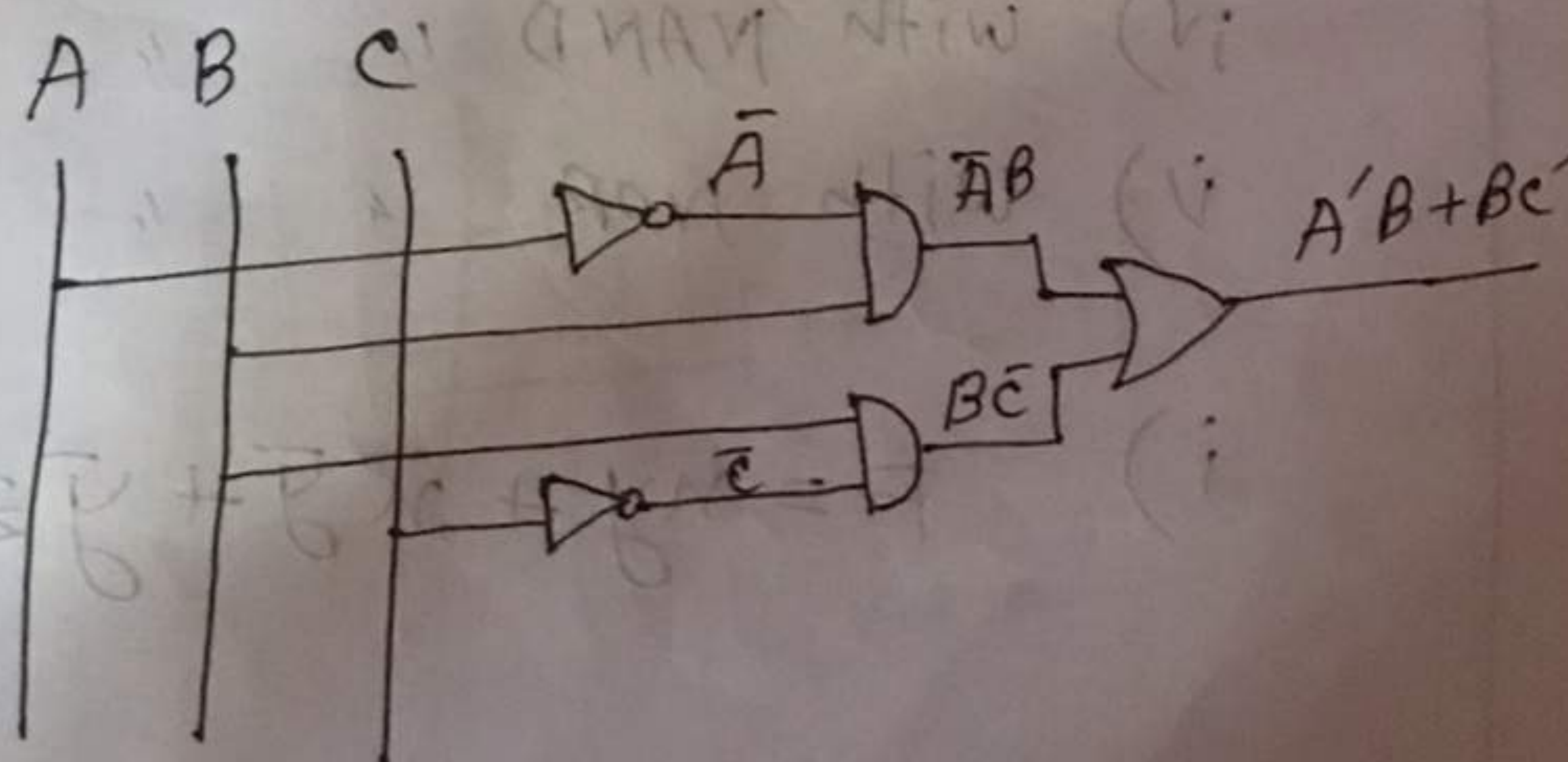
① Mention the duality principle?

The principle of duality is a kind of pervasive property of algebraic structure in which two principles or concepts are interchangeable only if all outcomes help true in one formulation are also held true in another. This concept is also referred to as "dual formulation".

② Implement the function using NAND gate?

$$F = A'B + BC'$$

Logic gate:



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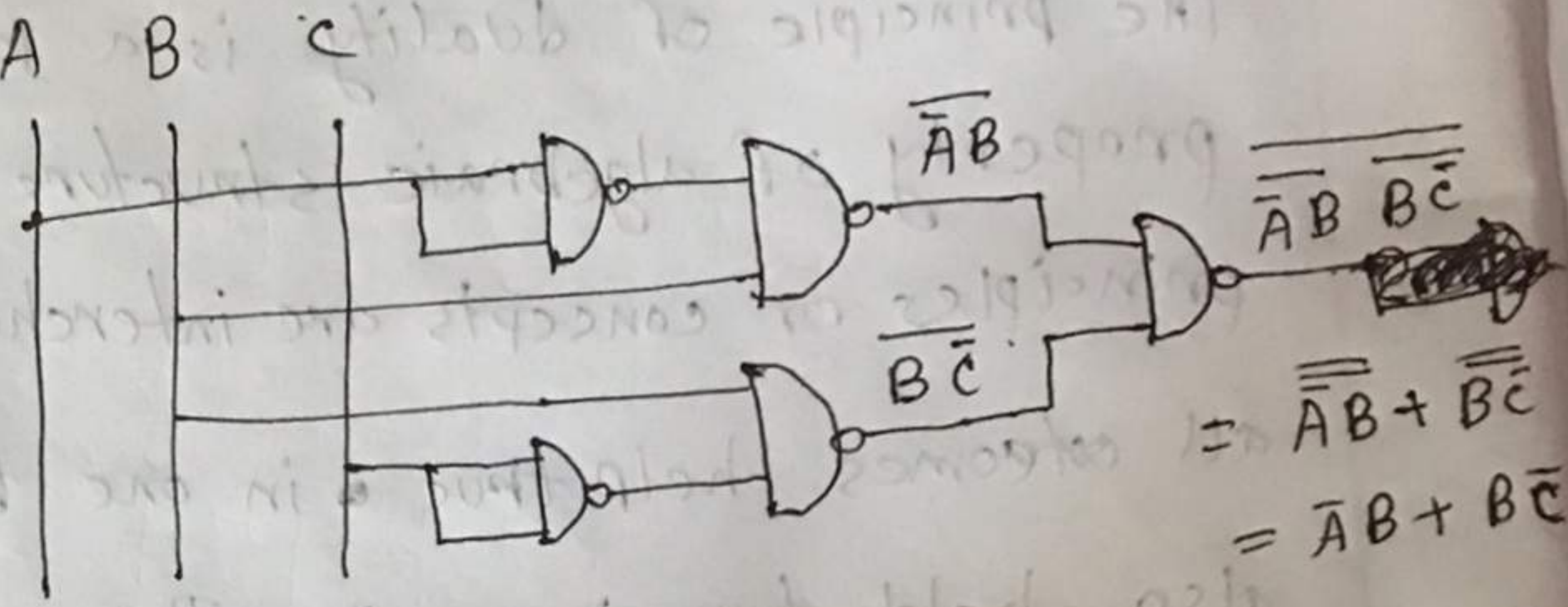
Implementation by NAND gate :



$= \overline{\overline{\bar{A}B}} + \overline{\overline{B\bar{C}}}$

$= \bar{A}B + B\bar{C}$

③ Implementation the Boolean function ?

$$F = xy + x'y' + y'z$$

i) with AND, OR, and Inverter gate

ii) with AND and Inverterr gate

iii) with OR and " "

iv) with NAND " " "

v) with NOR " " "

i) $F = xy + \bar{x}\bar{y} + \bar{y}z$

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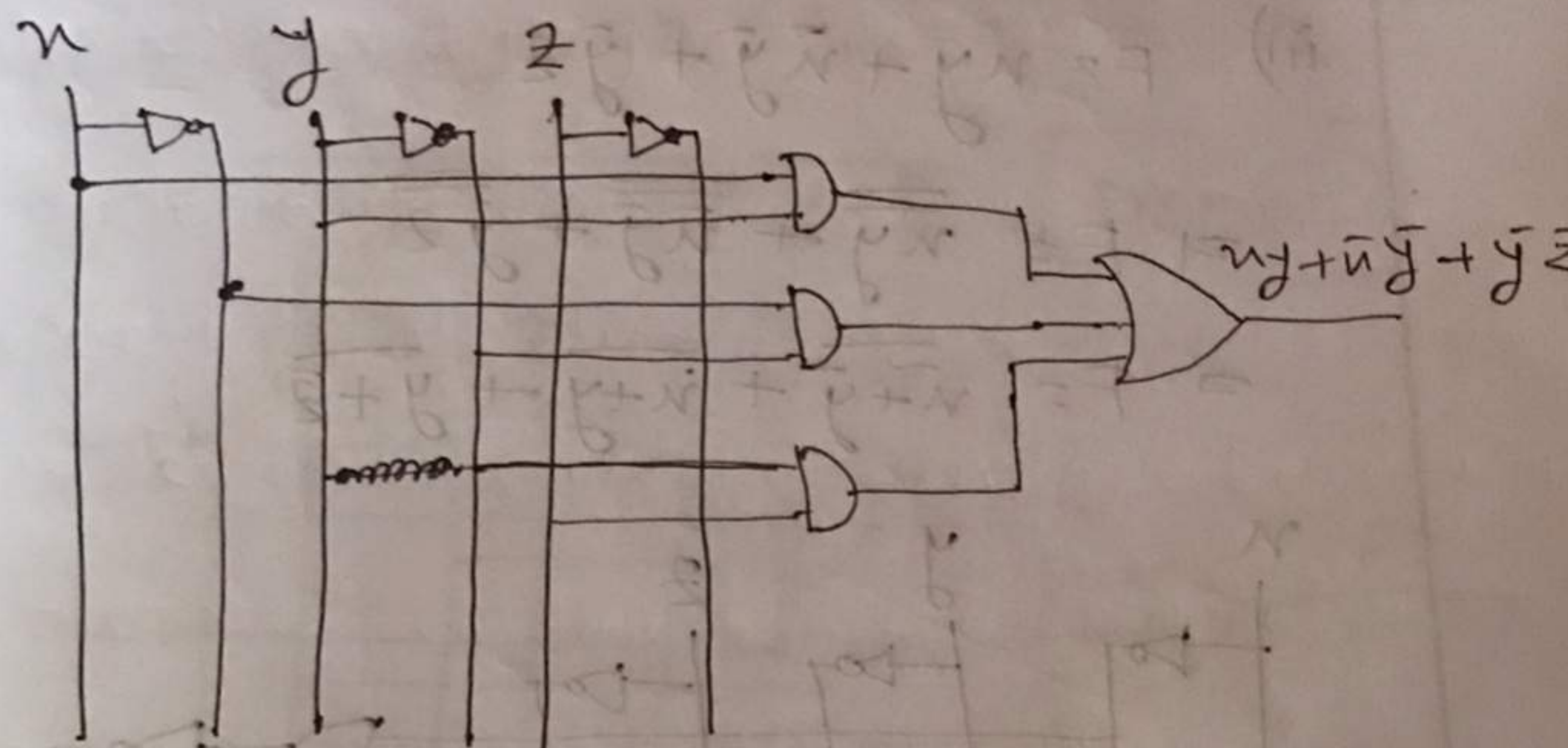
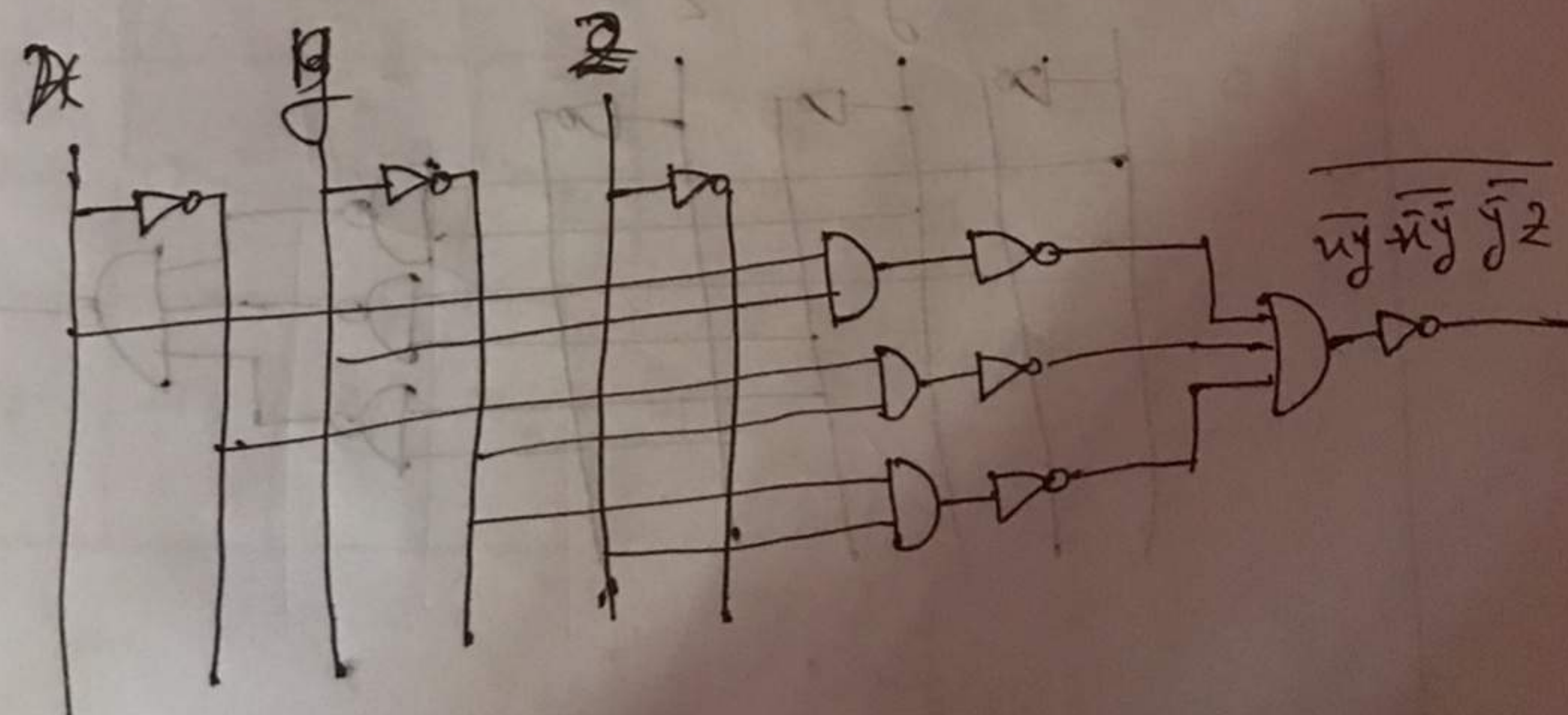


ii) $F = xy + \bar{x}\bar{y} + \bar{y}z$

$\Rightarrow F = \overline{\overline{xy + \bar{x}\bar{y} + \bar{y}z}}$

$\Rightarrow F = \overline{\overline{xy}\;\overline{\bar{x}\bar{y}}\;\overline{\bar{y}z}}$



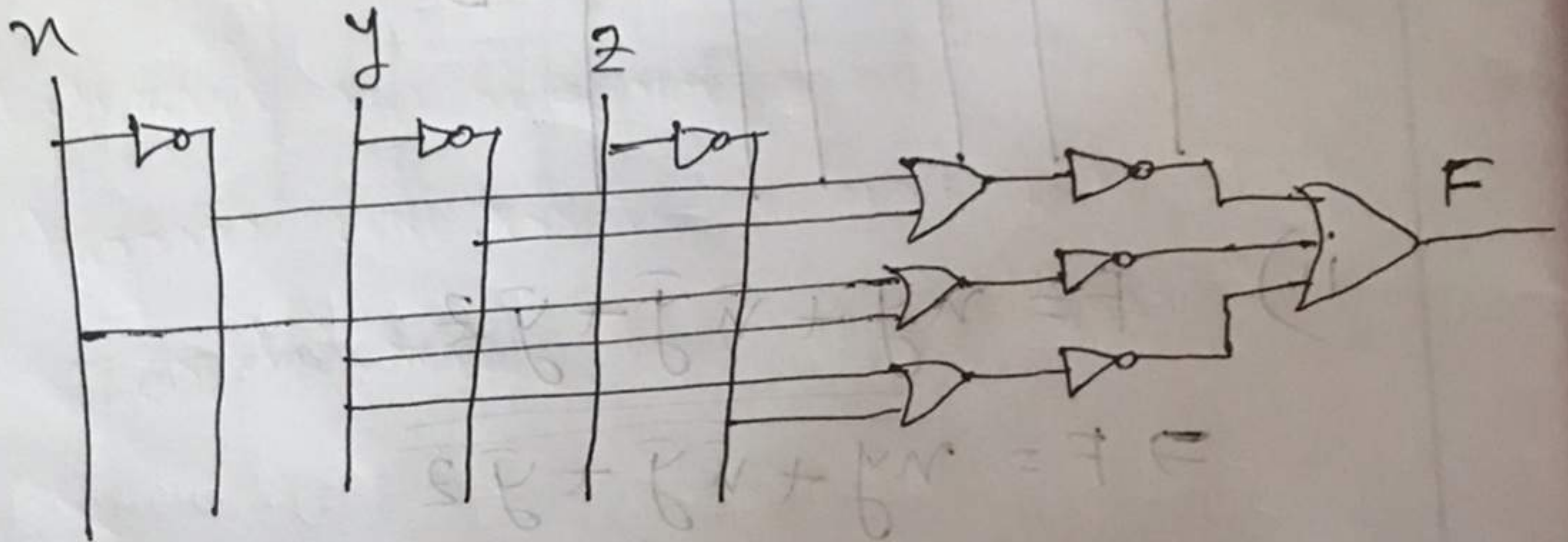
Subject: ....

Date : ....

iii) $F = xy + \bar{x}\bar{y} + \bar{y}z$

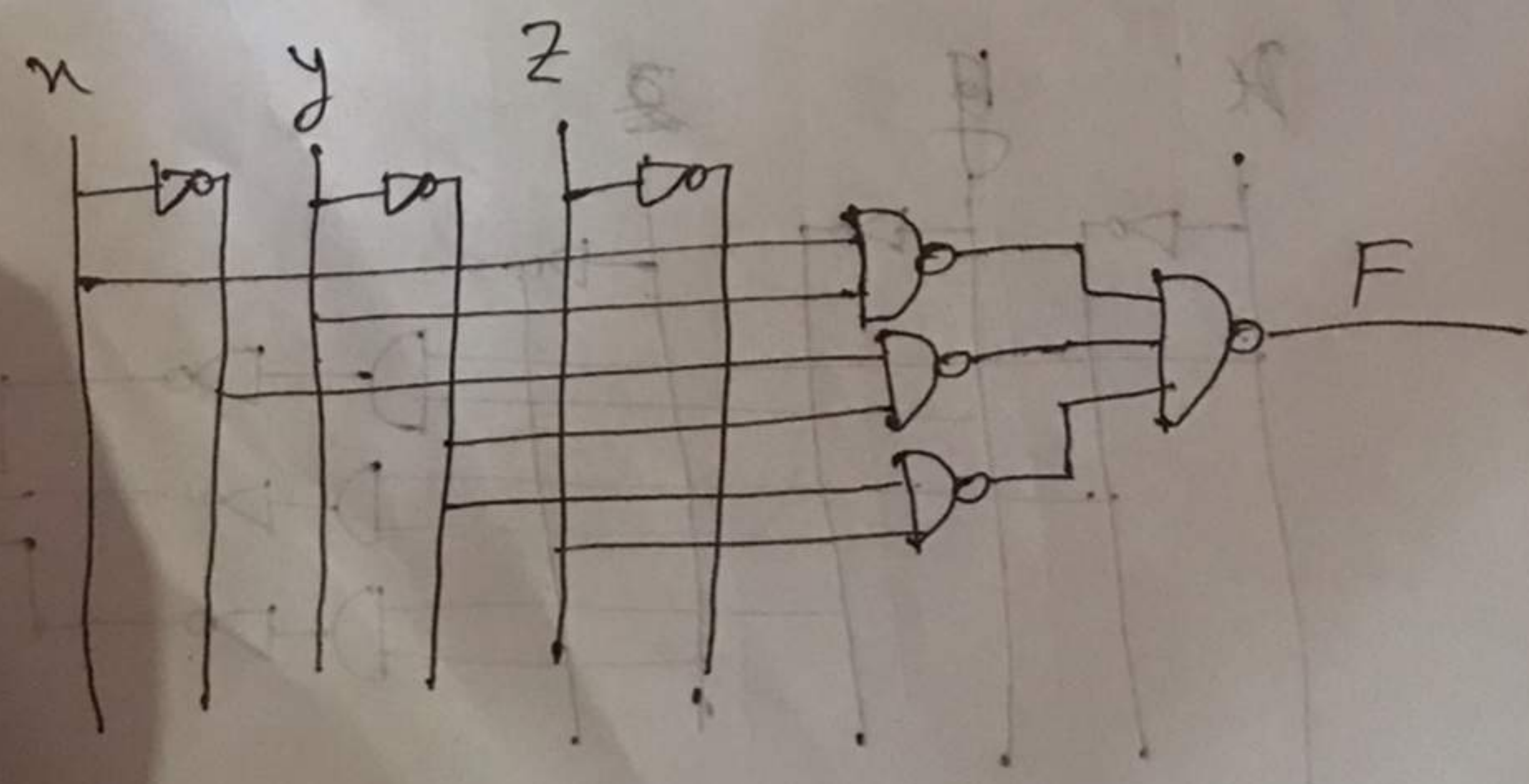
$\Rightarrow F = \overline{\overline{xy}} + \overline{\overline{\bar{x}\bar{y}}} + \overline{\overline{\bar{y}z}}$

$\Rightarrow F = \overline{\bar{x}+\bar{y}} + \overline{x+y} + \overline{y+\bar{z}}$



iv) $F = xy + \bar{x}\bar{y} + \bar{y}z$ [From (ii)]

$\Rightarrow F = \overline{\overline{xy}\;\;\overline{\bar{x}\bar{y}}\;\;\overline{\bar{y}z}}$



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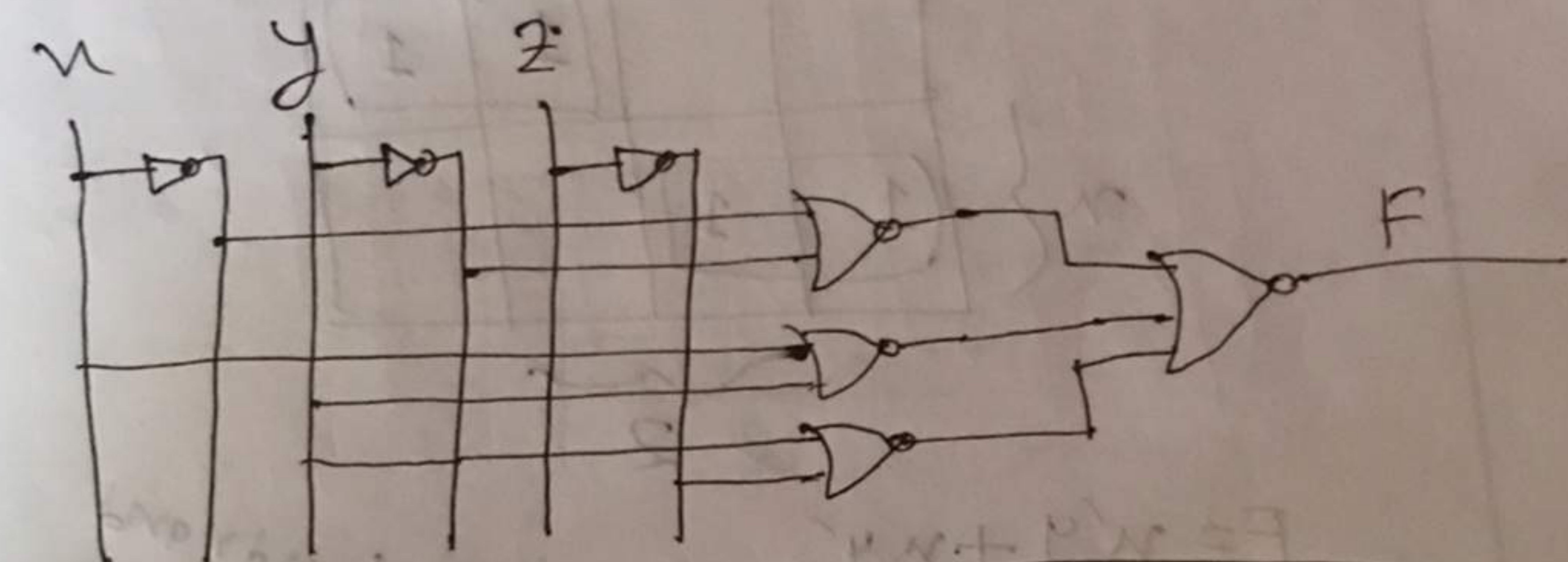
(v) $F = xy + \bar{x}\bar{y} + yz$

$\Rightarrow F = \overline{\bar{x}+\bar{y}} + \overline{x+y} + \overline{y+\bar{z}}$ [From (iii)]



K-Map

variable = 3

m_0	m_1	m_3	m_2
m_4	m_5	m_7	m_6

Note:

$x + 0 = x$

$x + 1 = 1$

$x + x = x$

$x + \bar{x} = 1$

$x . 0 = 0$

$x . 1 = x$

$x . x = x$

$x . \bar{x} = 0$

$2^3 = 8$

x\yz	y'		y	
$\bar{x}$	$x'y'z'$			
x				
	z'	z		z'

$x'y'z'$

Subject:

Date :

Example : ① standard form

$F = x'yz + x'yz' + xy'z' + xy'z$

$x \backslash yz$ $\quad$ y

			1	1
x	1	1		

z

$F = x'y + xy'$

standard form

Example : ②

$F = A'C + A'B + AB'C + BC$

$A \backslash BC$ $\quad$ B

		1	1	1
A		1	1	

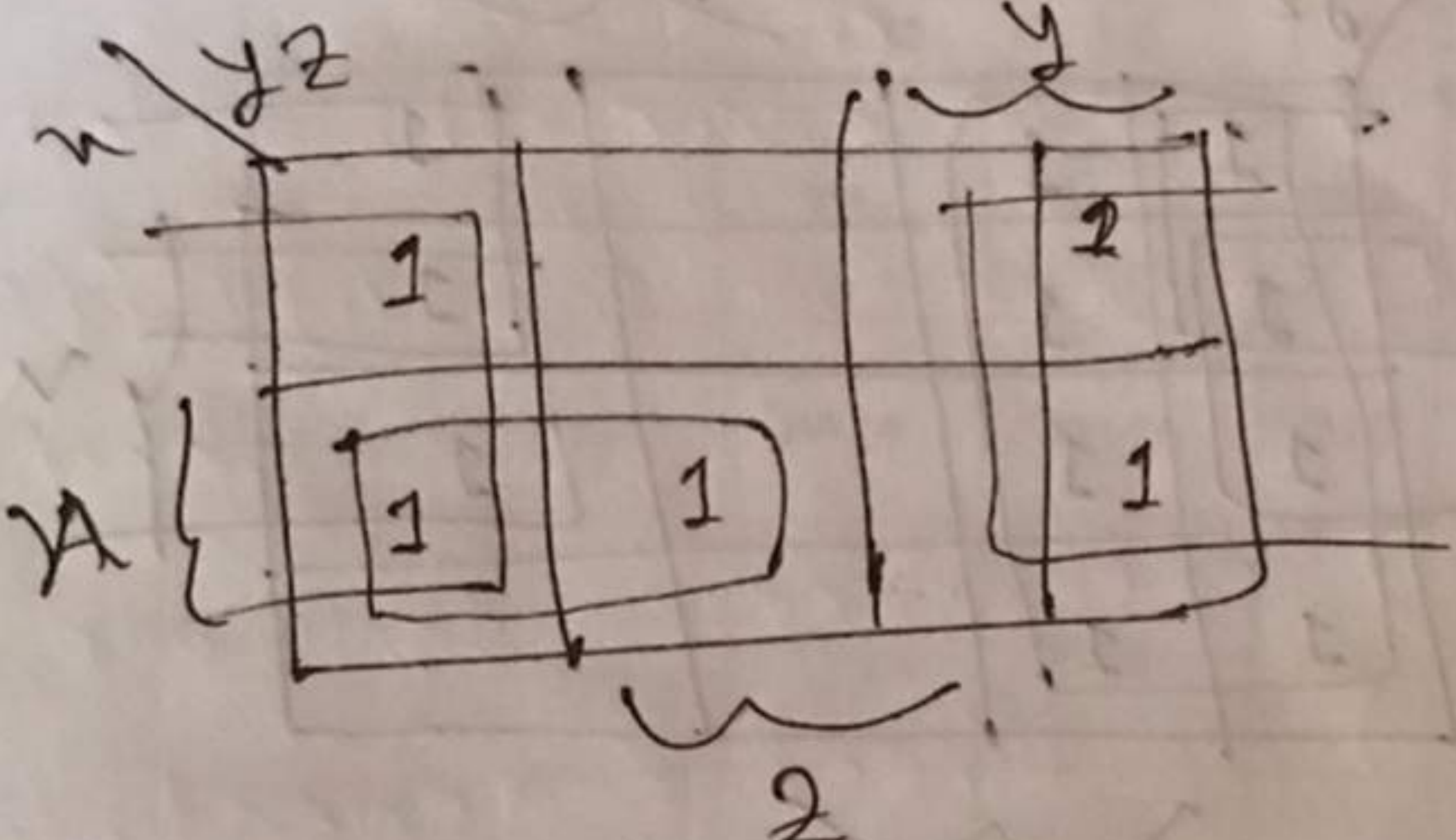
C

$F = C + A'B$

Subject:
Date: canonical form

Example : 3

$F(x,y,z) = \Sigma(0,2,4,5,6)$

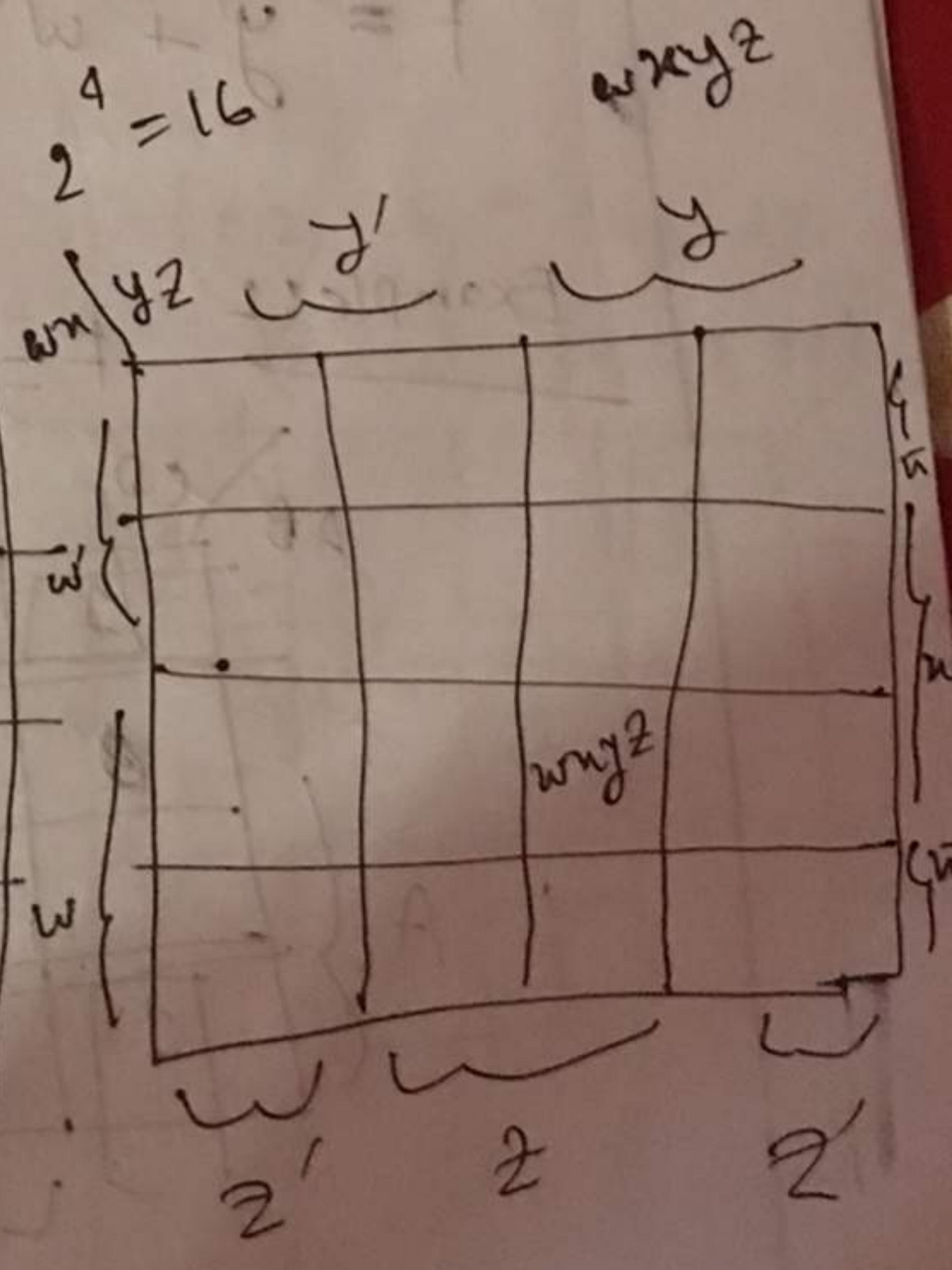


$F = z' + xy'$

4 variable

$2^4 = 16$

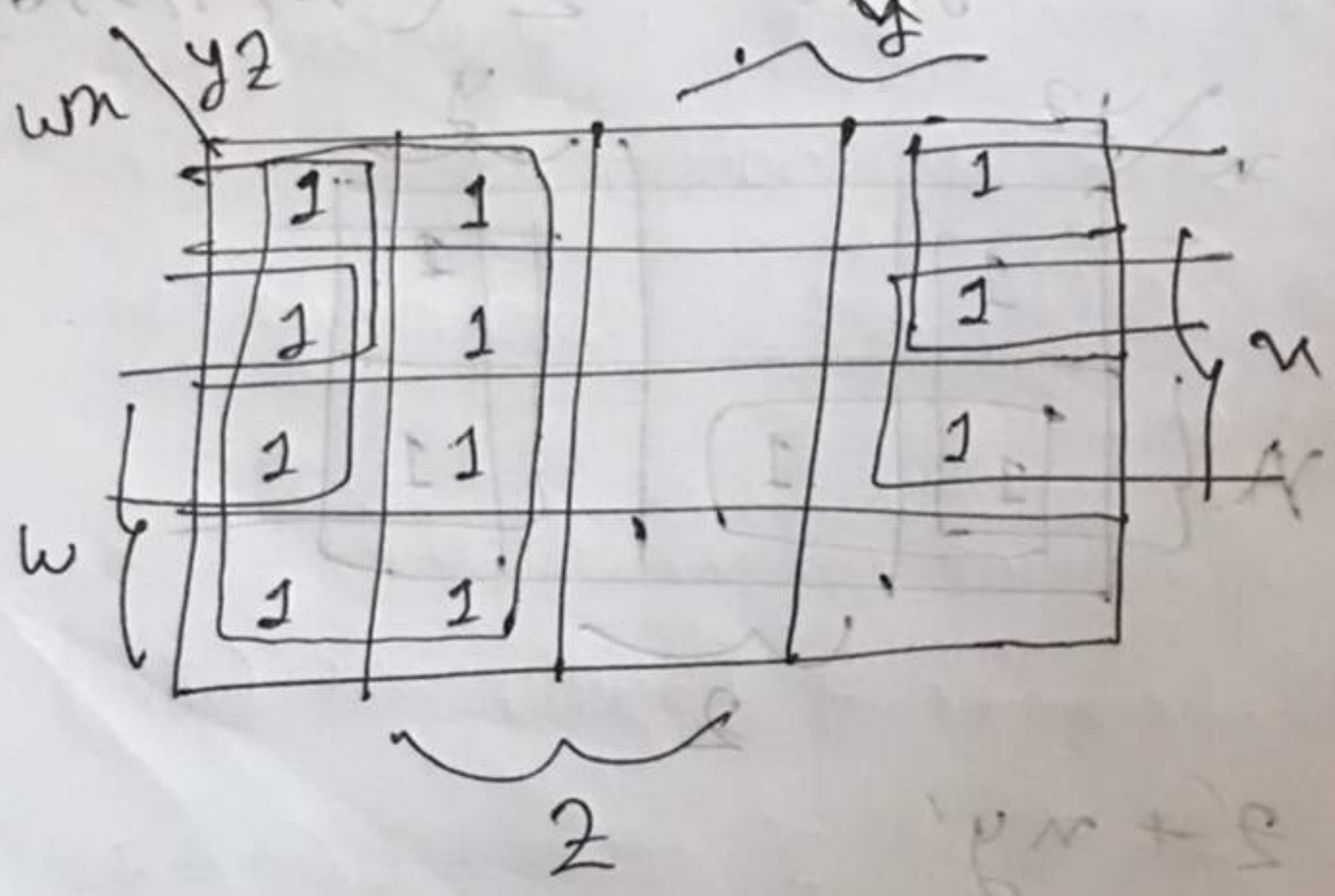
m_0	m_1	m_3	m_2
m_4	m_5	m_7	m_6
m_{12}	m_{13}	m_{15}	m_{14}
m_8	m_9	m_{11}	m_{10}



canonical form

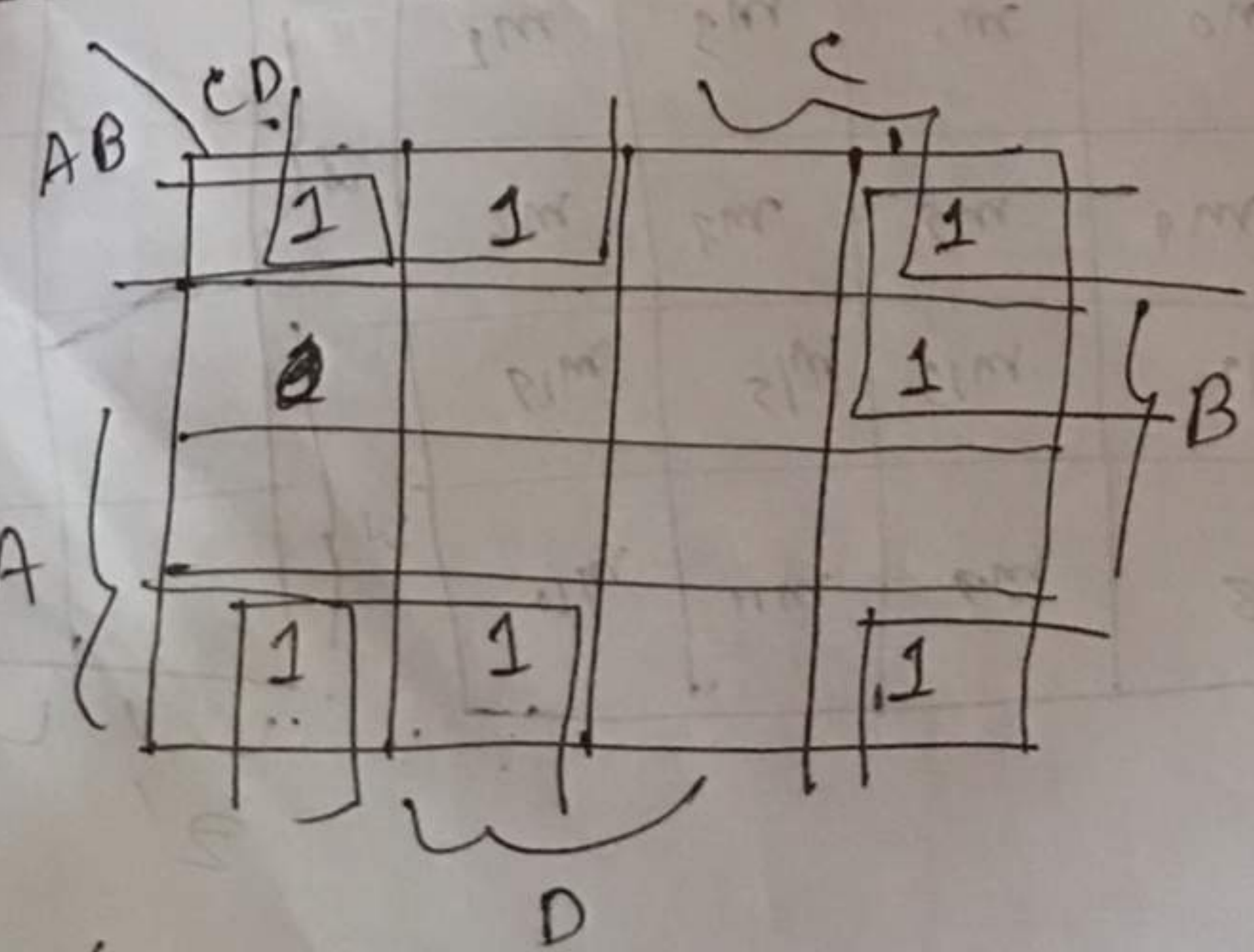
Subject:
Date:

Example : 1 $f(w,x,y,z) = \Sigma(0,1,2,4,5,6,8,9,12,13,14)$



$F = y' + w'z' + xz'$

Example : 2 $F = A'B'C' + B'CD' + A'BCD' + AB'C'$



$F = B'C' + B'D' + A'CD'$

Subject:
Date:

5 Variable

$A'BCDE'$ $\quad 2^5 = 32$ $\quad A'B'C'D'E'$

AB \ CDE	$C'D'E'$ 000	$C'D'E$ 001	$C'DE$ 011	$C'DE'$ 010	CDE' 110	CDE 111	$CD'E$ 101	$CD'E'$ 100
$A'B'$ 00	$A'B'C'D'E'$ m_0	m_1	m_3	m_2	m_6	m_7	m_5	m_4
$A'B$ 01	m_8	m_9	m_{11}	m_{10}	$A'BCDE'$ m_{14}	m_{15}	m_{13}	m_{12}
AB 11	m_{24}	m_{25}	m_{27}	m_{26}	m_{30}	m_{31}	m_{29}	m_{28}
AB' 10	m_{16}	m_{17}	m_{19}	m_{18}	m_{22}	m_{23}	m_{21}	m_{20}

Example: 1

$$F(A,B,C,D,E) = \sum(0,2,4,6,9,11,13,15,17,21,25,27,29,31)$$

AB \ CDE	$C'D'E'$	$C'D'E$	$C'DE$	$C'DE'$	CDE'	CDE	$CD'E$	$CD'E'$
$A'B'$	1			1	1			1
$A'B$		1	1			1	1	
AB		1	1			1	1	
AB'		1					1	

$\boxed{F = BE + A'B'E' + AD'E}$

Ans.

Subject:
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(4) List Limitation of k-map ?

i) scalability ii) visual complexity
iii) Human error iv) Limited to Binary Logic
v) complex Functions vi) Difficulty with don't cares
vii) Dependence on completeness
viii) No Direct Implementation.

Sum of product / minterms
product of sum / maxterms

$$\boxed{\begin{array}{l} \text{minterms} \Rightarrow x'y'z' \\ \text{maxterms} \Rightarrow x+y+z. \end{array}}$$

Sum of product / minterms:

$$F = A + B'C$$

$$A = A(B+\bar{B}) \qquad [B+\bar{B}=1]$$

$$\Rightarrow A = AB + A\bar{B}$$

$$\Rightarrow A = AB(C+\bar{C}) + A\bar{B}(C+\bar{C})$$

$$\Rightarrow A =$$

Subject:
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$\Rightarrow A = ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C}$

$\Rightarrow \bar{B}C = \bar{B}C(A+\bar{A})$

$\Rightarrow A\bar{B}C + \bar{A}\bar{B}C$

$F = A + \bar{B}C$

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + \bar{A}\bar{B}C$

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C$

$[x+x=x]$

$= m_7 + m_6 + m_5 + m_4 + m_1$

$F(A,B,C) = \sum(1,4,5,6,7)$

product of sum / max terms

$F = xy + x'z$

$= (x+x'z)(y+x'z)$

$= (x+x')(x+z)(y+x')(y+z)$

$x+x' = \cancel{x+x'+y.y'} \quad [y.y'=0]$

$= \cancel{(x+x'+y)}\cancel{(x+x'+y')}$

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$\cancel{x+z = x+z}$.

$= (x+z)(y+x')(y+z)$

$x+z = x+z+y\cdot\bar{y} \quad \boxed{y\cdot\bar{y}=0}$

$= (x+z+y)(x+z+\bar{y})$

$y+x' = y+x'+z\cdot\bar{z}$

$= (y+x'+z)(y+x'+\bar{z})$

$y+z = y+z+x\cdot\bar{x}$

$= (y+z+x)(y+z+\bar{x})$

$F = (x+y+z)(x+\bar{y}+z)(\bar{x}+y+z)(\bar{x}+y$

$(x+y+z)(\bar{x}+y+z)$

$= (x+y+z)(x+\bar{y}+z)(\bar{x}+y+z)(\bar{x}-$

$= M_0 \, M_2 \, M_4 \, M_5.$

$F(x,y,z) = \Pi(0,2,4,5)$

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(5) Simplify the following Boolean function D in product of sum—

$\Rightarrow D = BDE' + CD'E'$

$\Rightarrow$ ~~$D = (BDE' + BCD'E')$~~

$\Rightarrow$ ~~$D = BDE' +$~~

A	B	C
4	2	1
1	1	0

(6)

$A \; B \; C' \Rightarrow m_6$

$A' + B' + C \Rightarrow M_6$

Solve : $D = BDE' + CD'E'$

$\Rightarrow D = (B + CD'E')(D + CD'E')(E' + CD'E')$

$\Rightarrow D = (B+C)(B+D')(B+E')(D+C)(D+D')$
$(D+E')(E'+C)(E'+D')(E'+E')$

$\Rightarrow D = (B+C)(B+D')(B+E')(D+C)(D+E')$
$(E'+C)(E'+D') \cdot E'$

$B+C = B+C+A\cdot\bar{A}$
$= (B+C+A)(B+C+\bar{A})$

$B+C+A = B+C+A+D\cdot\bar{D}$
$= (B+C+A+D)(B+C+A+\bar{D})$

$B+C+A+\bar{D} = B+C+A+\bar{D}+E\cdot\bar{E}$
$= (B+C+A+\bar{D}+E)(B+C+A+\bar{D}+\bar{E})$

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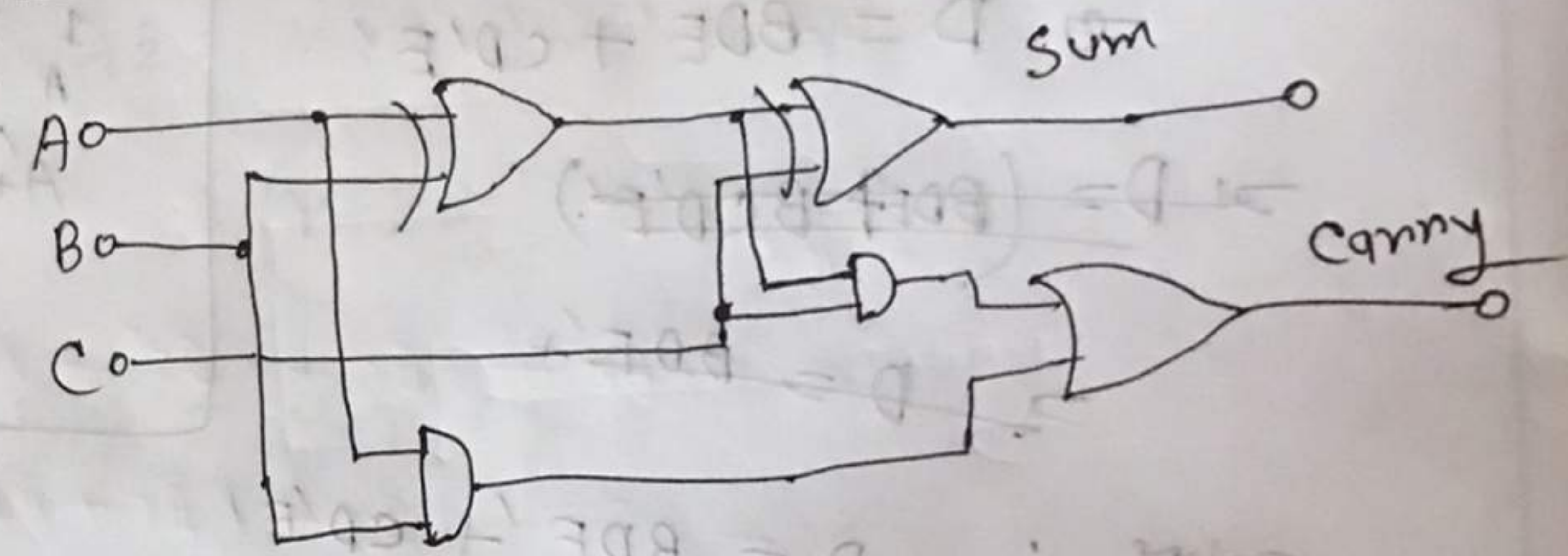
(6) Design a Full adder ?

Circuit Diagram :-



For Sum : Sum $= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$

$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$

$= A \oplus B \oplus C$

For carry : Carry $= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$

$= C(\bar{A}B + A\bar{B}) + AB(\bar{C} + C)$

$= C(A \oplus B) + AB$

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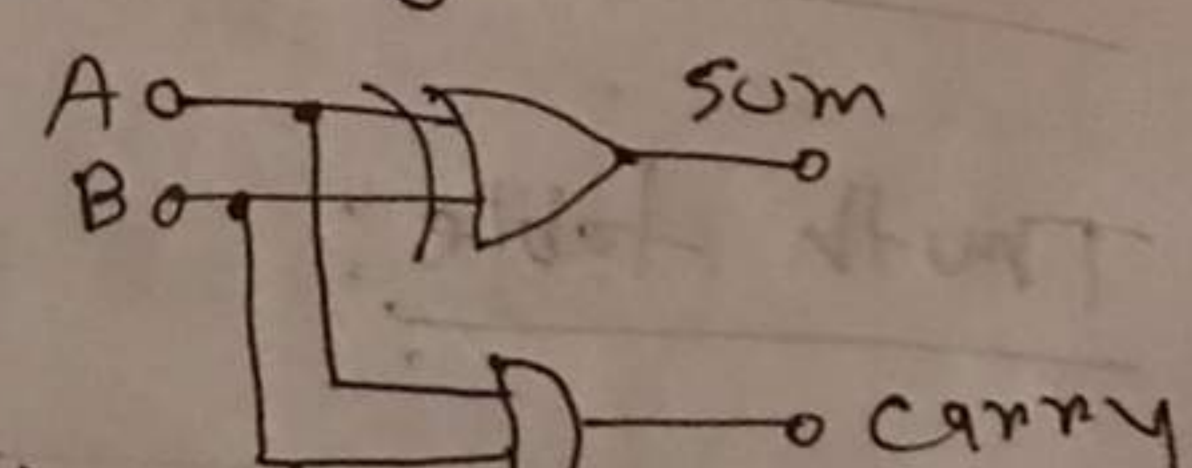
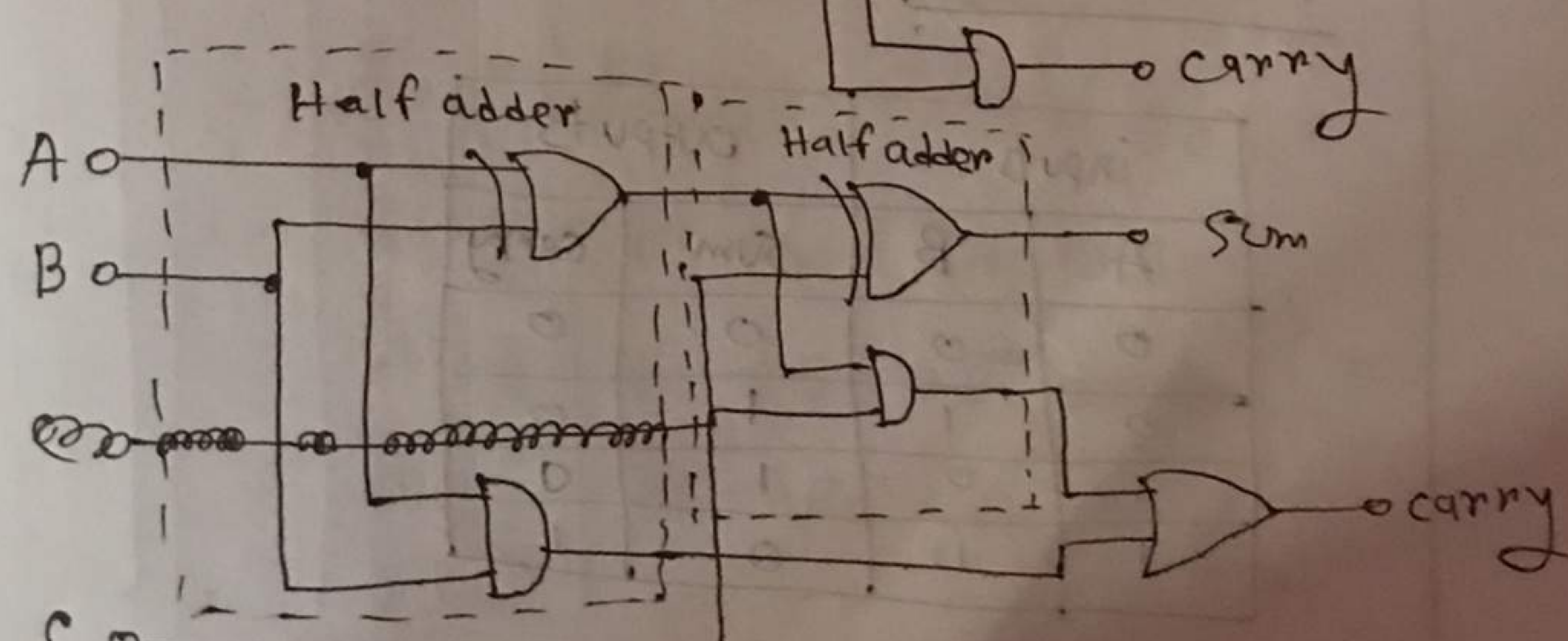
Truth table :

inputs			outputs	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	1	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(7) Draw a Full adder using two half adder?





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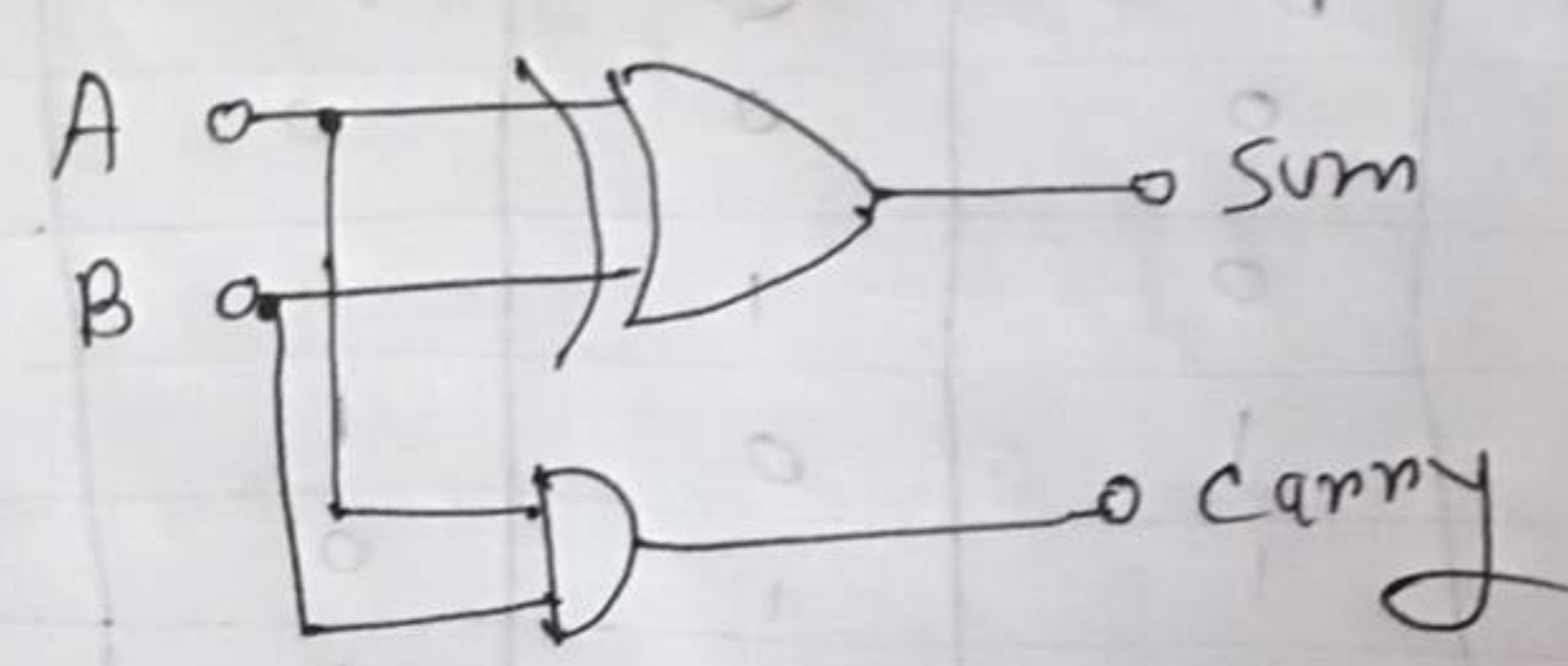
(7) Design Half adder ?

circuit Diagram:



For sum: $Sum = \bar{A}B + A\bar{B}$

$= A \oplus B$

For carry: $carry = AB$

Truth table:

inputs		outputs	
A	B	Sum.	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

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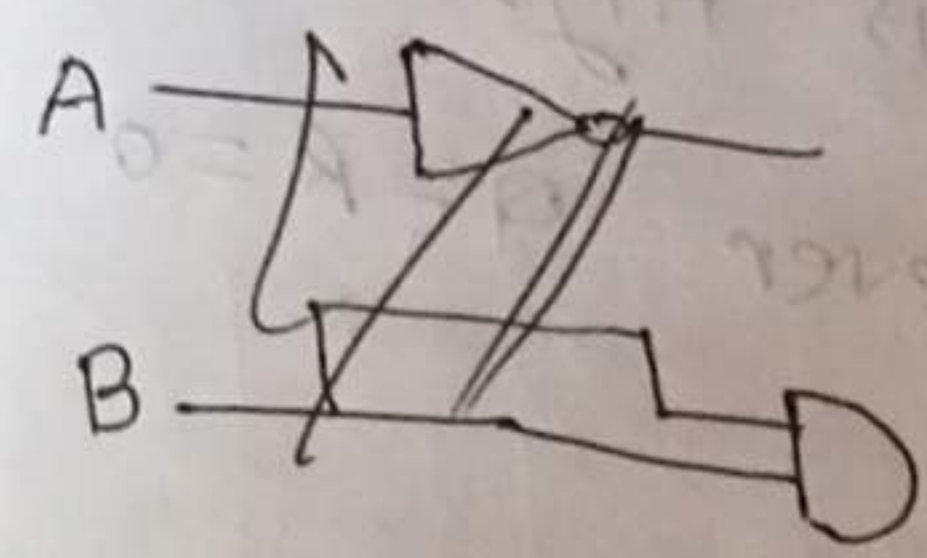
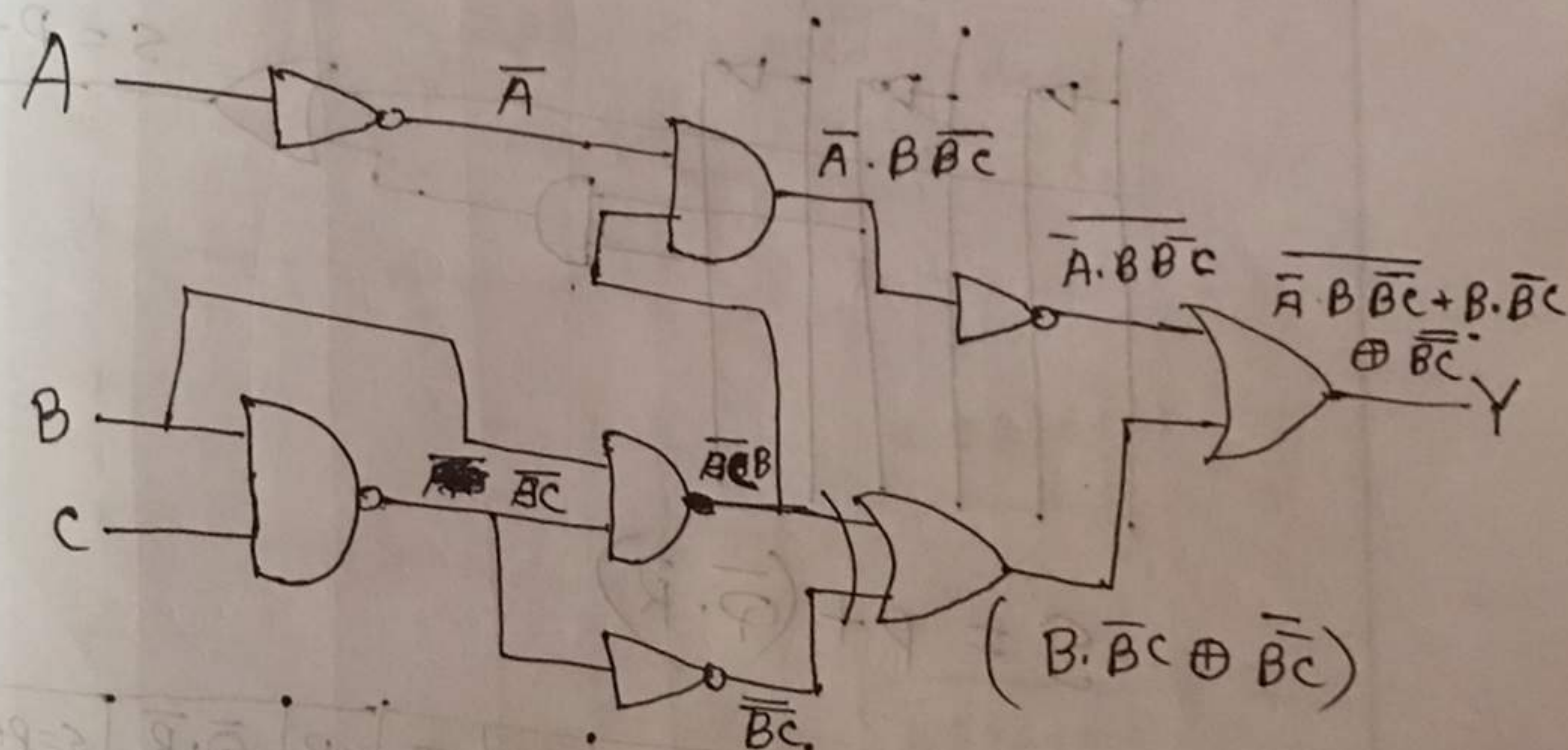
(8) Simplify the logic circuit ?





$$Y = \overline{\bar{A}\,B\,\overline{\bar{B}C}} + (B\cdot\overline{\bar{B}C} \oplus \overline{\overline{\bar{B}C}})$$

$$= \bar{\bar{A}} + \bar{B} + \overline{\overline{\bar{B}C}} + \{B(\bar{B}+\bar{C}) \oplus BC\}$$

$$= A + \bar{B} + BC + (B\bar{B} + B\bar{C} \oplus BC\}$$

$$= A + \bar{B} + BC + (B\bar{C} \oplus BC)$$

$$= A + \bar{B} + BC + (B\bar{C} \oplus BC).$$

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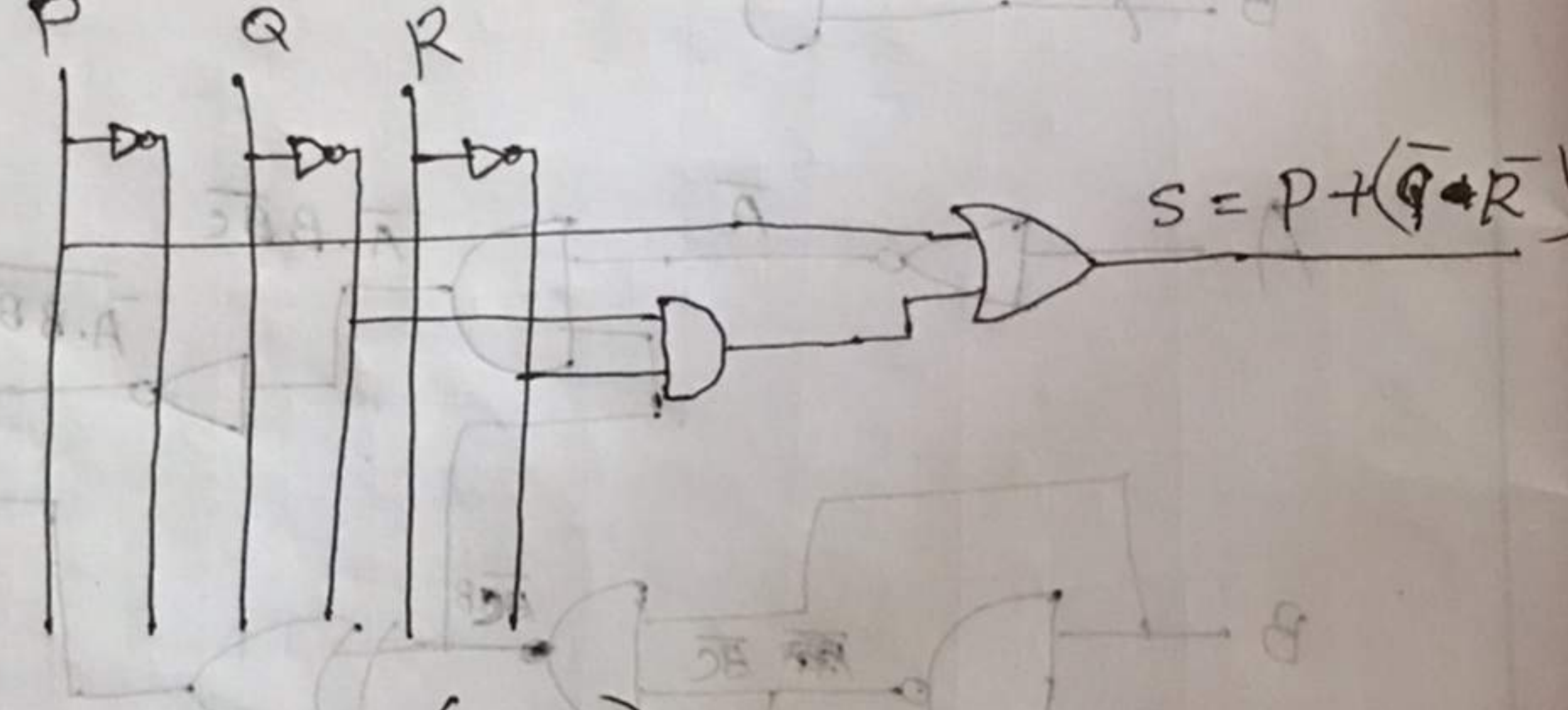
⑨ Design a logic circuit with input P, Q, R so that output S is High whenever P is "1" or whenever Q = R = 0



$$S = P + (\bar{Q} \cdot \bar{R})$$

P	Q	R	$\bar{Q}$	$\bar{R}$	P	$\bar{Q} \cdot \bar{R}$	$S = P + (\bar{Q} \cdot \bar{R})$
0	0	0	1	1	0	1	1
0	0	1	1	0	0	0	0
0	1	0	0	1	0	0	0
0	1	1	0	0	0	0	0
1	0	0	1	1	1	1	1
1	0	1	1	0	1	0	1
1	1	0	0	1	1	0	1
1	1	1	0	0	1	0	1

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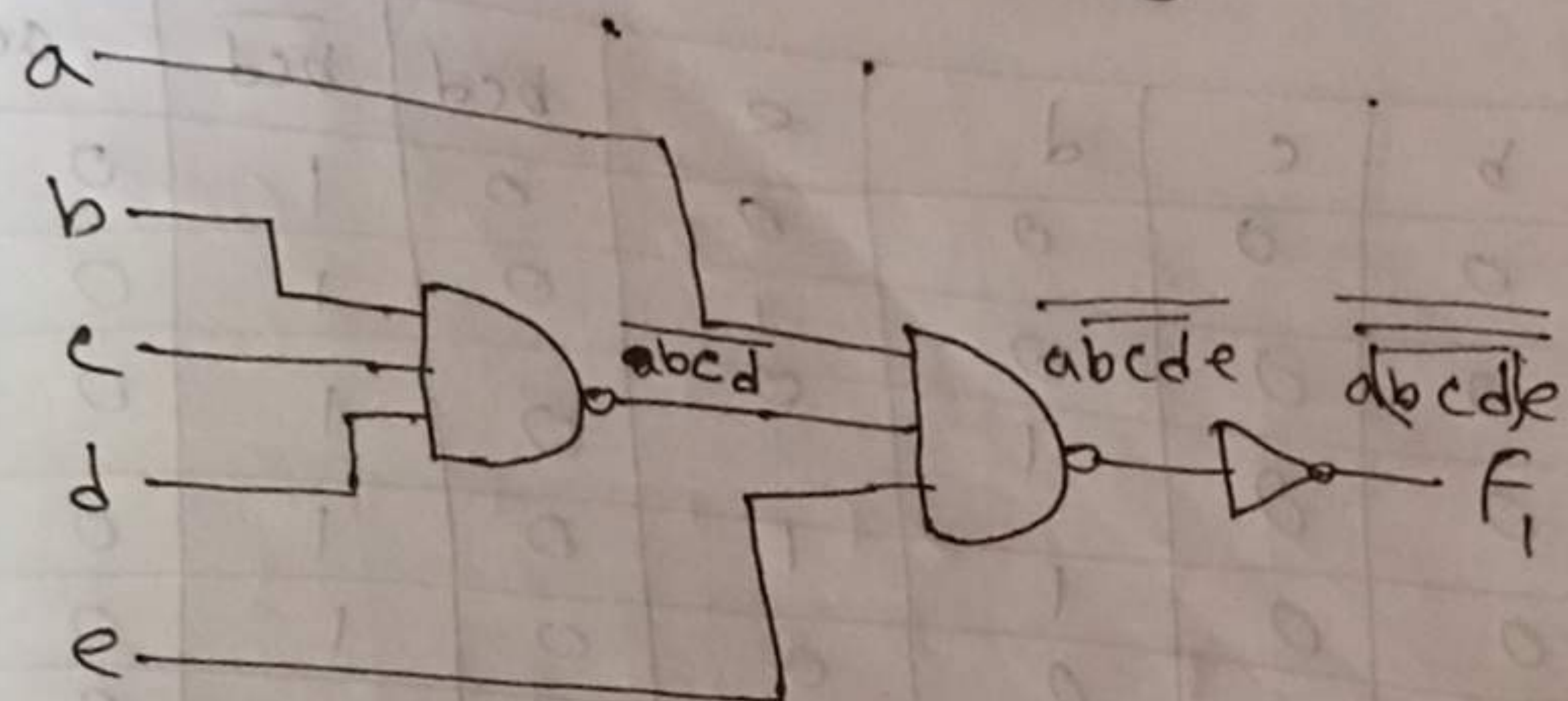
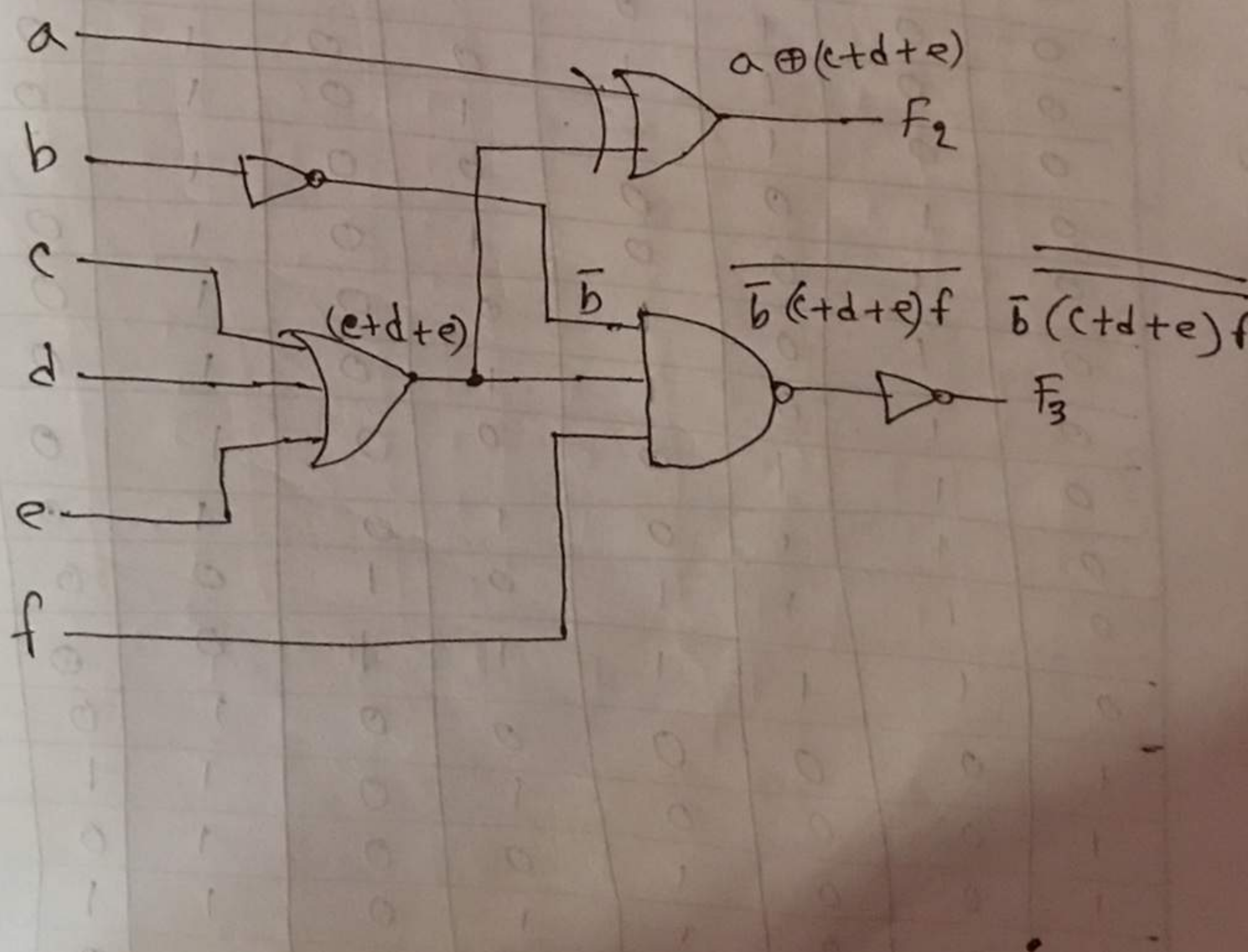
(10) write Boolean expressions and construct the truth tables describing the outputs of the circuits described by the following logic diagrams?





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Date :..................................

$$F_1 = \overline{\overline{a\overline{bcd}e}}$$

$$\Rightarrow F_1 = a\overline{bcd}e = ae\overline{bcd}$$

a	b	c	d	e	bcd	$\overline{bcd}$	ae	$\overline{bcd}ae$
0	0	0	0	0	0	1	0	0
0	0	0	0	1	0	1	0	0
0	0	0	1	0	0	1	0	0
0	0	0	1	1	0	1	0	0
0	0	1	0	0	0	1	0	0
0	0	1	0	1	0	1	0	0
0	0	1	1	0	0	1	0	0
0	0	1	1	1	0	1	0	0
0	1	0	0	0	0	1	0	0
0	1	0	0	1	0	1	0	0
0	1	0	1	0	0	1	0	0
0	1	0	1	1	0	1	0	0
0	1	1	0	0	0	1	0	0
0	1	1	0	1	0	1	0	0
0	1	1	1	0	1	0	0	0
0	1	1	1	1	1	0	0	0
1	0	0	0	0	0	1	0	0
1	0	0	0	1	0	1	1	1
1	0	0	1	0	0	1	0	0
1	0	0	1	1	0	1	1	1
1	0	1	0	0	0	1	0	0
1	0	1	0	1	0	1	1	1

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$F_2 = a \oplus (c+d+e)$

a	c	d	e	$c+d+e$	$a \oplus (c+d+e)$
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	1	1
0	0	1	1	1	1
0	1	0	0	1	1
0	1	0	1	1	1
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	0
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	1	0

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$F_3 = \overline{\overline{\bar{b}\,(c+d+e)\,f}}$

$\Rightarrow F_3 = \bar{b}f\,(c+d+e)$

b	c	d	e	f	$\bar{b}$	$\bar{b}f$	c+d+e	$\bar{b}f(c+d+e)$
0	0	0	0	0	1	0	0	0
0	0	0	0	1	1	1	0	0
0	0	0	1	0	1	0	1	0
0	0	0	1	1	1	1	1	1
0	0	1	0	0	1	0	1	0
0	0	1	0	1	1	1	1	1
0	0	1	1	0	1	0	1	0
0	0	1	1	1	1	1	1	1
0	1	0	0	0	1	0	1	0
0	1	0	0	1	1	1	1	1
0	1	0	1	0	1	0	1	0
0	1	0	1	1	1	1	1	1
0	1	1	0	0	1	0	1	0
0	1	1	0	1	1	1	1	1
0	1	1	1	0	1	0	1	0
0	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	1	0
1	0	0	1	1	0	0	1	0

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(11) Show that a ~~p tha~~ ~~a~~ positive logic NAND gate is a negative logic NOR gate and viceversa.

Definitions:

1) positive Logic: i) Logic Level '1' (true) is represented by a high voltage
ii) Logic Level '0' (false) is represented by a low voltage.

2) negative Logic: i) Logic Level '1' (true) is represented by a low voltage.
ii) Logic Level '0' (false) is represented by a high voltage

NAND gate : $P = \overline{A \cdot B}$

NOR gate : $P = \overline{A + B}$

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NAND gate (positive)

A	B	AB	$\overline{AB}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

In positive, The output is high (1) for all combinations of inputs except when both inputs are high (1)

NOR gate (negative)

A	B	$\overline{A+B}$
1	1	0
1	0	1
0	1	1
0	0	1

In negative, The output is low (0) only when baths inputs are high (1).

For NAND gate in positive logic.

When both inputs are low (0), the output is high (1), and when both inputs are high (1), the output is low (0).

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For NOR gate in Negative Logic:

when both inputs are high(1), the output is low (0), and when both inputs are ~~hig(1)~~, low(0), the output is high (1).

Thus, we can see that a positive logic NAND gate behaves like a negative logic NOR gate and vice versa.

Extra:

AND (positive)

A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

AND (Negative)

A	B	$\overline{AB}$
1	1	1
1	0	1
0	1	1
0	0	0

NAND (positive)

A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

NAND (Negative

A	B	$\overline{AB}$
1	1	0
1	0	0
0	1	0
0	0	1

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OR (positive)

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

OR (negative)

A	B	A+B
1	1	1
1	0	0
0	1	0
0	0	0

NOR (positive)

A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

NOR (Negative)

A	B	$\overline{A+B}$
1	1	0
1	0	1
0	1	1
0	0	1

Dual Form :

গুন থাকলে যোগ।

যোগ থাকলে গুন।

AB (positive) → AB (Negati
or A+B (pos

A+B (positive) → A+B (negative)
or AB (positive)

Subject:
Date:

(12) Show that the dual form of the XOR is also its complement ?

<u>Soln</u> : $x \oplus y = xy' + x'y$

$\text{complement} = (x \oplus y)' = (xy' + x'y)'$

$= \overline{xy' + x'y}$

$= \overline{xy'}\ \overline{x'y}$

$= (x' + y)(x + y')$

$\text{Dual of} = (x \oplus y) = \text{Dual of } (xy' + x'y)$

$= (x + y')(x' + y)$

$= (x' + y)(x + y')$

$\therefore (x \oplus y)' = \text{Dual of } (x \oplus y)$

Subject:
Date:

(13) Implement the following Boolean expression with Exclusive-OR and AND gate?

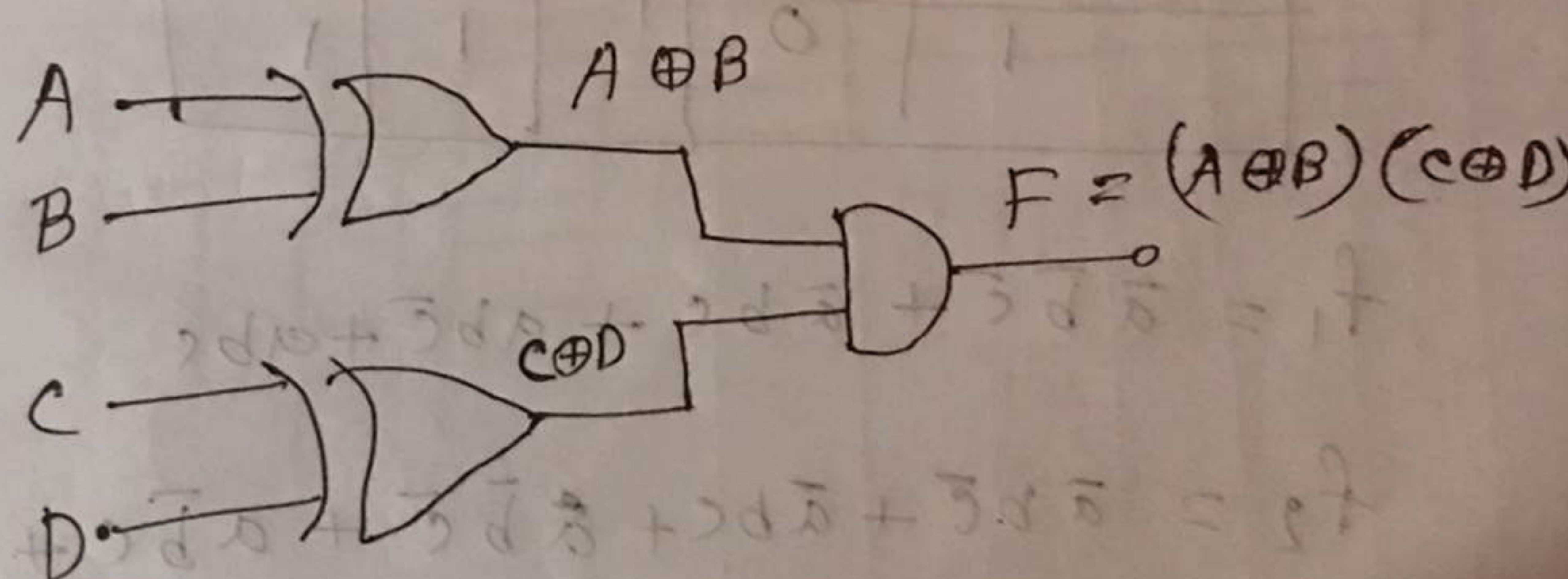
$$F = AB'CD' + A'BCD' + AB'C'D + A'BC'D$$

$$\Rightarrow F = CD'(AB' + A'B) + C'D(AB' + A'B)$$

$$\cancel{\Rightarrow F = (A'B + AB')}$$

$$\Rightarrow F = (AB' + A'B)(CD' + C'D)$$

$$\Rightarrow F = (A \oplus B)(C \oplus D)$$



Subject:

Date :

(19) write the Boolean expression and draw the logic circuit whose outputs are by the following truth table?

f_1	f_2	a	b	c
1	0	0	0	0
0	0	0	0	1
0	1	0	Φ	0
1	1	0	1	1
0	1	1	0	0
0	1	1	0	1
1	1	1	1	0
1	0	1	1	1

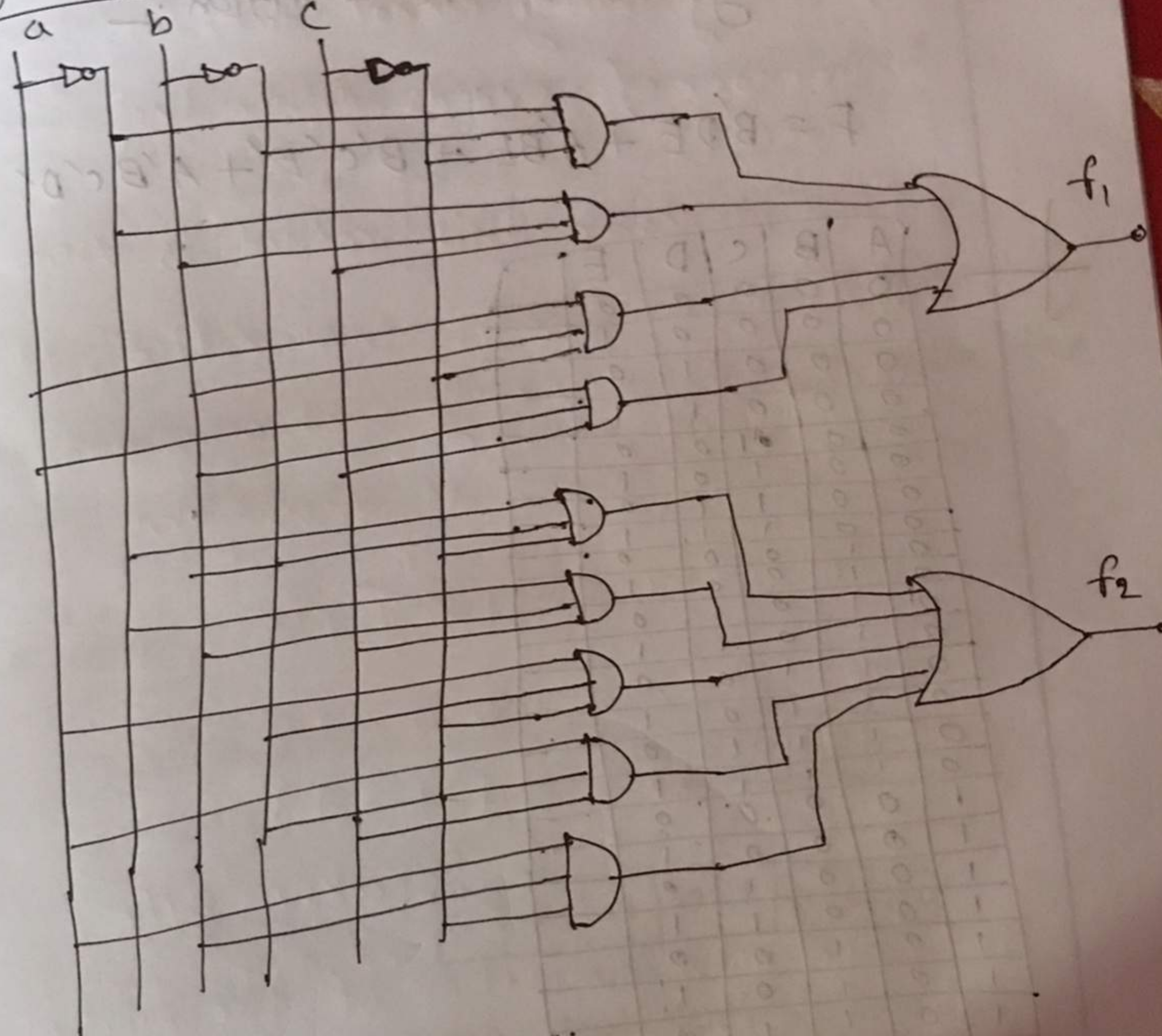
$$f_1 = \bar{a}\bar{b}\bar{c} + \bar{a}bc + ab\bar{c} + abc$$

$$f_2 = \bar{a}b\bar{c} + \bar{a}bc + a\bar{b}\bar{c} + a\bar{b}c + ab\bar{c}$$

Subject:

Date :

Logic Diagram.



data with parity bit.

Extra: K-Map (Don't care conditions)

Simplif the boolean function: $F(w,x,y,z) = \Sigma(1,3,7,11,15)$

$d(w,x,y,z) = \Sigma(0,2,5)$

wx\yz		y	
X	1	1	X
	X	1	
		1	
		1	

z

$$\boxed{F = yz + w'z}$$

[Combining 1's and x's]

NAND gate is a universal gate?

① A universal gate is a gate which can implement any Boolean function without need to use any other gate type. NOR and NAND gate is called universal gates because all the gates (NOT, AND, OR) can be created by using this gate.

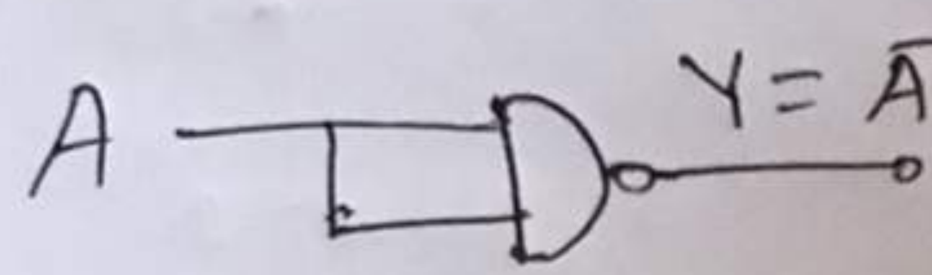
Subject:

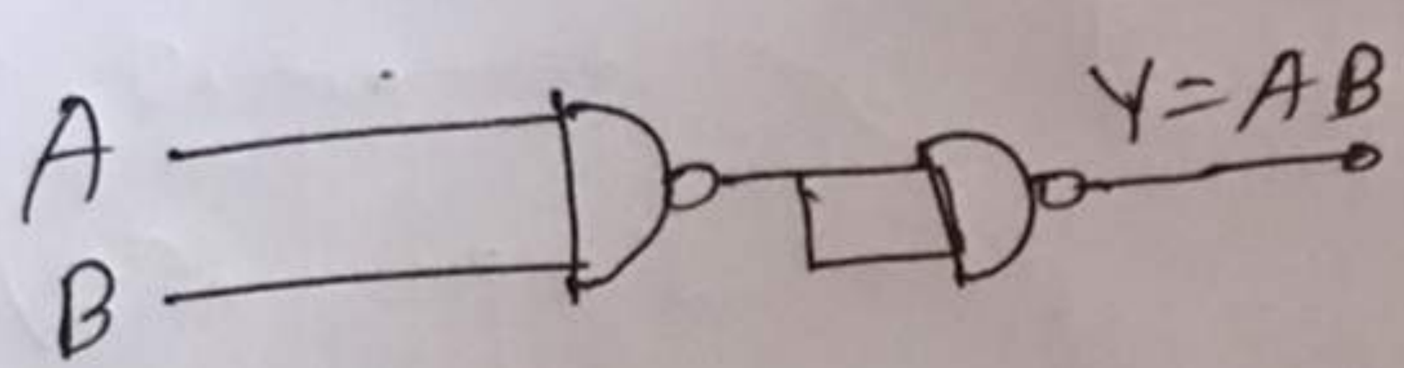
Date :

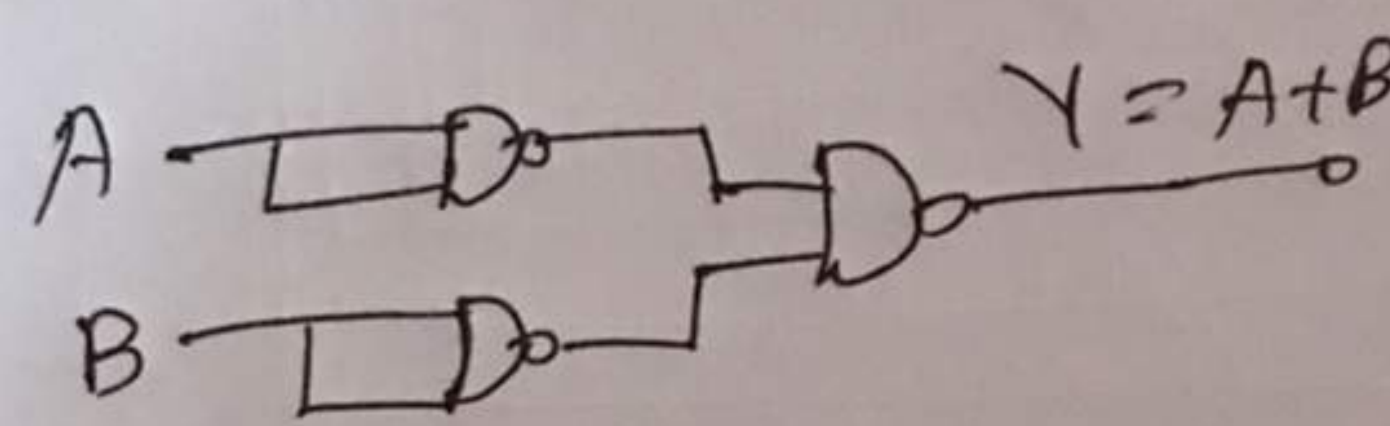
Implement :

NAND

~~NOR~~







NOR