Computer Peripheral & Interfaces (Introduction) **from A Sahu Deptt. of Comp. Sc. & Engg. IIT Guwahati**

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Outline

- Introduction
- Linux Kernel Split View
- Motivation
- Dolby Digital
- HD Cinema
- MI TECH 2010: Nvidia GPUs
- MI Tech 2010: USB 3.0
- MI Tech 2010: Bluetooth 4.0
- Peripherals Controller Migratio
- Why Migration?
- Moorestown Platform
- Intel Centrino Processor
- Intel Atom Processor

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Introduction

Computer system

1. Internal {Processor and Memory(RAM)}
2. Peripheral (Disk, Display, Audio System, Ethernet Card)

Interface:

- connects Internal and peripheral devices.
- Two Types:

Intermediate Hardware: Nvdia GPU Card, Creative Sound Blaster

Intermediate Software: Nvdia GPU Driver, Sound Blaster Driver Software

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Introduction

More Examples

Intermediate Hardware

- Timer: Measures time intervals.
- Counter: Counts the number of events
- DMA (Direct Memory Access): directly access memory
- USB (Universal Serial Bus): Used for connection, communication and power supply
- UART (Universal Asynchronous Receiver/Transmitter): Handle asynchronous serial communication.
- Peripheral Controller: Manages peripheral devices.

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Introduction

More Examples

Intermediate Software/Programs

- Device Driver (Linux): A specific type of software that allows the operating system to control hardware.
- Assembly Code: Low level programming language

Peripheral Component Interconnect (PCI):

- Audio card
- VGA (Video Graphic Array) card
- Ethernet Card

Low level signal + high level C code (Combination of these two helps the interface to control hardware)

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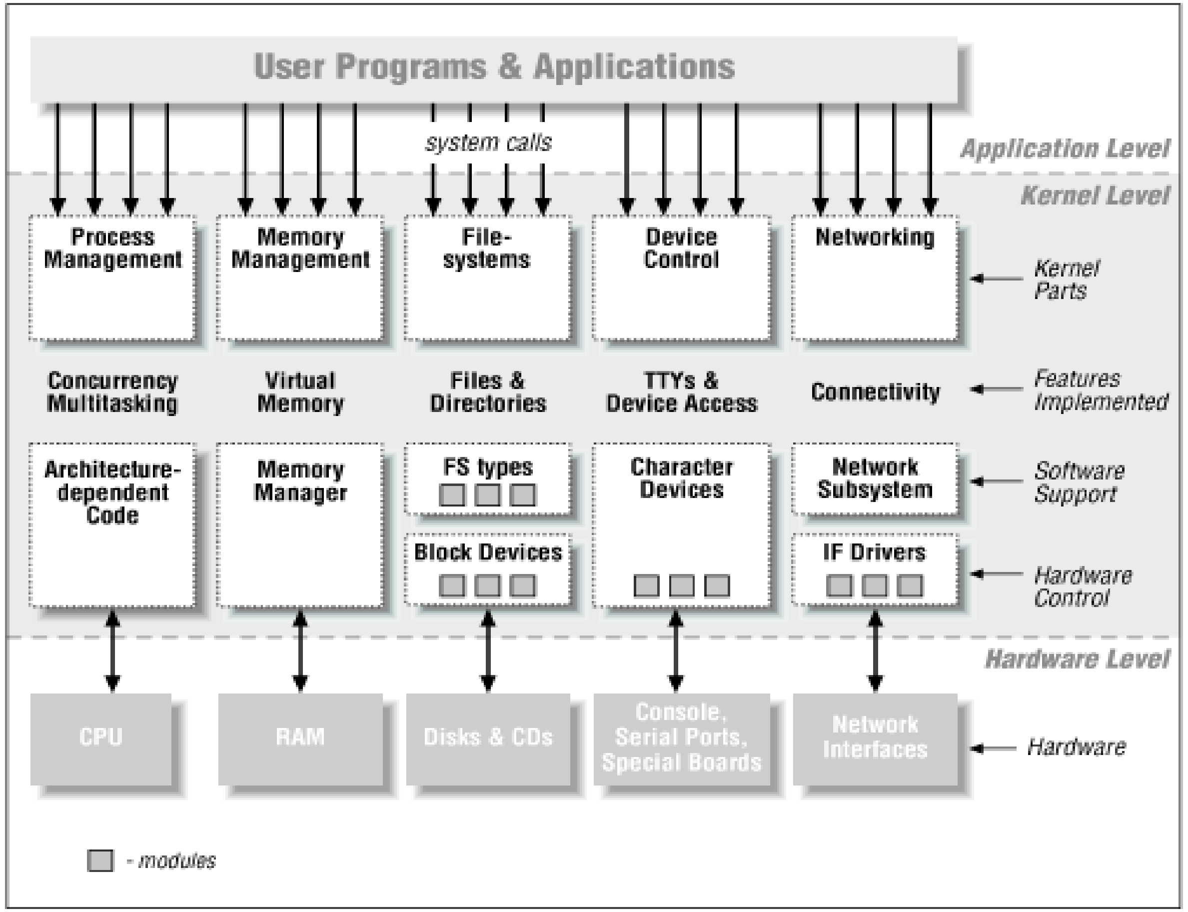
Linux Kernel Split View

In a Unix system, several concurrent processes attend to different tasks. Each process asks for system resources, be it computing power, memory, network connectivity, or some other resource. The kernel is the big chunk of executable code in charge of handling all such requests. Though the distinction between the different kernel tasks isn't always clearly marked, the kernel's role can be split, as shown in Figure



A split view of the kernel

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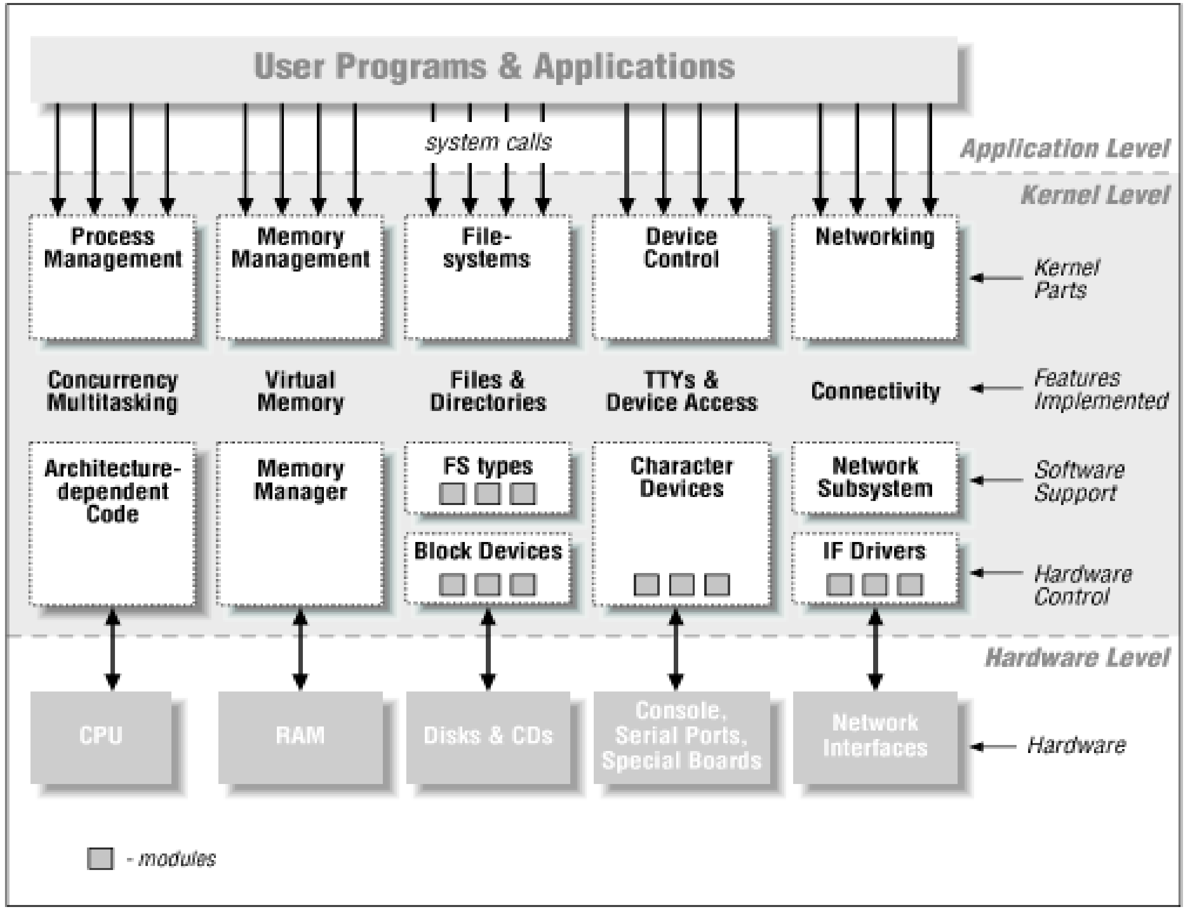
Linux Kernel Split View

These 5 parts of Kernel split execute various roles.

1. **Process management**
2. **Memory management**
3. **Filesystems**
4. **Device control**
5. **Networking**



A split view of the kernel

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Motivation

1. **Knowledge: both hardware & software**

Hardware		Software	
Internal	External(Peripheral)	System	Application
Motherboard, CPU, RAM, Hard Drive	Mouse, Keyboard, Microphone	Operating System, Language Processor, Device Driver	Web browser, facebook, Instagram etc

2. **Exact interface: Architecture & OS**

Architecture	OS
• Von-Neumann Architecture • Harvard Architecture • Instruction Set Architecture	Windows, linux , macOS, Unix, Android etc

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Motivation

3. Used in many places (Computer +Embedded System

- An embedded system

A specialized computer designed to perform specific tasks within a larger device or system, like controlling a washing machine or a car's engine.

4. Highly paid job in industries

Intel | NVIDIA | IBM

5. Low level signal + Device drivers

Low level signal	Device drivers
directly control hardware components	enable the operating system to communicate with and control hardware devices.
0 or 1, High voltage or Low voltage	

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Motivation

6. Knowledge of simple peripherals

(Display, Audio, Disk drives, Ethernet) In connection with 8085/8086

Display	Audio	Disk Drivers	Ethernet
memory-mapped I/O , port-mapped I/O	PWM (Pulse Width Modulation) signals	programmed I/O or DMA	transmitted/received via I/O ports or memory-mapped registers
7-segment displays or CRTs		floppy disk controller (FDC)	Intel 82586

7. Peripheral are powerful than main computing

Advanced Peripherals & Technologies

- Linux/Windows Device Drivers.
- Dolby Digital Stereo, HD Cinema, Dolby Atmos (present), USB 3.0, USB 4.0 (present).
- Graphics cards (Nvidia with 480 core) , RTX (Ray Tracing eXtreme)- 40 series, GTX (Giga Texel Shader eXtreme)-16 series by NVIDIA (present).

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Motivation

8. Use of old technology in newer devices

- Intel Atom processor (PII technology with modification)
- Use of winXP in mobile; may be obsolete for PC in very short

9. Combining peripheral controller in main computing for low power

1. Intel Centrino have wireless controller functionality inside processor chip
2. Intel atom 45x have DDR2 memory controller + Graphics controller in inside processor chip in very short

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Dolby Digital

Dolby digital audio placement technology can deliver high-quality audio even at lower bitrates and realistic surround sound compared to plain audio

Dolby Stereo:

- It is a unified brand for two completely different basic systems: the Dolby SVA (stereo variable-area) 1976 system used with optical sound tracks on 35mm film, and Dolby Stereo 70mm noise reduction on 6-channel magnetic soundtracks on 70mm prints.
- Humans have two eyes to measure the depth of image which can be called a stereo image.

Stereo Ear Phone

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Dolby Digital

Dolby Lab:

- It supports up to 5.1 channels of surround sound.
- It can deliver more directional sound effects than stereo audio.
- 5 ear-level speakers & 1 subwoofer. 5 channels have 20 Hz – 20,000 Hz.1 channel have 20 Hz – 120 Hz.
- 5 ear-level channels are 3 front channel (Left, Center, Right) provide clean dialogue & accurate placement of on-screen sounds & the 2 surround channels (Left surround, Right surround)
- Low Frequency channel (LFE) called ".1 channel," delivers deep, powerful bass effects that can be felt as well as heard.
- Max bit rate: 560 bit/s

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Dolby Digital

Dolby HD:

- It supports up to 7.1 channels of surround sound.
- 7 ear-level speakers & 1 subwoofer.
- Max bit rate:18MB/s

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HD Cinema

Video specification:

- Frame rate . 30 frames/sec
- 1 Hour video size (Based on resolution) .
  - VGA (Video Graphic Array) (640 x 480) pixels: Uncompressed size: 199 GB, Compressed size: 450 MB
  - 720P (1280 × 720) pixels Uncompressed size: 597 GB Compressed size: 1.2 GB
  - 1080P/i(1920 × 1080) pixels Uncompressed size: 1.35 TB Compressed size: 2.4 GB

File formats:

- MP2: Typically used for DVD & broadcasting. It is an older but reliable format.
- MP4: One of the most common video formats, ideal for streaming.
- MKV: It can contain multiple audio, video, subtitle tracks, all within a single file. It's often referred to as a 'Matryoshka' or 'Nested doll'.

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HD Cinema

Cinema resolution:

- Old 2k(2048×1080): It is used in digital cinema, specially for older or low budget production.
- New 4k(4096×2160): It is standard for high end digital cinema offering extremely high video quality.

Projection technologies :

- Digital Light Processing (DLP): It is developed by Texas Instruments. This technology uses micro-mirrors to project images. It is widely used in projectors, including cinema projectors for bright & vivid images.

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HD Cinema

Projection technologies :

- **Liquid Crystal on Silicon (LCOS):** It is a reflective display technology that allows rapid switching of light for display projection purposes. It is a better version than LCD & DLP technology. It produces very bright & high resolution images used in large high definition screens.

- **Silicon X-tal Reflective Display (SXRD):** It is the evolution of LCOS technology, developed by Sony. It offers high resolution & contrast, used in high end projectors & cinema display

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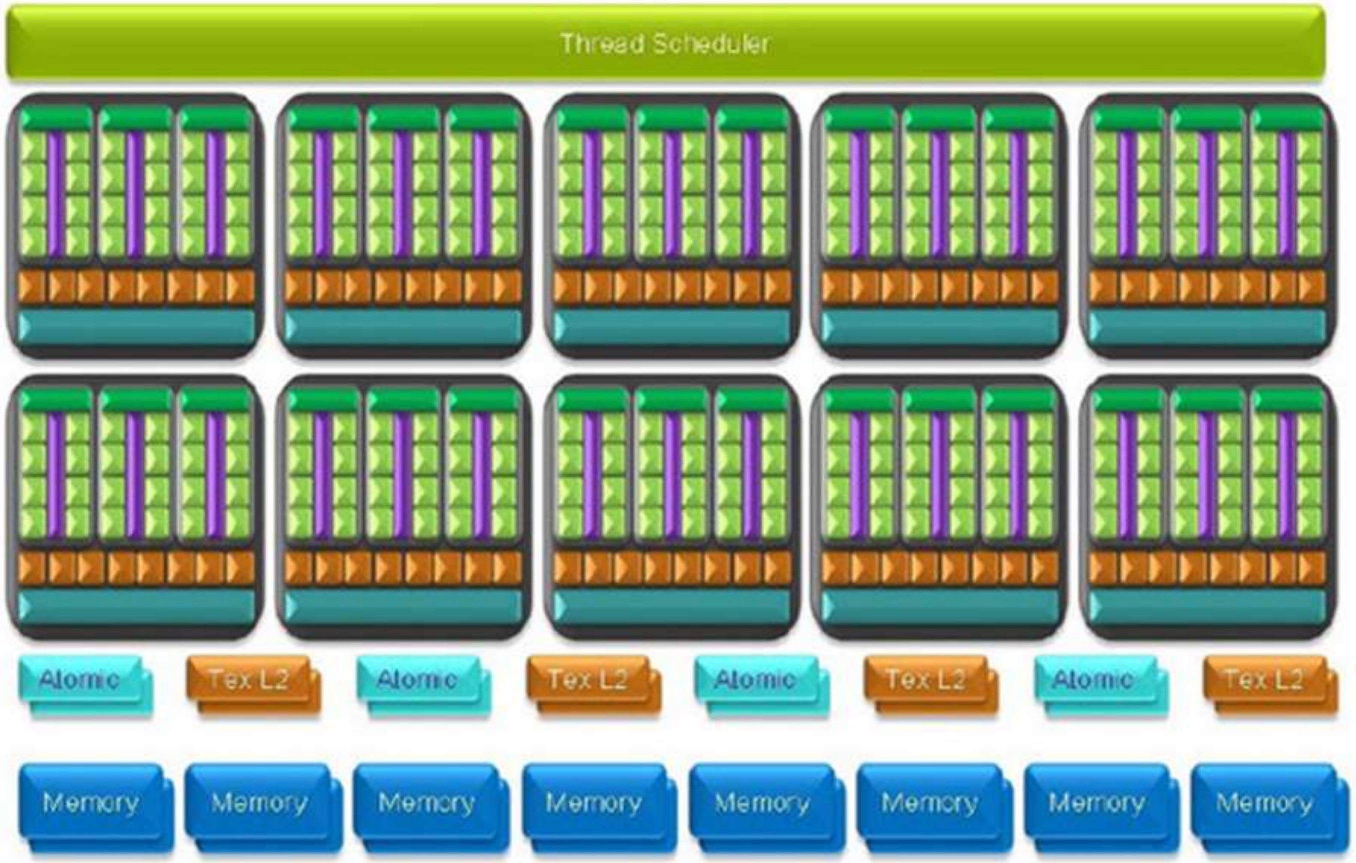
MI TECH 2010: Nvidia GPUs

Nvidia GPUs are powerful graphics processing units designed primarily for rendering images, videos, and animations for display



Structure:

- **CUDA (Compute Unified Device Architecture) Cores:** The grid-like structure in the diagram represents CUDA cores, which are parallel processing units within the GPU.

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MI TECH 2010: Nvidia GPUs

- **Thread Scheduler:** The green bar at the top labeled "Thread Scheduler" is responsible for managing and dispatching tasks (threads) to the CUDA cores.
- **Atomic Units** (in light blue) are responsible for managing operations that require access to shared memory without interference from other processing threads, ensuring data consistency.

- **Tex L2** (Texture Level 2) units (in orange) handle texture data, which is used in rendering images and graphics.
- **Memory:** The blocks labeled "Memory" (in blue) represent the GPU's memory,

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MI TECH 2010: Nvidia GPUs

Key Features:

- **Nvidia GTX295**: Equipped with 480 CUDA cores, which are parallel processors used for tasks such as rendering graphics, computational simulations, and other data-intensive tasks.
- **VGA (Video Graphics Array):** Capable of supporting resolutions up to 2048x1536. Supports dual-monitor setup, providing flexibility for multiple displays.
- **HD Cinema & MKV File Playback**: Supports high-definition cinema viewing and can play MKV files, which are commonly used for high-quality video storage.

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MI Tech 2010: USB 3.0

USB 3.0 is a major upgrade over previous USB versions, offering significantly faster data transfer speeds and better efficiency in handling devices connected to computers.

Key Features:

- **SuperSpeed Bus: USB 3.0** introduced the "SuperSpeed" mode, which allows for much faster data transfer compared to USB 2.0..
- **Enhanced Host Controller Interface (EHCI):** With USB 3.0, the EHCI was enhanced to support higher speeds and better performance.
  - **Register-level Interface:** Maintains compatibility with older USB 2.0 devices while also supporting the new features of USB 3.0.
  - **SATA HDD Integration:** USB 3.0 could work with SATA hard drives, allowing for faster data transfers, particularly for external storage devices.
- **Transfer Mode:** USB 3.0 supports transfer speeds up to **5.0 Gbit/s**, which is roughly **400 MB/s.** The previous version speed was 480 Mbit/s.

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MI Tech 2010: USB 3.0

Technical Aspects:

- **8B/10B Encoding**: A method of encoding data to ensure reliable transmission by balancing the number of 1s and 0s sent over the cable.
- **Linear Feedback Shift Register (LFSR) Scrambling**: This technique helps in reducing electromagnetic interference, which can affect the quality of data transmission.
- **Spread Spectrum**: This is used to spread the signal over a wider bandwidth, which also helps in reducing interference and improves signal integrity.
- **Receivers and Equalization**: Advanced receivers in USB 3.0 include mechanisms for periodic signaling and dynamic equalization, ensuring that data is accurately received and processed, even in challenging conditions.

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MI Tech 2010: Bluetooth 4.0

Bluetooth 4.0, introduced in 2010, marked a significant advancement in wireless communication technology, offering improved features like higher data transfer rates, lower power consumption, and enhanced connectivity options.

Key Features:

1. **Classic Bluetooth**: Operates at a frequency of 2.4 GHz using Frequency Hop Spread Spectrum (FHSS). Offers a typical range of about 1 meter and data transfer rates of up to 3 MB/s.
2. **Bluetooth High Speed**: This feature is based on Wi-Fi technology, allowing for much faster data transfer rates than previous versions of Bluetooth. Ideal for applications requiring quick data exchange.
3. **Bluetooth Low Energy (BLE):** A major addition in Bluetooth 4.0, BLE is designed for devices that need to operate on very low power.

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Peripherals Controller Migration

Overview

- What do meant by peripherals controller migration
- Why is the Peripherals Controller Migration necessary

- Architecture of the Moorestown platform
- Intel Centrino Processor and Intel Atom Processor with functionality

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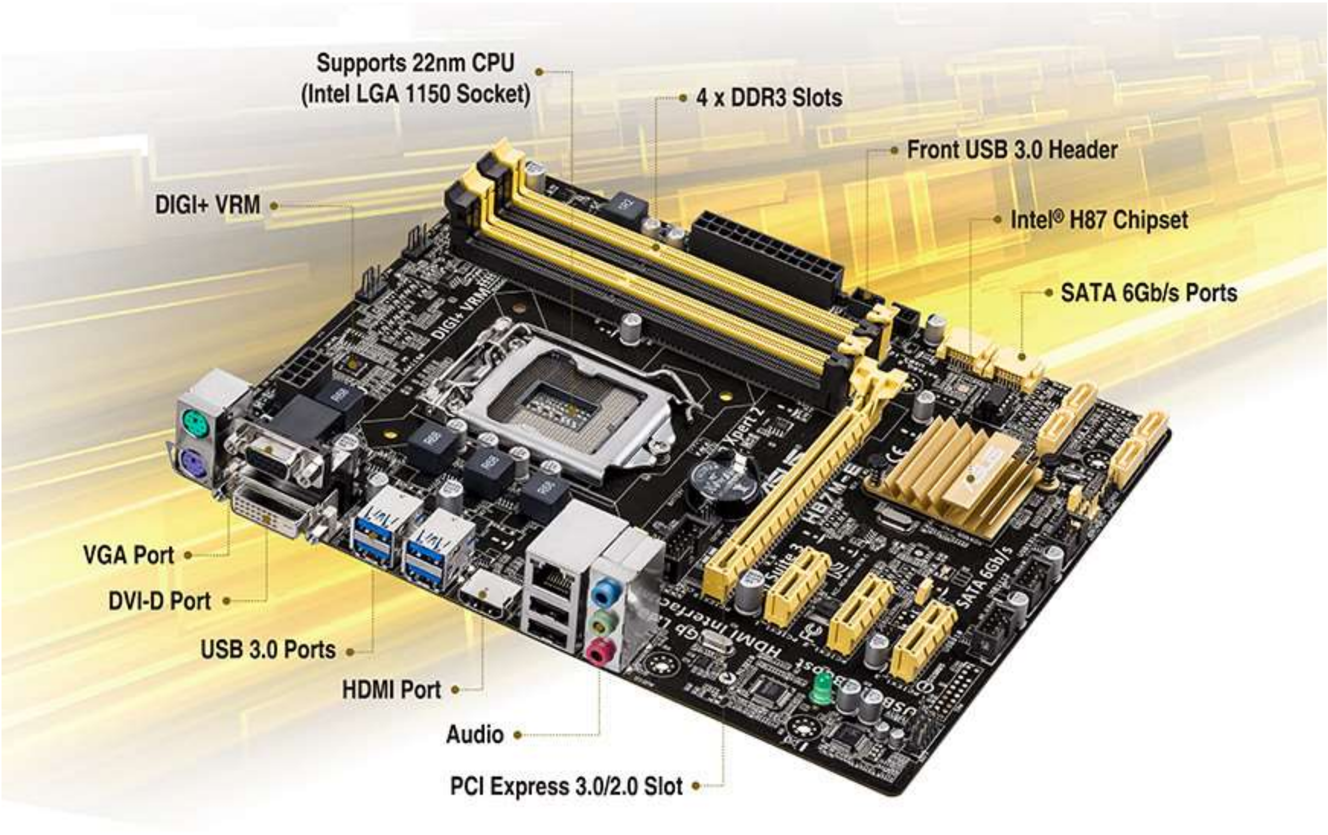
Peripherals Controller Migration

- ✓ **Cards on motherboard**
  - ❖ Graphics
  - ❖ Audio
  - ❖ Modem
- ✓ **Onboard**
- ✓ **Inside Processor**
  - ❖ Graphics
  - ❖ Memory Controller



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Why Migration?

Key Aspects :

- ✓ Hardware Upgrade
- ✓ Platform or Architecture Shift like x86-based system to ARM based system
- ✓ Consolidation

Why Important?

- ✓ Performance Improvement: Offer better performance, more features, or support for newer peripherals.
- ✓ Cost Efficiency: Can more efficient use of system resources.
- ✓ Compatibility: Older controllers may no longer support new peripherals, necessitating a migration to maintain compatibility.

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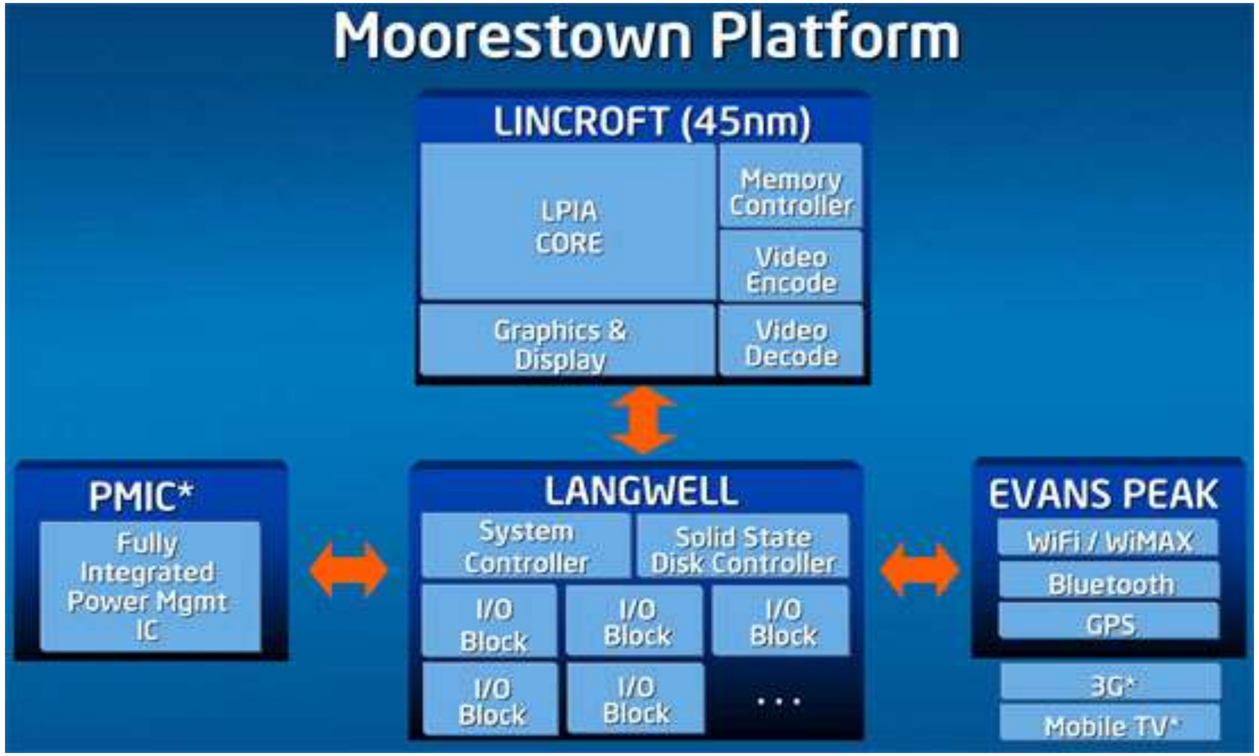
Moorestown Platform

- **Lincroft System on a Chip (SoC):** It features a LPIA (Low Power Intel Architecture) CPU core (Silverthorne derivative), on-die graphics and on-die memory controller.
- **Langwell South Hub :** Langwell is composed of a system controller, solid state disk controller and I/O blocks for things like USB or audio.



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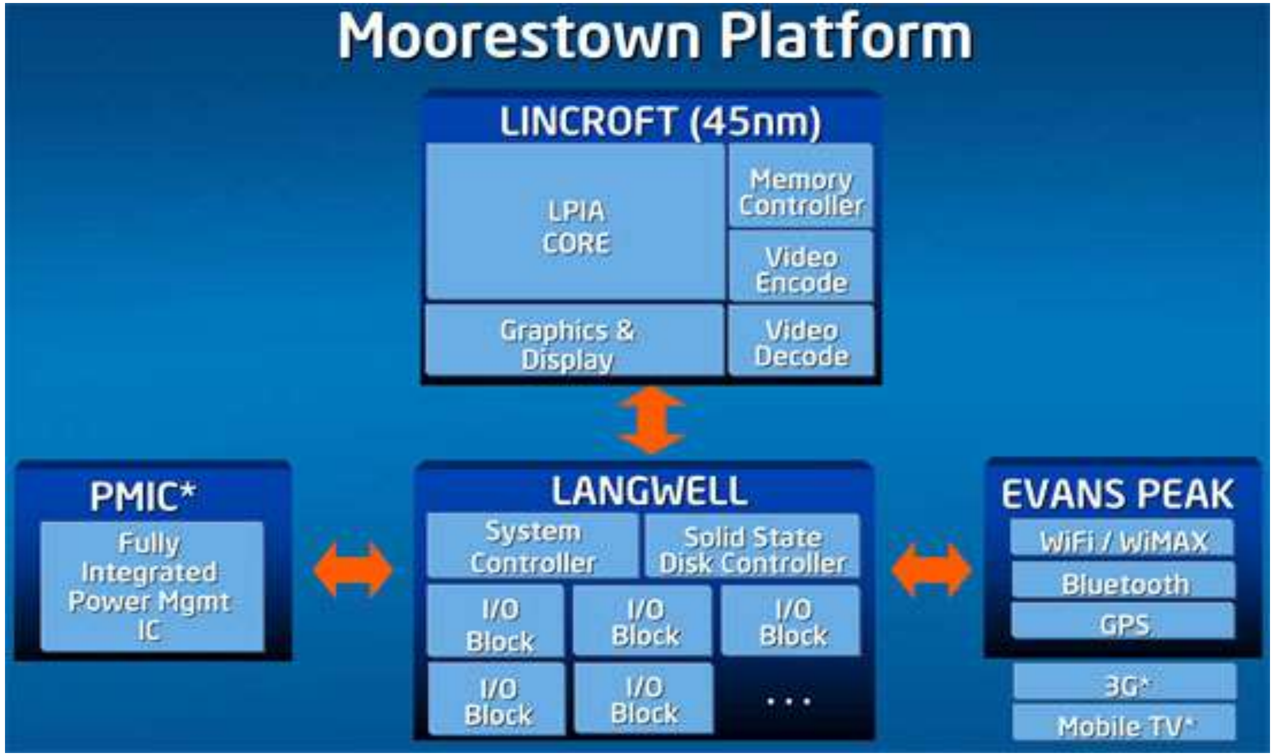
Moorestown Platform

- **PMIC** : The Power Management IC (PMIC) plays a mystery role at this point. Intel is just revealing that it handles power management for the platform yet not fully detailing its active roles.
- **Evans Peak Networking**: The final component of Moorestown is the Evans Peak networking hub, which is made up of Intel and non-Intel silicon.



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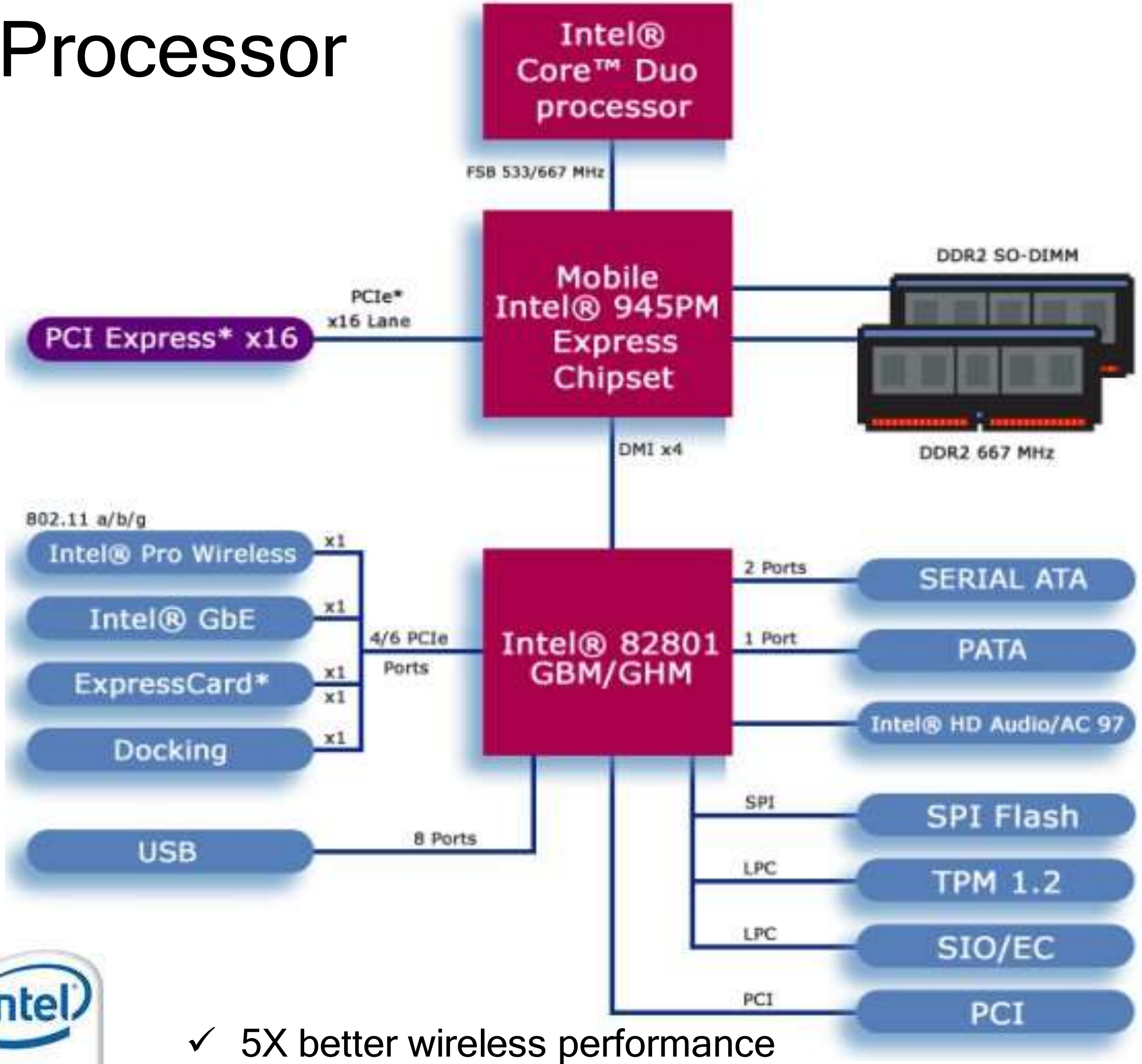
Intel Centrino Processor

PCI Express* x16 Interface: Supports the latest high-performance graphics cards.

Intel High Definition (HD) Audio: Integrated audio support enables premium sound and delivers advanced features such as multiple audio streams.



- ✓ 5X better wireless performance
- ✓ Longer Battery Life

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Intel Atom Processor

- ✓ Old Pentium architecture with modification (Low power addition) : 10Watt
- ✓ Inside processor chip
  - ➢ Graphics processor, Memory controller
  - ➢ Wireless controller (Centrino Atom)

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Thank You!!

We Are Looking For Questions.

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Review of Computer Architetcure

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Outline

- Computer organization Vs Architecture
- Processor architecture
- Pipeline architecture
  - Data, resource and branch hazards
- Superscalar & VLIW architecture
- Memory hierarchy
- Reference

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Computer organization Vs Architecture

Comp Organization => Digital Logic Module

Logic and Low level

=====================

Comp Architecture = > ISA Design, MicroArch Design

Algorithm for

- Designing best micro architecture,
- Pipeline model,
- Branch prediction strategy, memory management
- Etc…..

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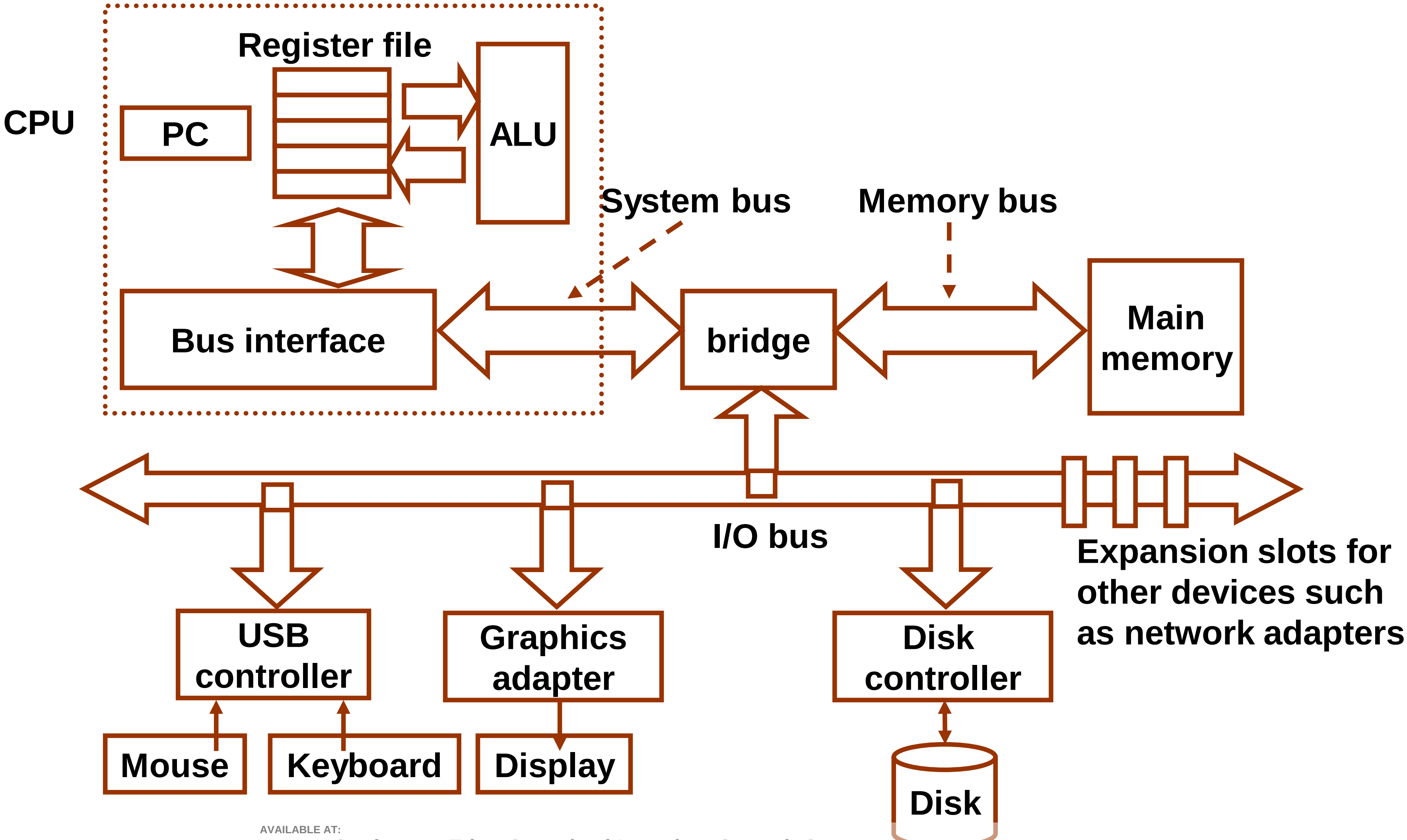
Hardware abstraction



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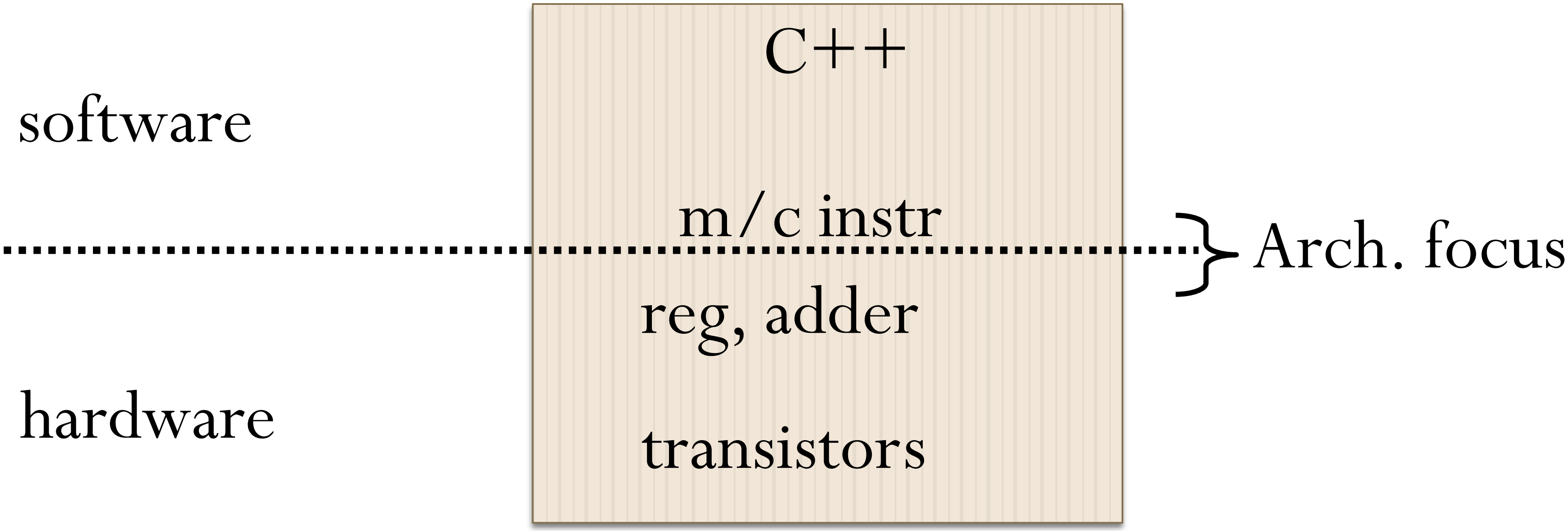
Hardware/software interface



- Instruction set architecture
  - Lowest level visible to a programmer
- Micro architecture
  - Fills the gap between instructions and logic modules

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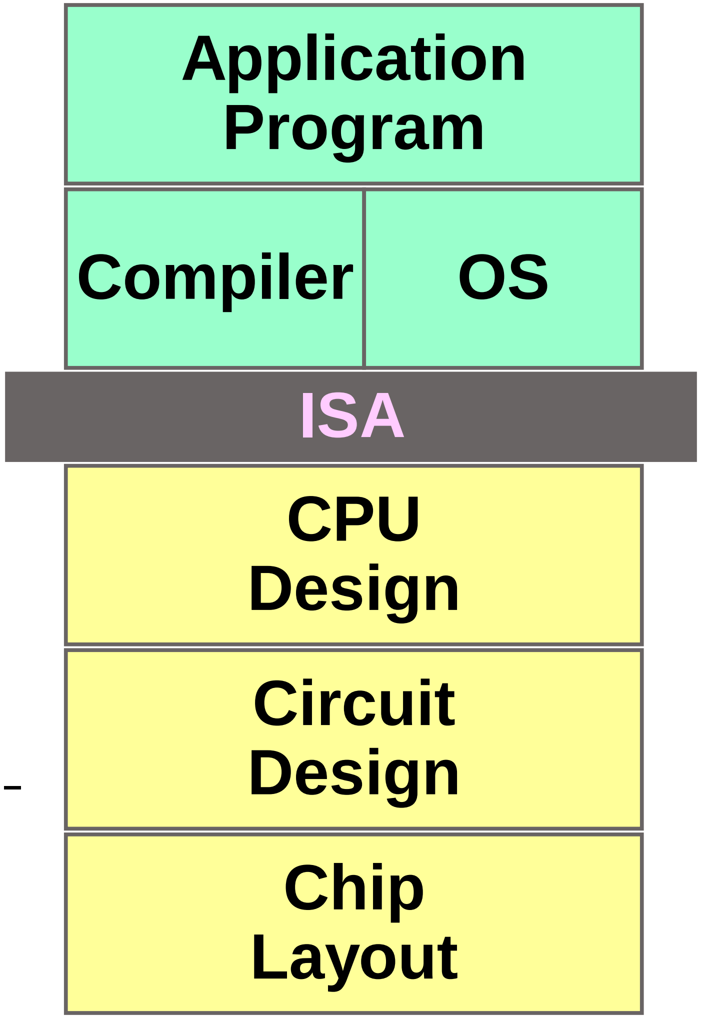
Instruction Set Architecture

- Assembly Language View
  - Processor state (RF, mem)
  - Instruction set and encoding
- Layer of Abstraction
  - Above: how to program machine - HLL, OS
  - Below: what needs to be built - tricks to make it run fast



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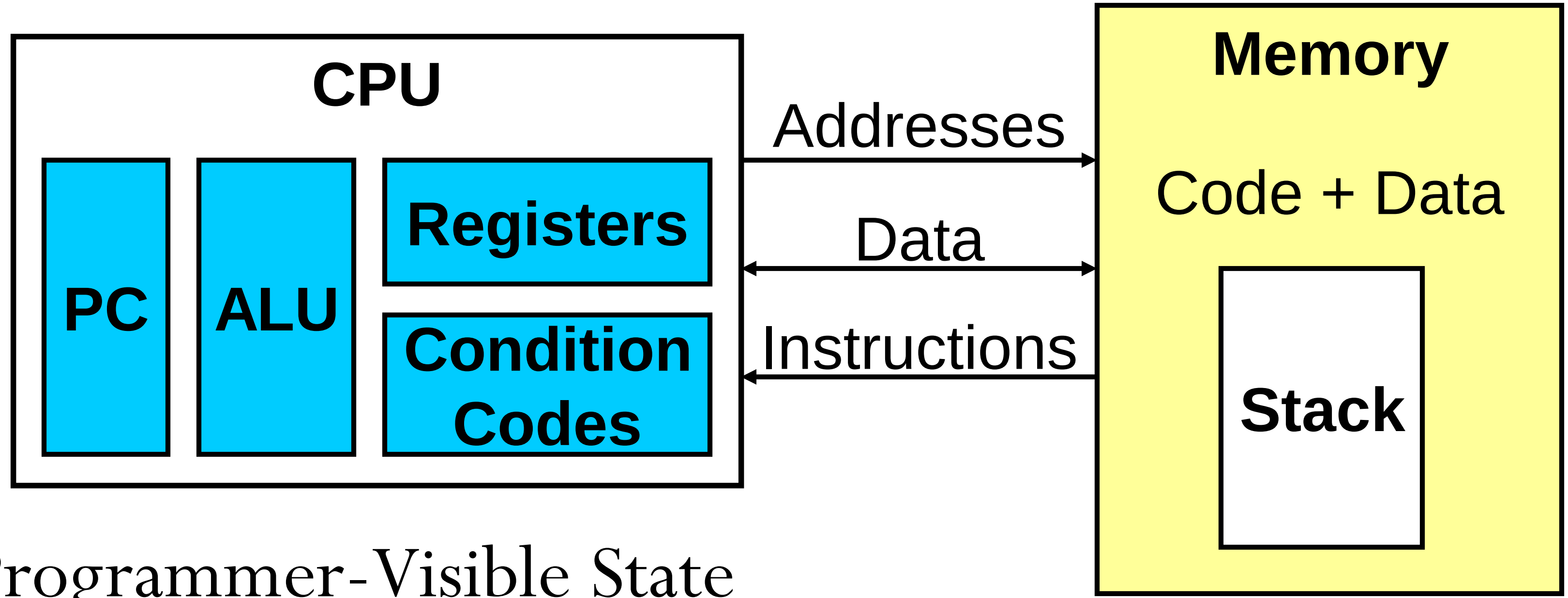
The Abstract Machine



- Programmer-Visible State
  - PC Program Counter
  - Register File
    - heavily used data
  - Condition Codes

- Memory
  - Byte array
  - Code + data
  - stack

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Instructions

- Language of Machine
- Easily interpreted
- primitive compared to HLLs

- Instruction set design goals
  - maximize performance,
  - minimize cost,
  - reduce design time

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Instructions

- All MIPS Instructions: 32 bit long, have 3 operands
  - Operand order is fixed (destination first)

    Example:

    C code: A = B + C

    MIPS code: add $s0, $s1, $s2

    (associated with variables by compiler)

- Registers numbers 0 .. 31, e.g., $t0=8,$t1=9,$s0=16,$s1=17 etc.
- 000000 10001 10010 01000 00000 100000

  op rs rt rd shamt funct

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Instructions LD/ST & Control

- **Load and store instructions**
- **Example:**

C code:	*A[8] = h + A[8];*
MIPS code:	**lw $t0, 32($s3)**
	add $t0, $s2, $t0
	sw $t0, 32($s3)

- **Example: lw $t0, 32($s2)**

35	**18**	**9**	**32**
op	**rs**	**rt**	**16 bit number**

- **Example:**

if (i != j)		**beq $s4, $s5, Lab1**
h = i + j;		**add $s3, $s4, $s5**
else		**j Lab2**
h = i - j;	**Lab1:**	**sub $s3, $s4, $s5**
	Lab2:	**...**

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What constitutes ISA?

- **Set of basic/primitive operations**
  - Arithmetic, Logical, Relational, Branch/jump, Data movement
- **Storage structure – registers/memory**
  - Register-less machine, ACC based machine, A few special purpose registers, Several Gen purpose registers, Large number of registers
- **How addresses are specified**
  - Direct, Indirect, Base vs. Index, Auto incr and auto decr, Pre (post) incr/decr, Stack
- **How operand are specified**
  - 3 address machine $r1 = r2 + r3$, 2 address machine $r1 = r1 + r2$
  - 1 address machine $Acc = Acc + x$ (Acc is implicit)
  - 0 address machine add values on (top of stack)
- How instructions are encoded

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RISC vs. CISC

- **RISC**
  - Uniformity of instructions,
  - Simple set of operations and addressing modes,
  - Register based architecture with 3 address instructions
- **RISC: Virtually all new ISA since 1982**
  - ARM, MIPS, SPARC, HP's PA-RISC, PowerPC, Alpha, CDC 6600
- **CISC :** Minimize code size, make assembly language easy

  VAX: instructions from 1 to 54 bytes long!

  Motorola 680x0, Intel 80x86

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MIPS subset for implementation

- Arithmetic - logic instructions
  - add, sub, and, or, slt
- Memory reference instructions
  - lw, sw
- Control flow instructions
  - beq, j

Incremental changes in the design to include other instructions will be discussed later

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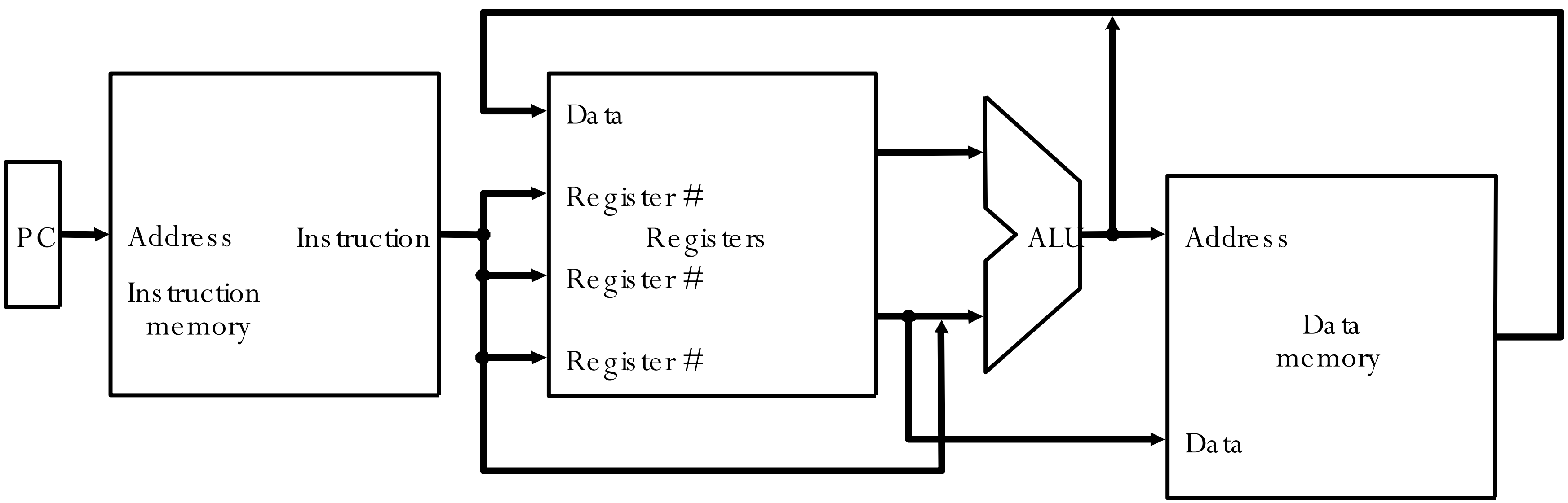
Design overview

- Use the program counter (PC) to supply instruction address
- Get the instruction from memory
- Read registers
- Use the instruction to decide exactly what to do



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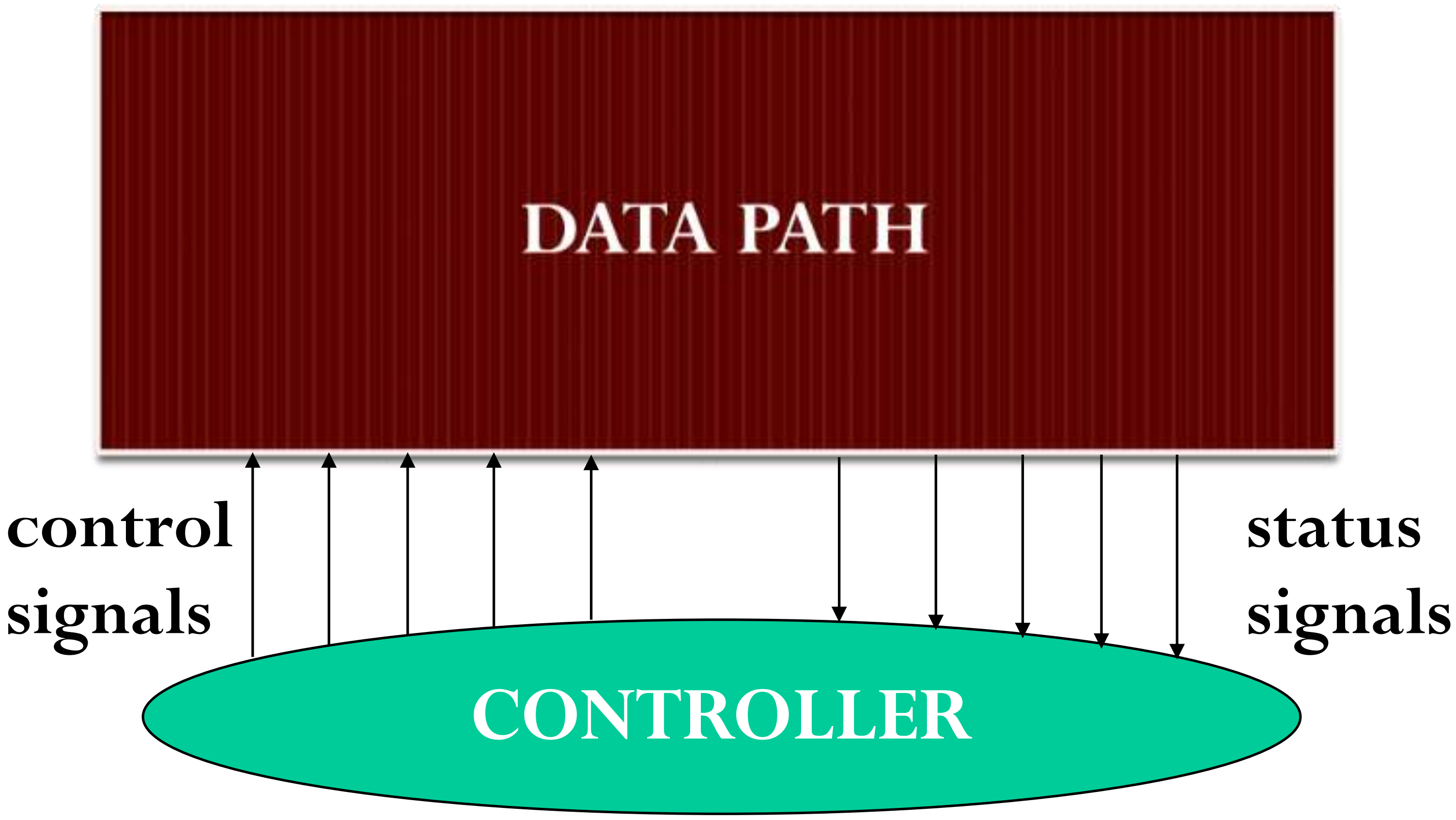
Division into data path and control



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Building block types

Two types of functional units:

- elements that operate on data values (combinational)
  - output is function of current input, no memory
  - Examples
    - gates: and, or, nand, nor, xor, inverter ,Multiplexer, decoder, adder, subtractor, comparator, ALU, array multipliers
- elements that contain state (sequential)
  - output is function of current and previous inputs
  - state = memory
  - Examples:
    - flip-flops, counters, registers, register files, memories

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Components for MIPS subset

- Register,
- Adder
- ALU
- Multiplexer
- Register file
- Program memory
- Data memory
- Bit manipulation components

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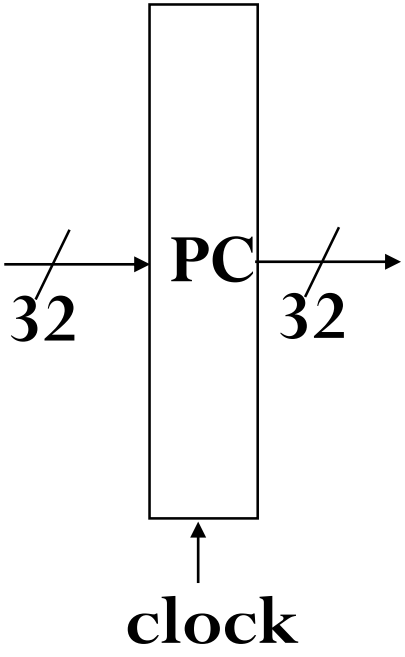
Components - register



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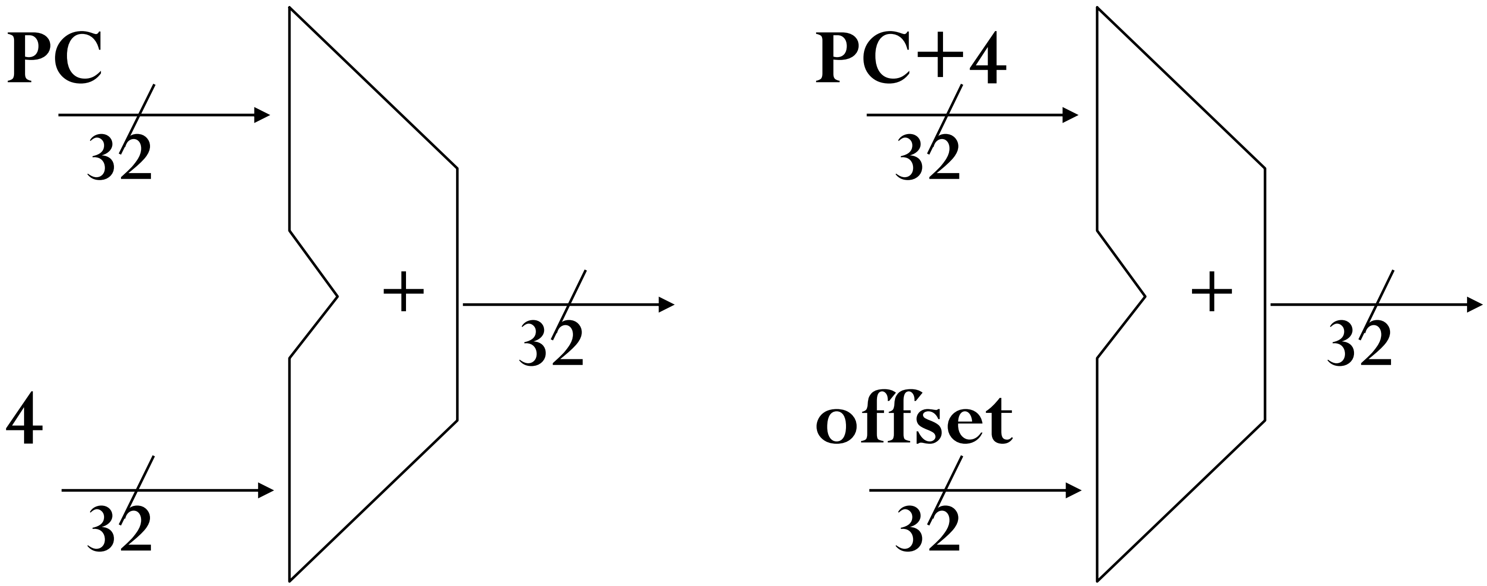
Components - adder



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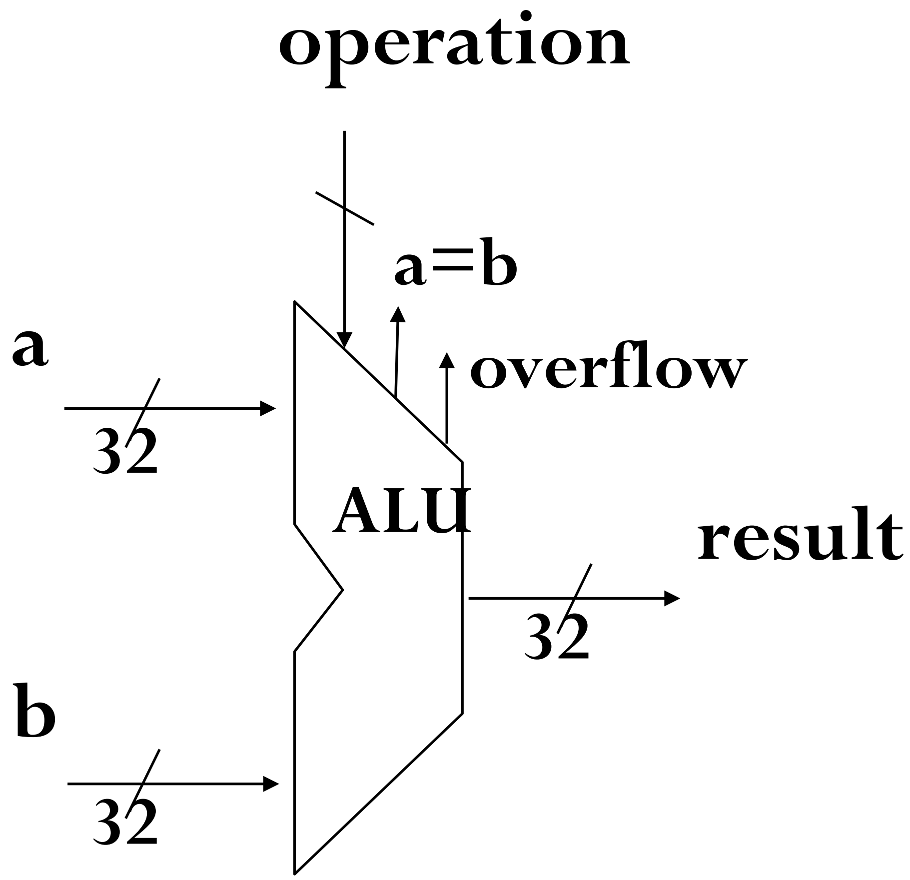
Components - ALU



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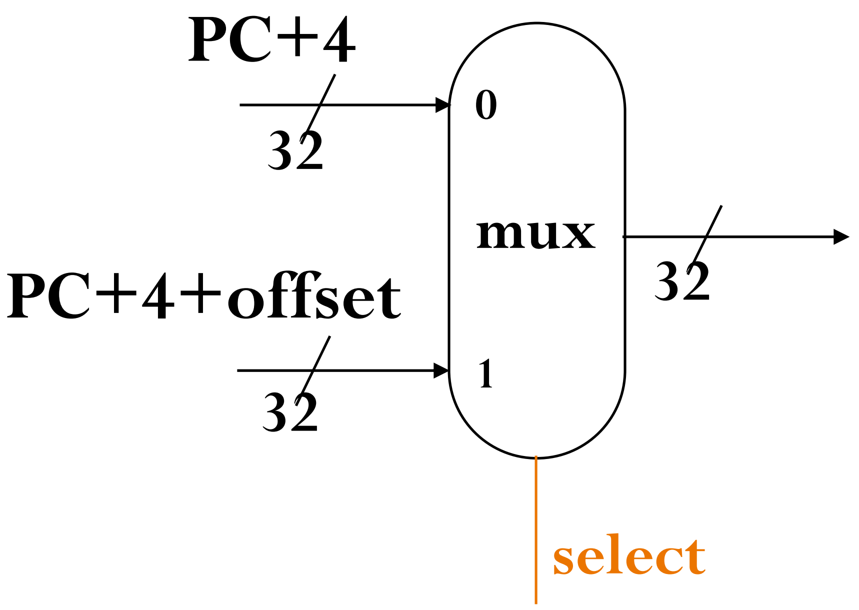
Components - multiplexers



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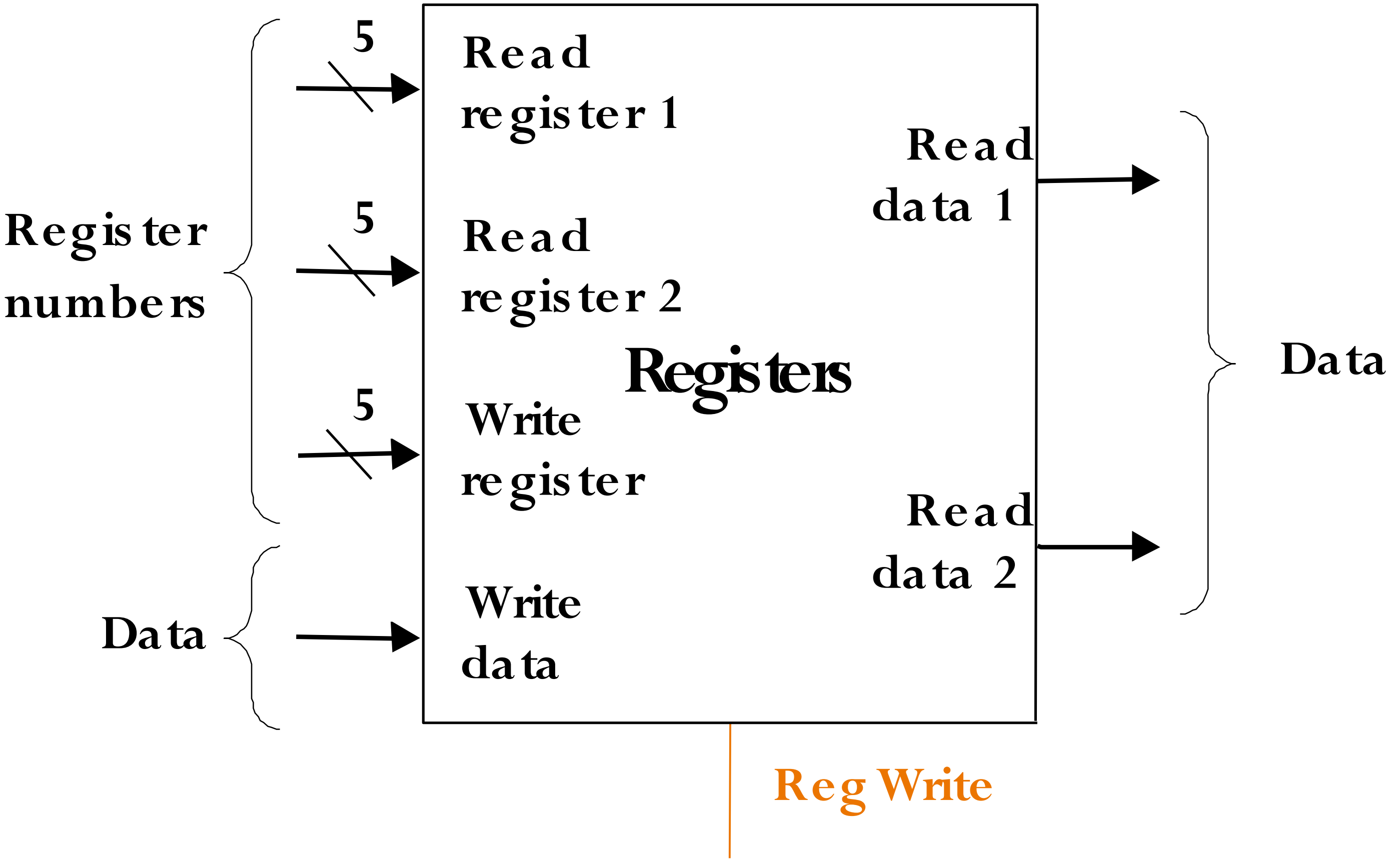
Components - register file



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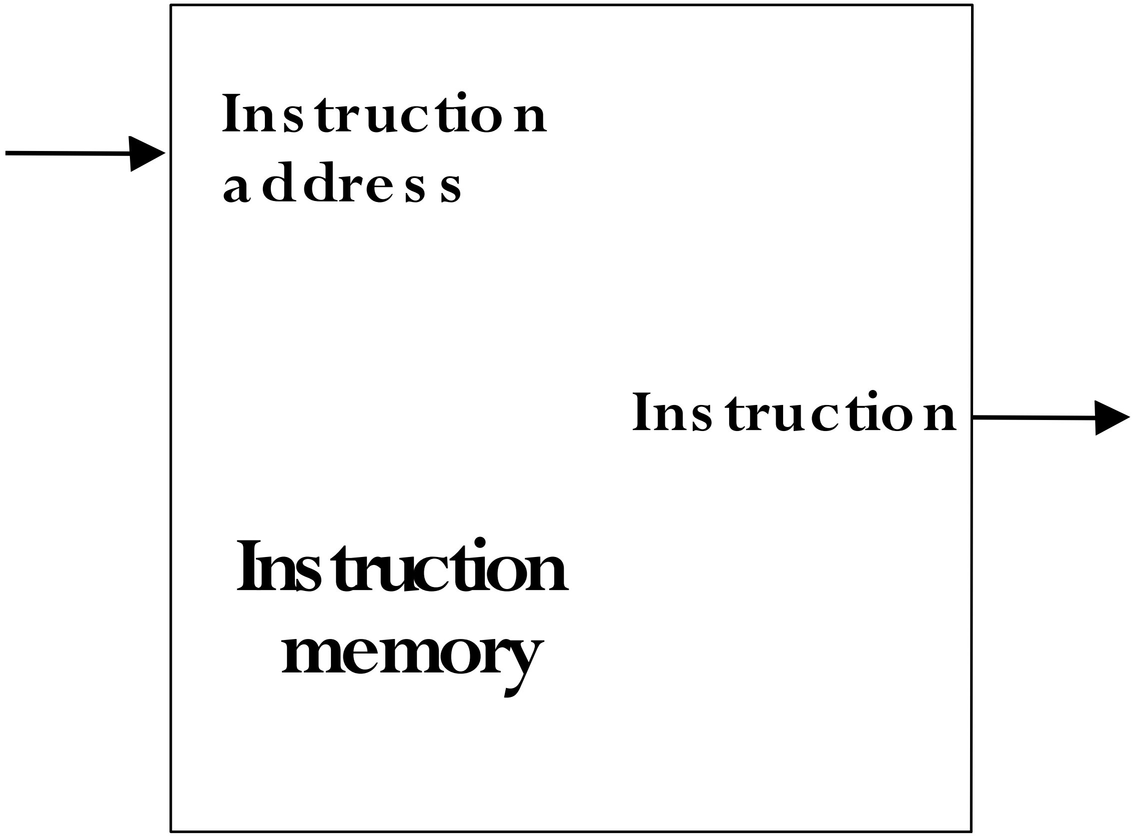
Components - program memory



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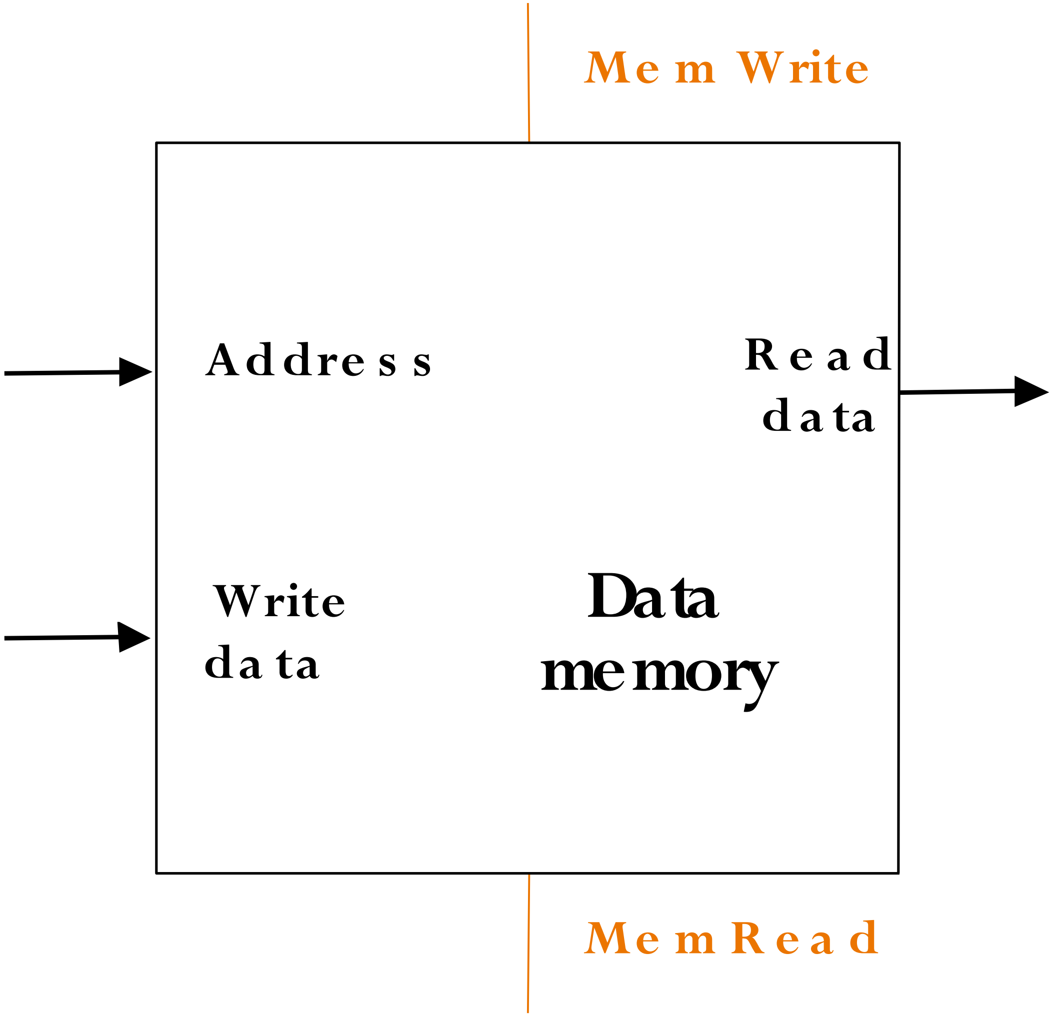
MIPS components - data memory



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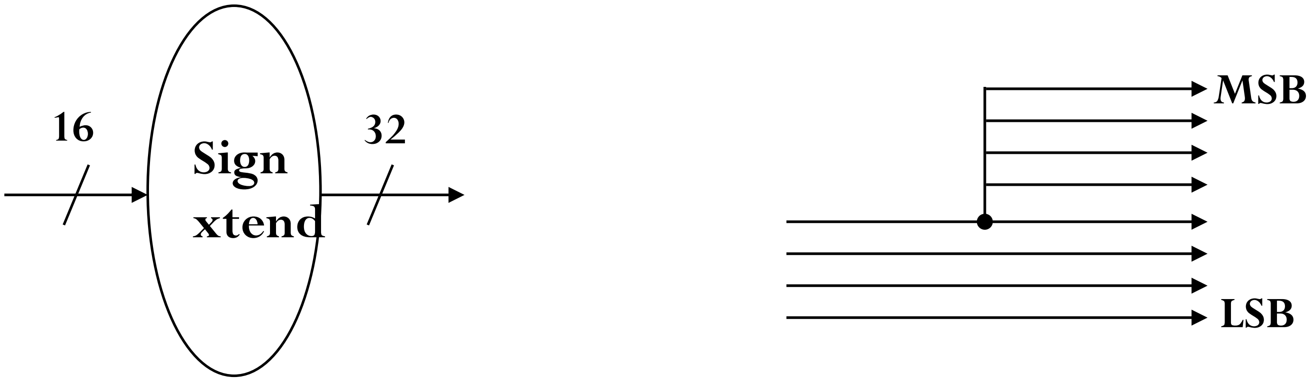
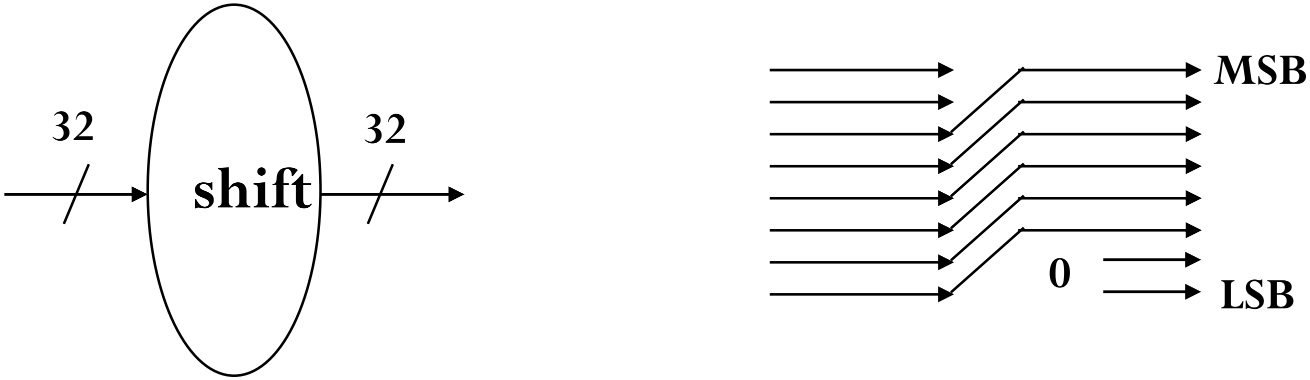
Components - bit manipulation circuits





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MIPS subset for implementation

- Arithmetic - logic instructions
  - add, sub, and, or, slt
- Memory reference instructions
  - lw, sw
- Control flow instructions
  - beq, j

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Datapath for add,sub,and,or,slt

- Fetch instruction
- Address the register file
- Pass operands to ALU
- Pass result to register file
- Increment PC

} actions required

Format: add $t0, $s1, $s2

000000	10001	10010	01000	00000	100000
op	rs	rt	rd	shamt	funct

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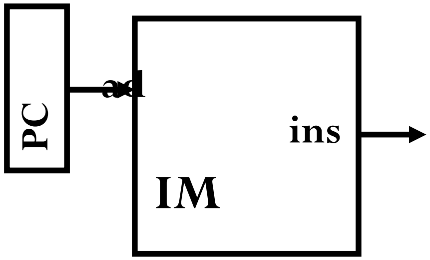
Fetching instruction



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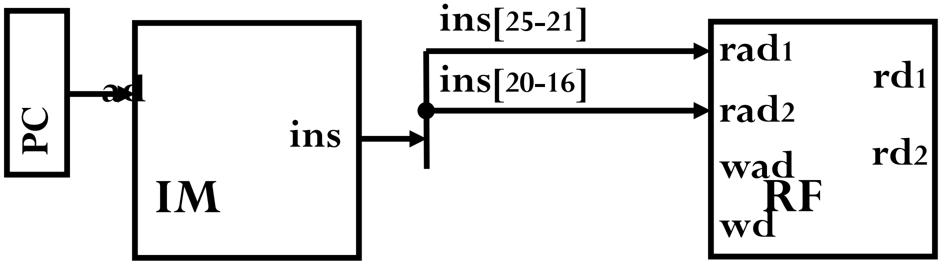
Addressing RF



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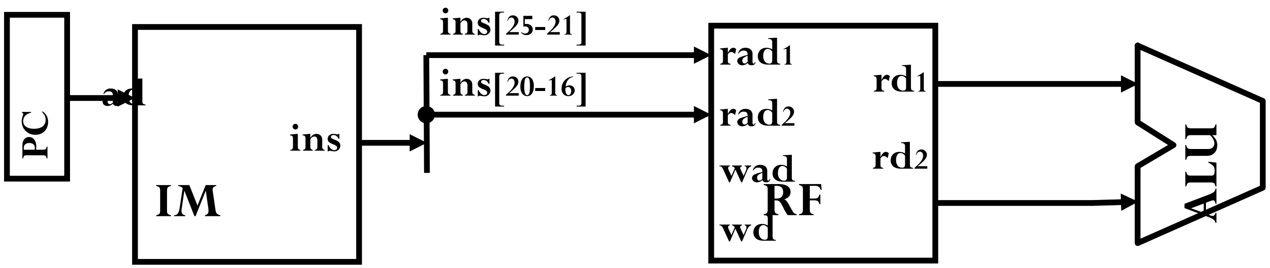
Passing operands to ALU



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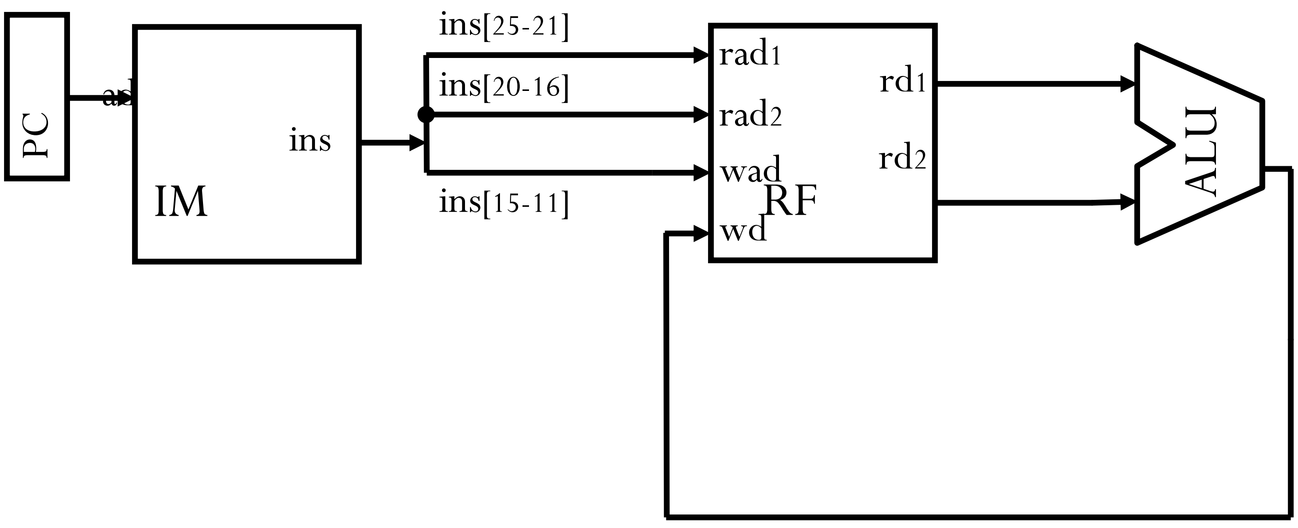
Passing the result to RF



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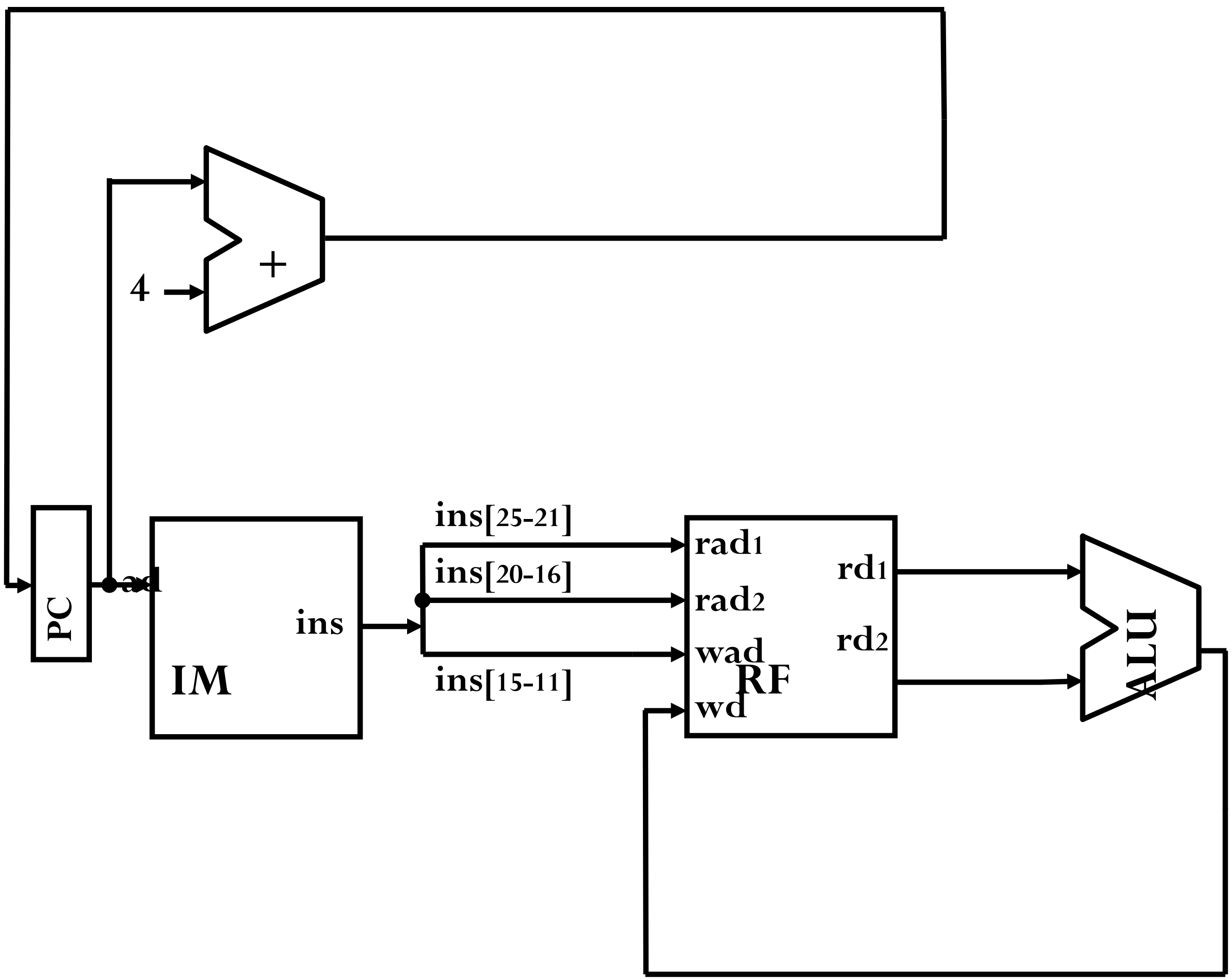
Incrementing PC



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Load and Store instructions

- **format : I**

- **Example: lw $t0, 32($s2)**

35	**18**	**9**	**32**
op	**rs**	**rt**	**16 bit number**

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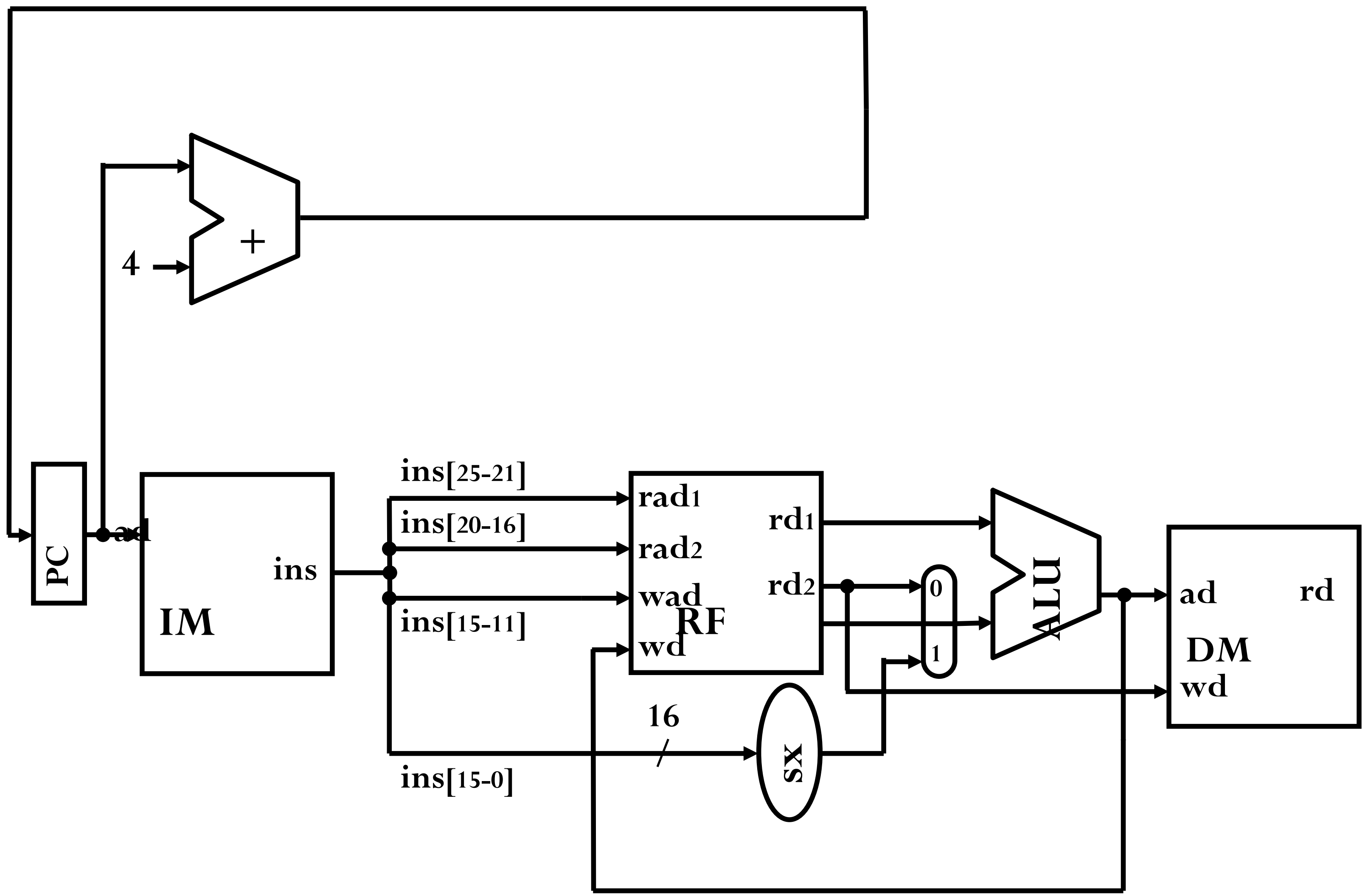
Adding "sw" instruction



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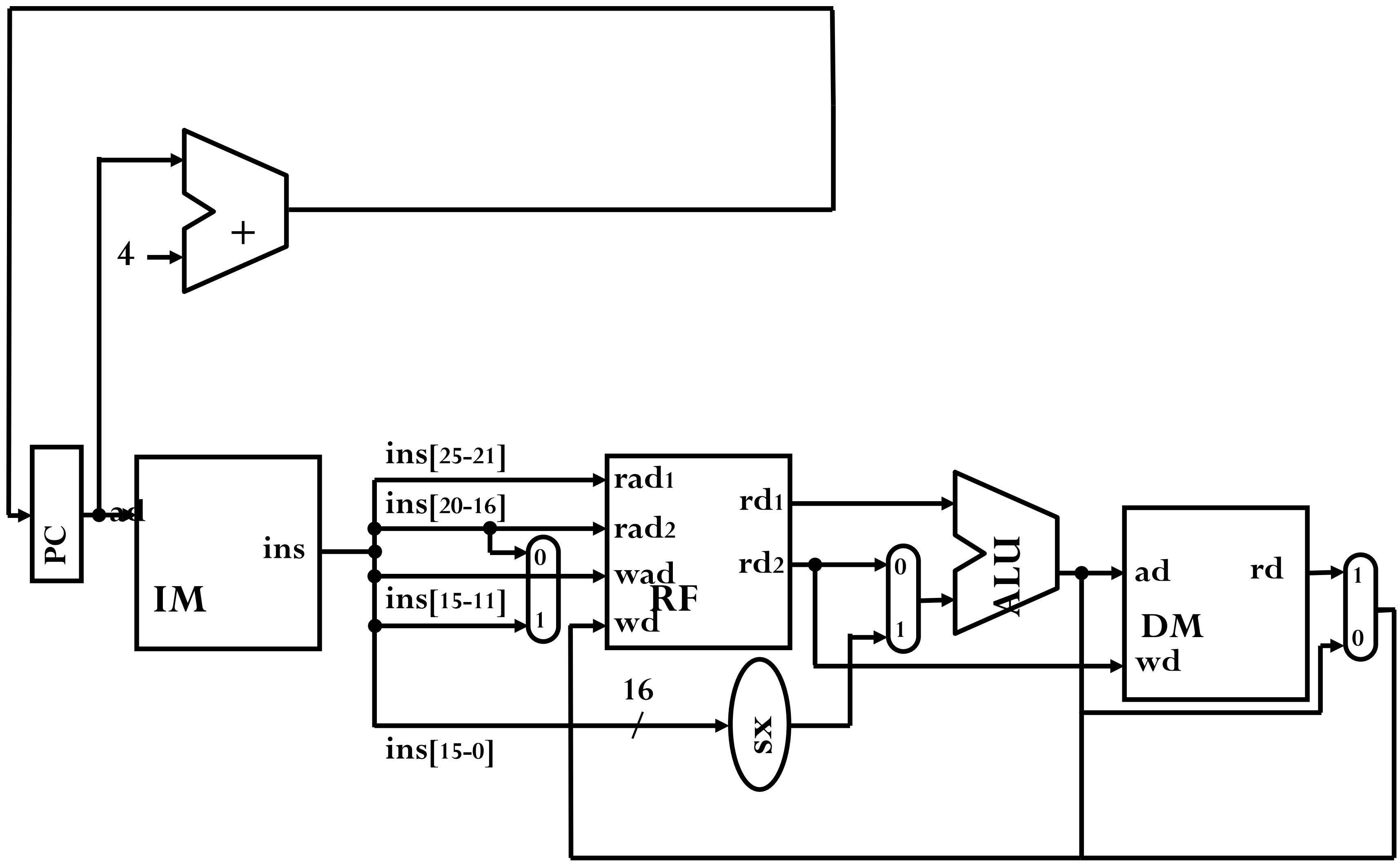
Adding "lw" instruction



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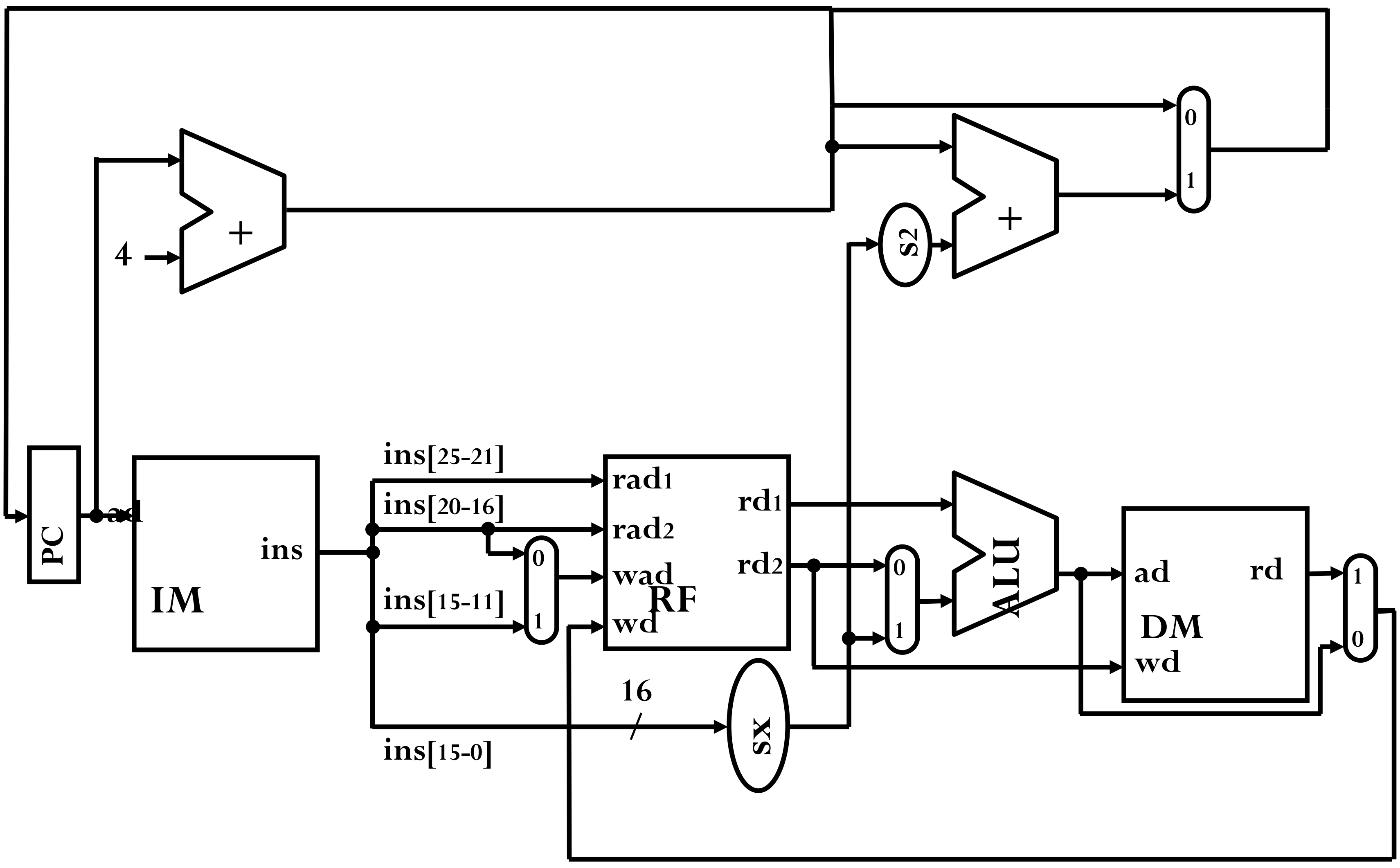
Adding "beq" instruction



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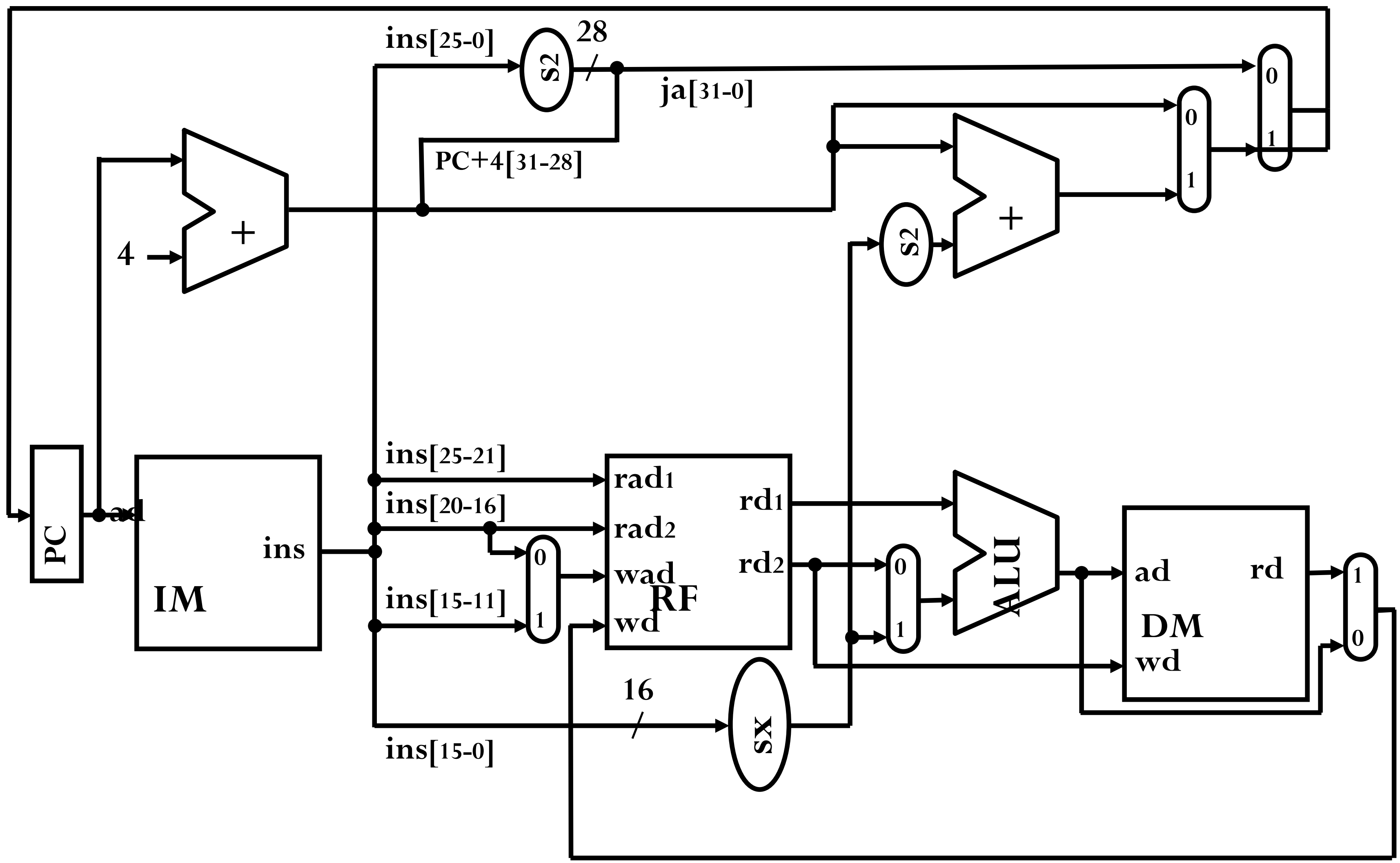
Adding "j" instruction



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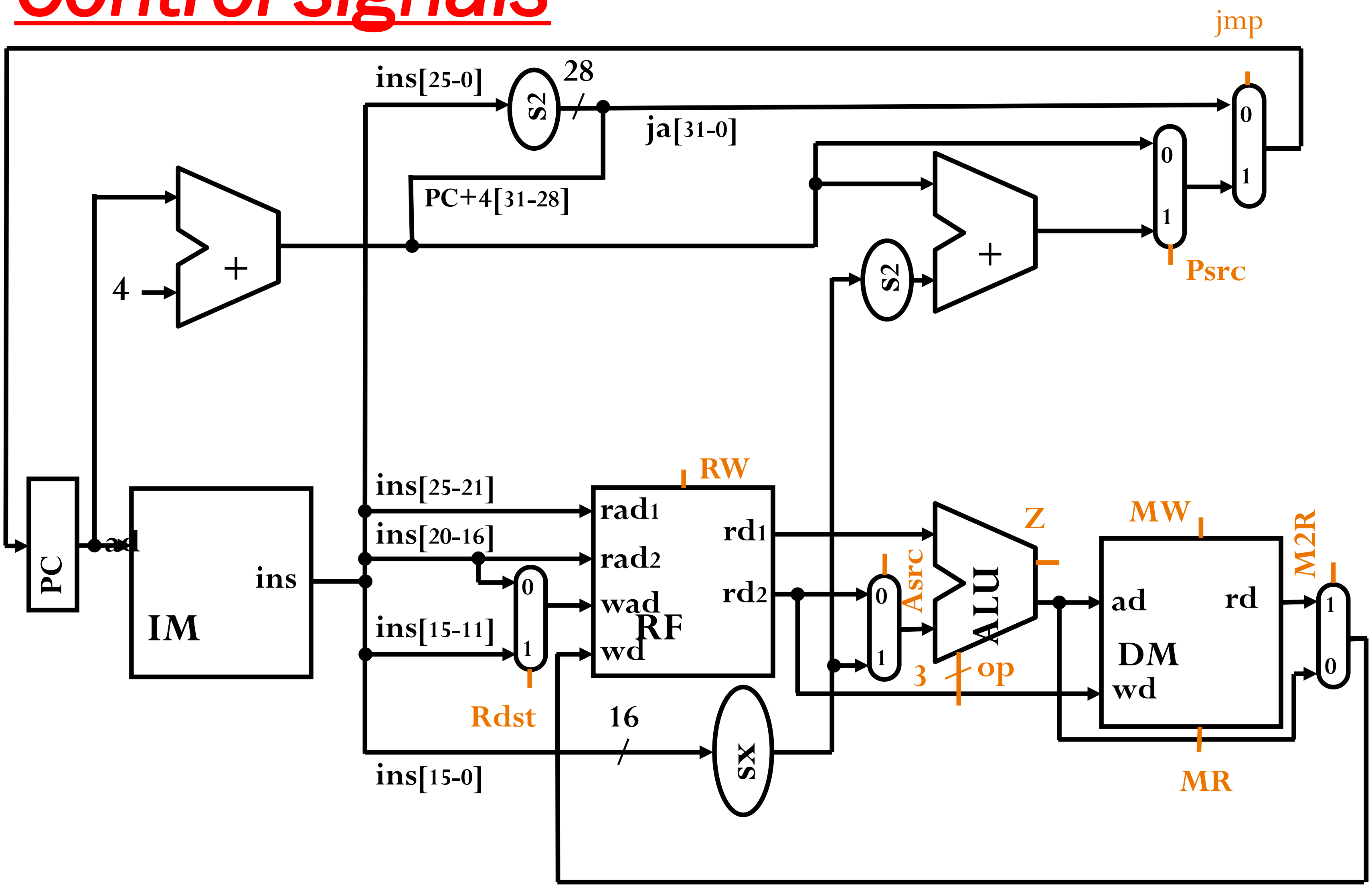
Control signals



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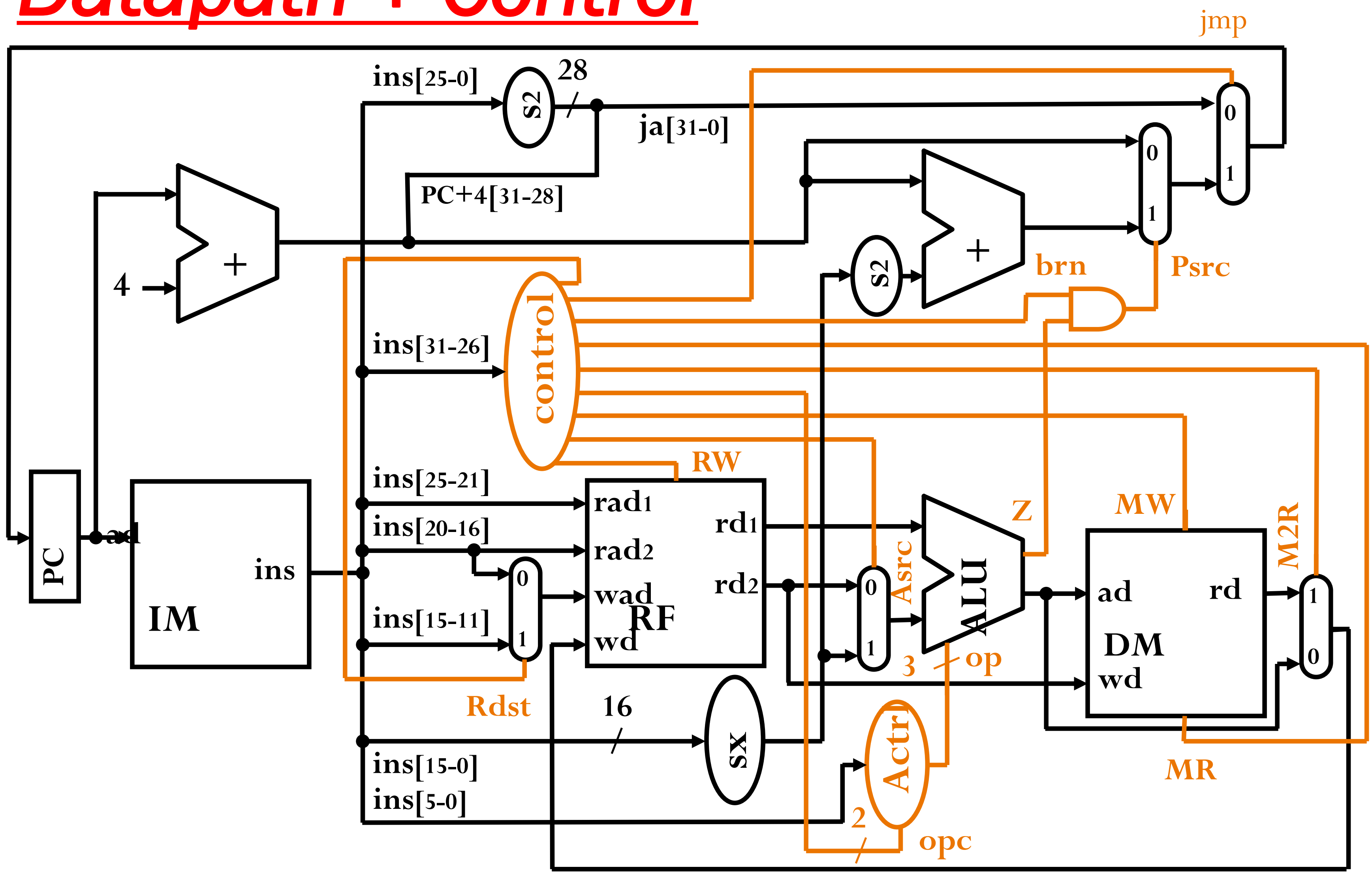
Datapath + Control



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Analyzing performance

Component delays

Register	0
Adder	t_+
ALU	t_A
Multiplexer	0
Register file	t_R
Program memory	t_I
Data memory	t_M
Bit manipulation components	0

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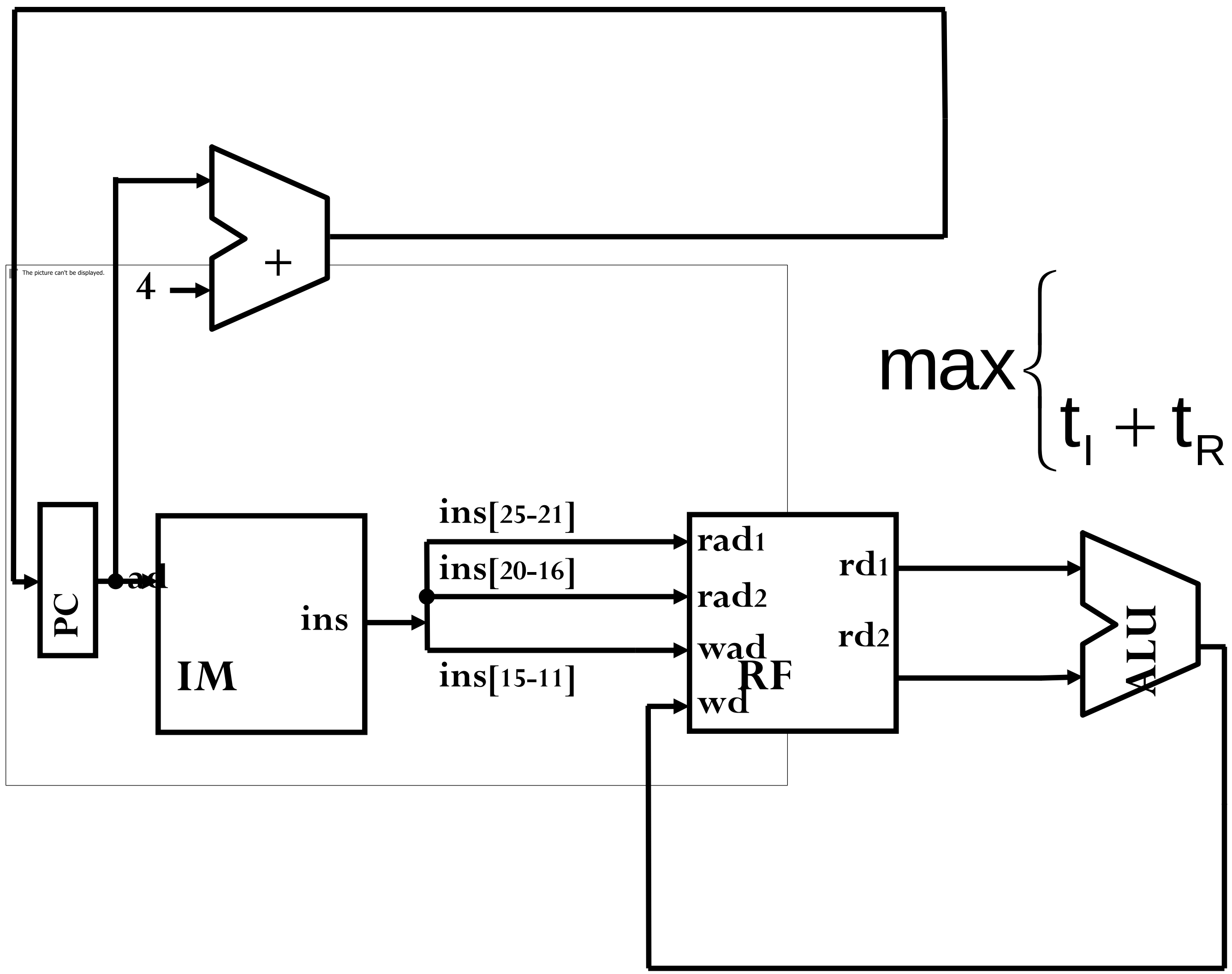
Delay for {add, sub, and, or, slt}



$$\max\begin{cases} t_{+} \\ t_I + t_R + t_A + t_R \end{cases}$$

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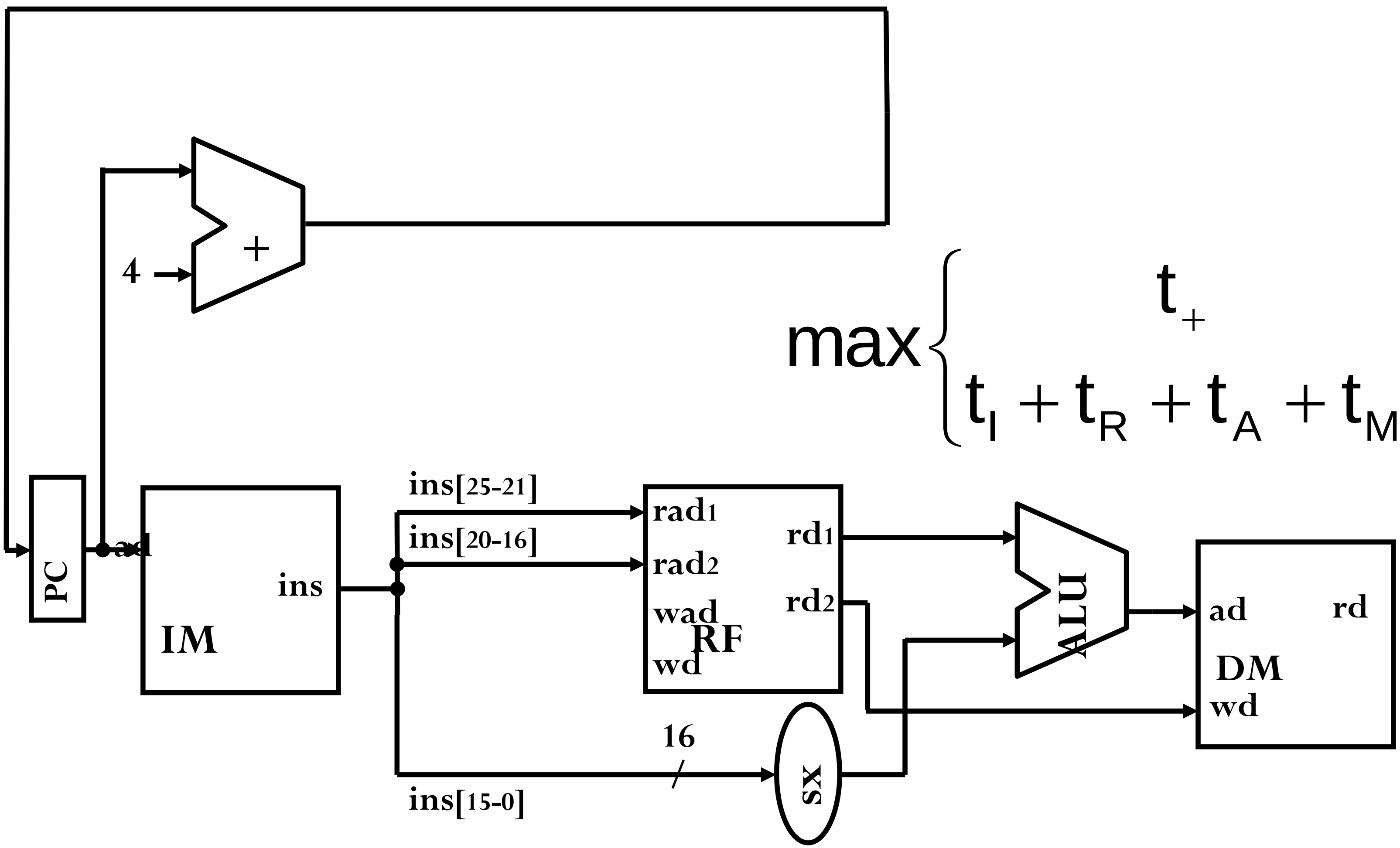
Delay for {sw}



$$\max \begin{cases} t_{+} \\ t_{I} + t_{R} + t_{A} + t_{M} \end{cases}$$

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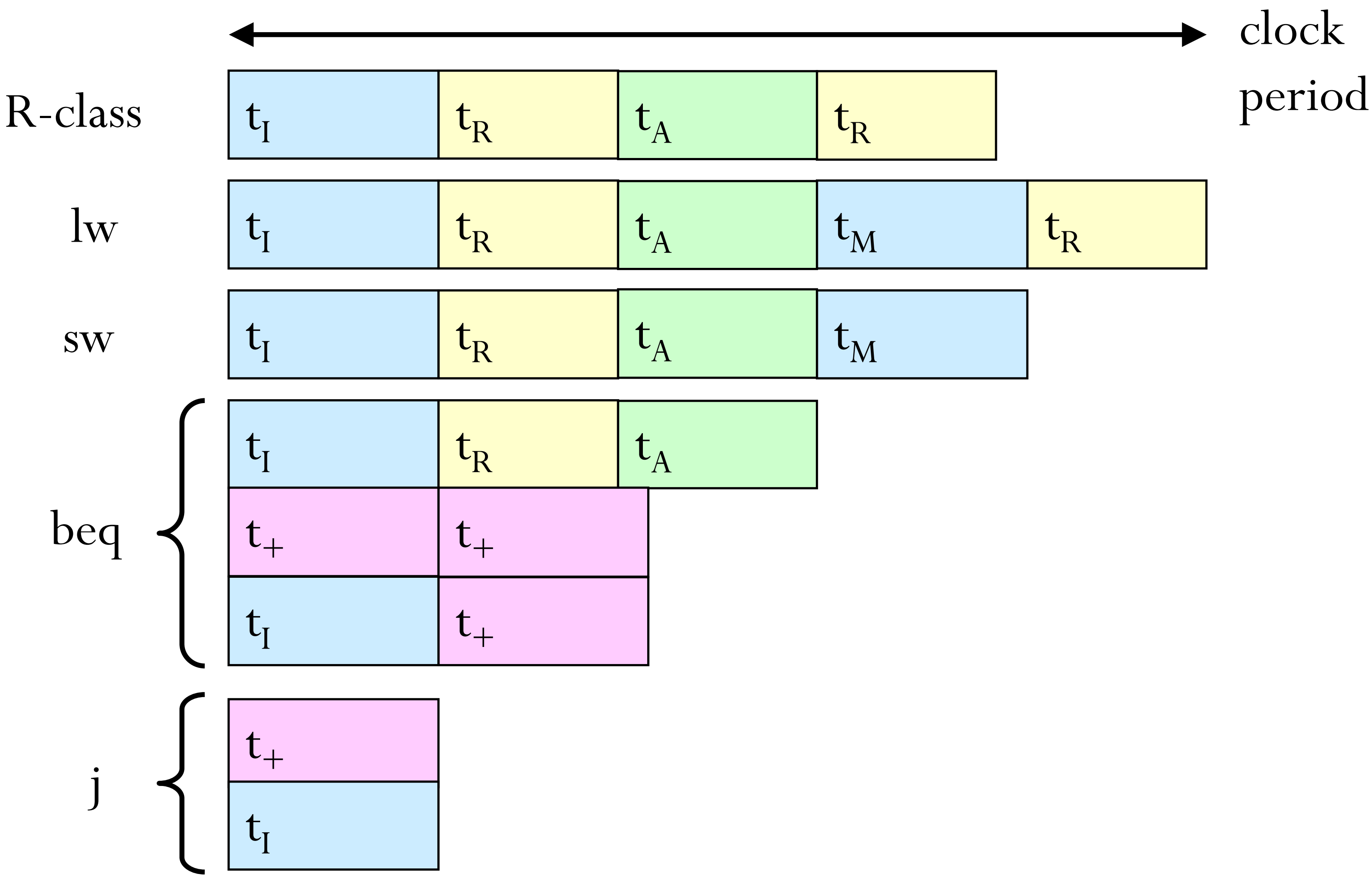
Clock period in single cycle design



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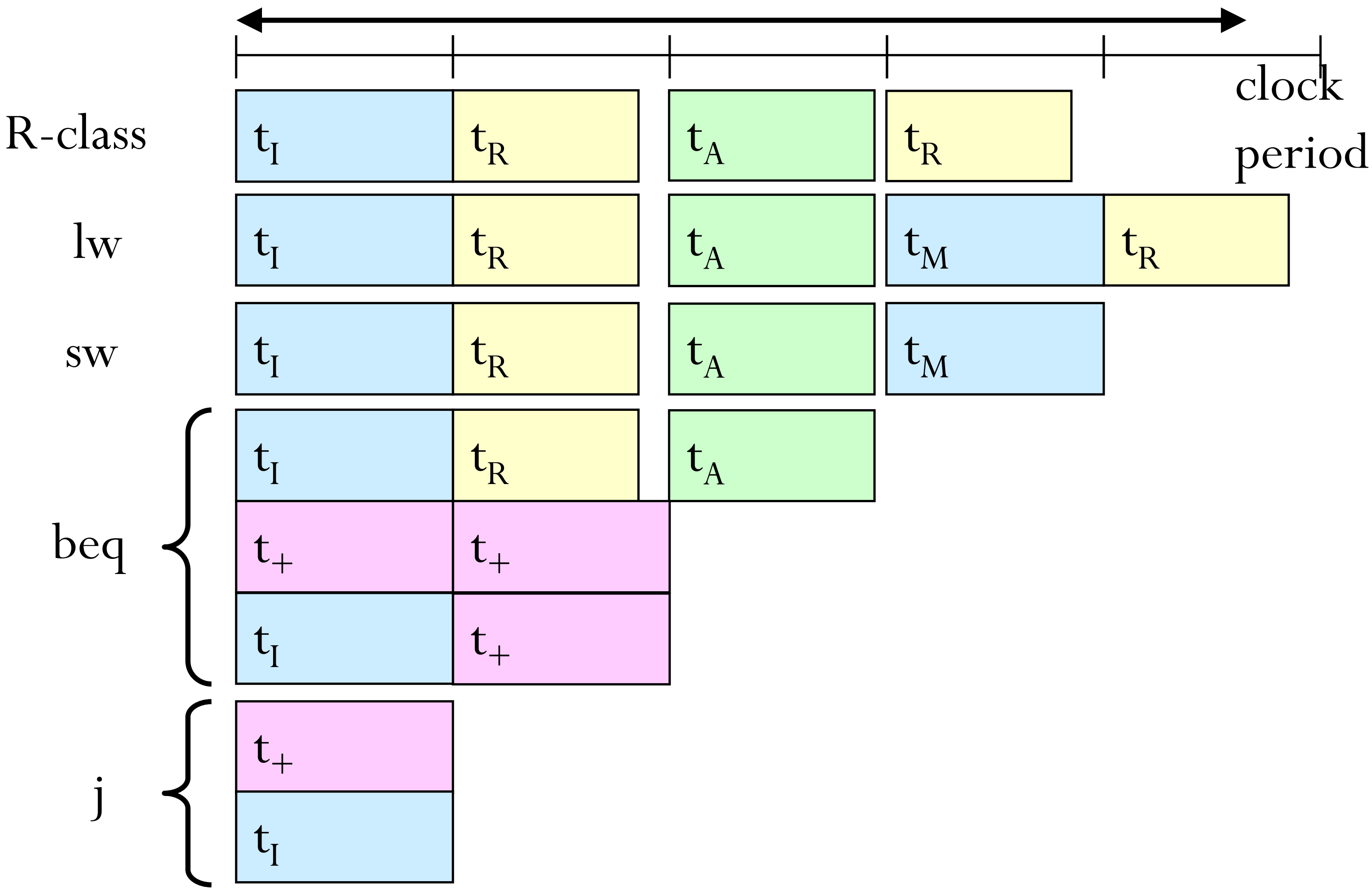
Clock period in multi-cycle design



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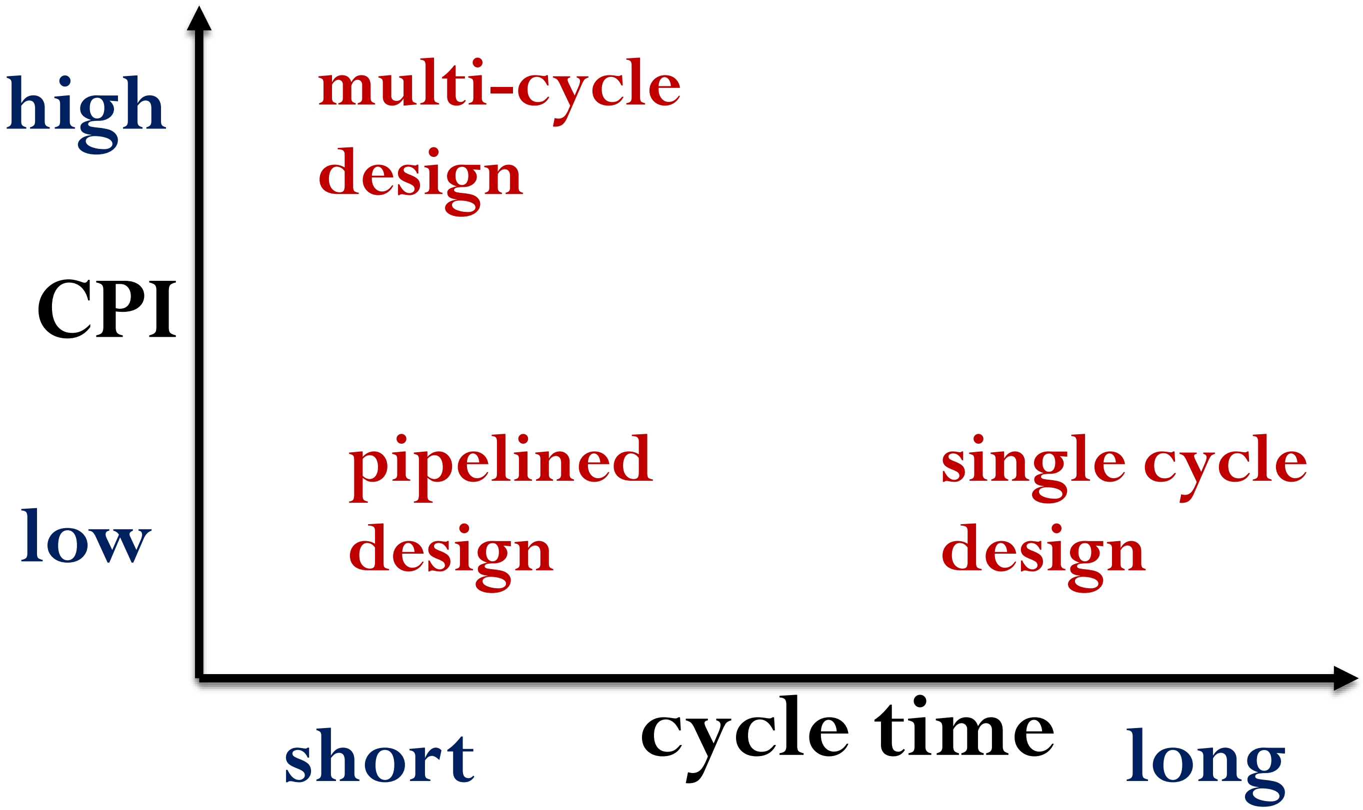
Cycle time and CPI



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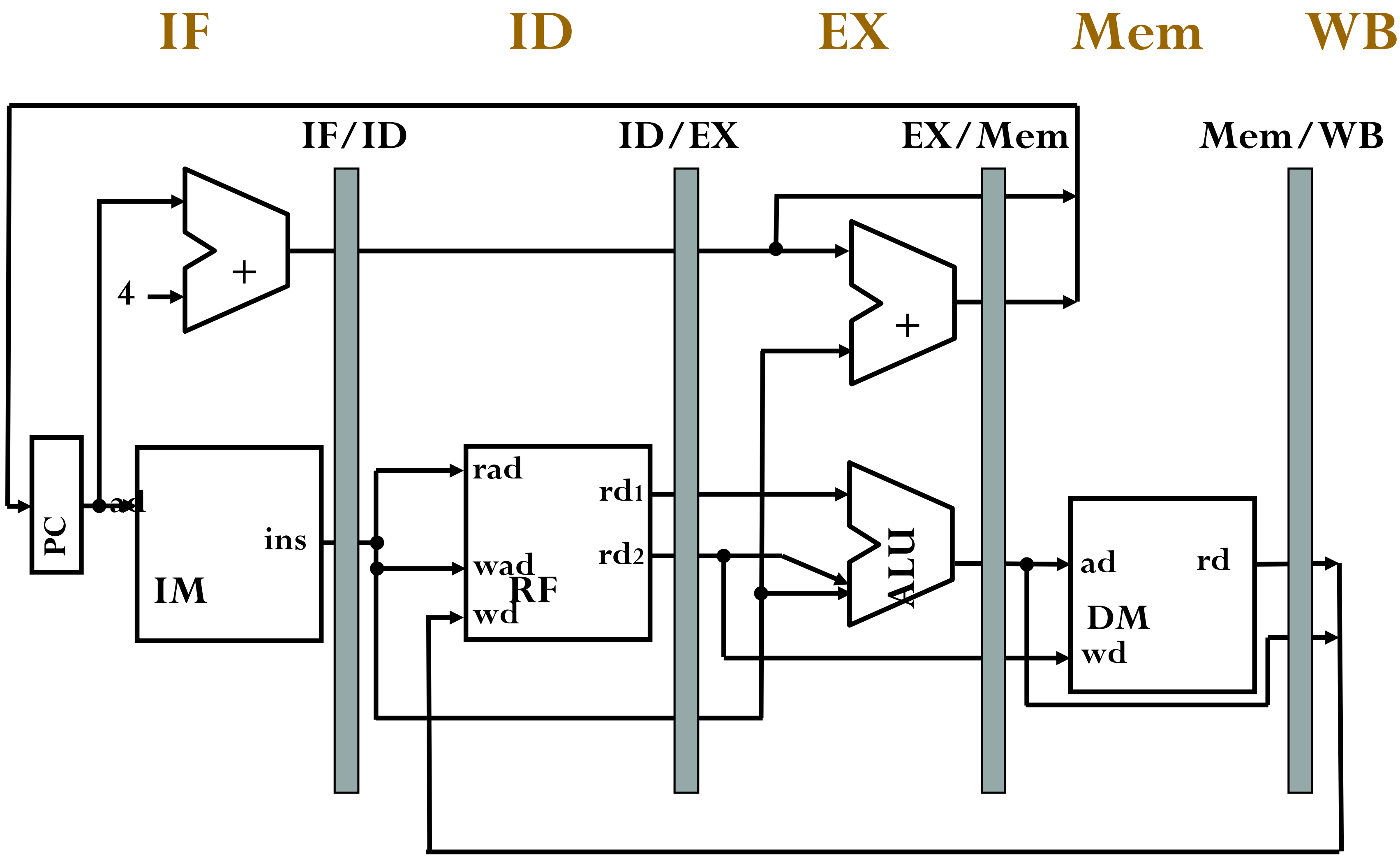
PIpelined datapath (abstract)



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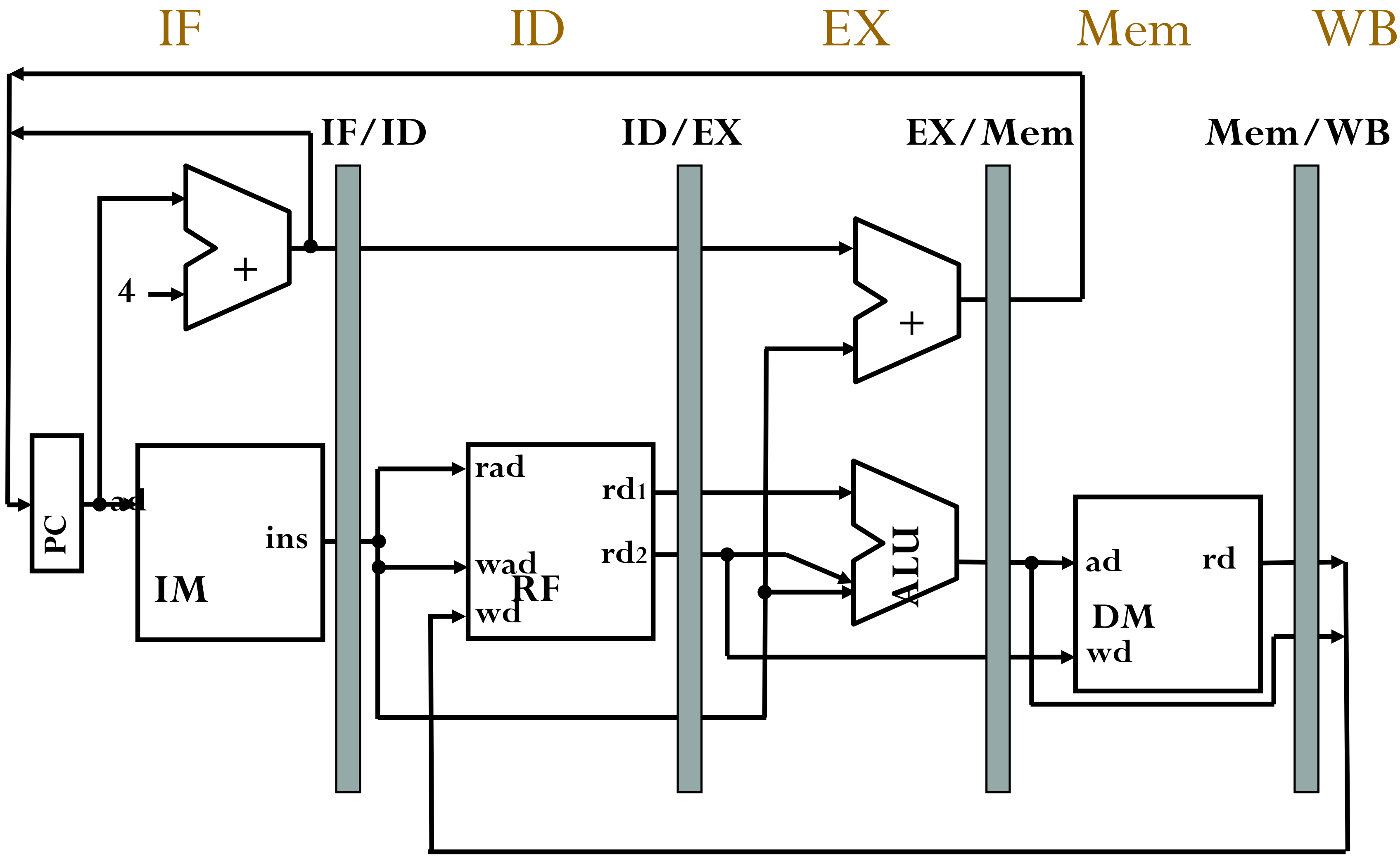
Fetch new instruction every cycle



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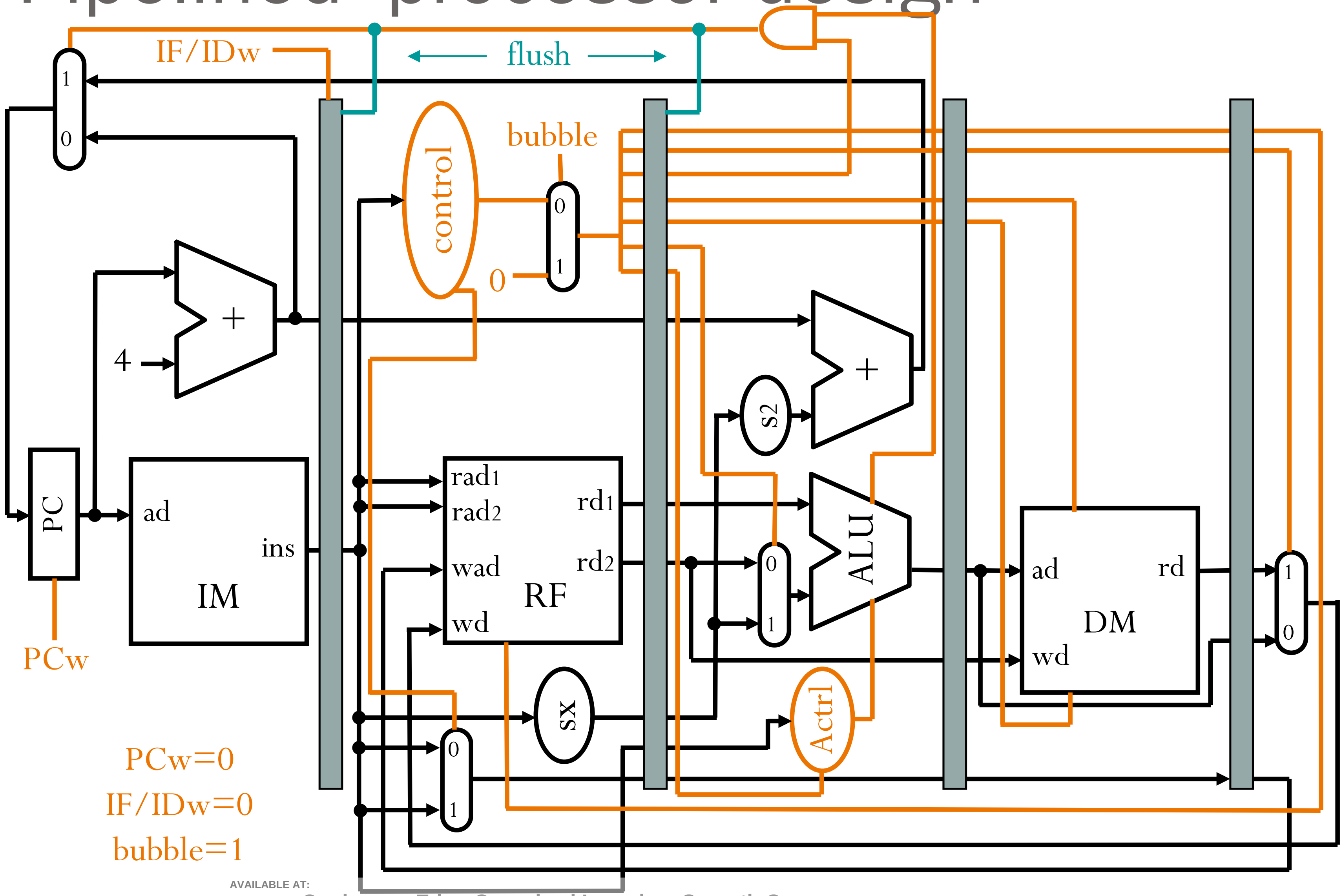
Pipelined processor design



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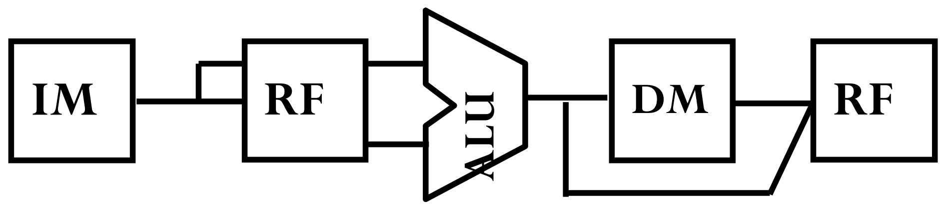
Graphical representation

5 stage pipeline

stages



actions

IF	ID	EX	Mem	WB

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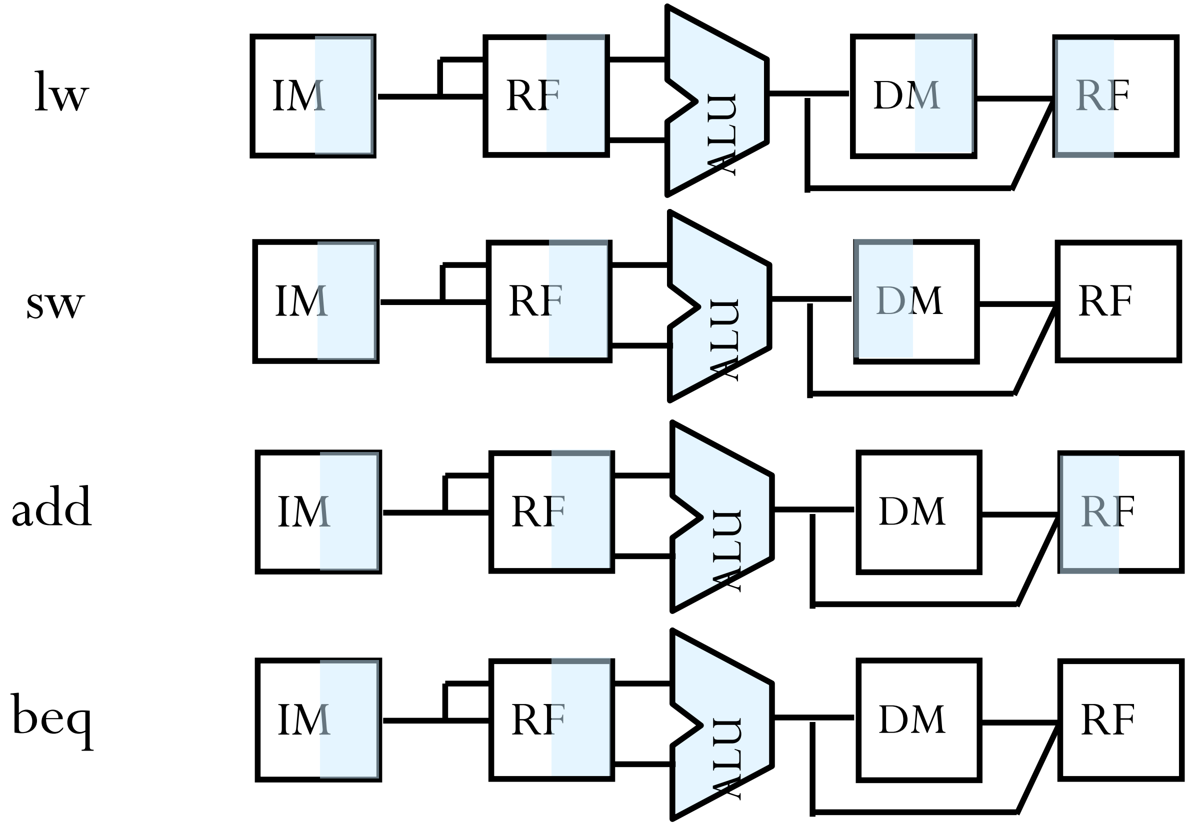
Usage of stages by instructions



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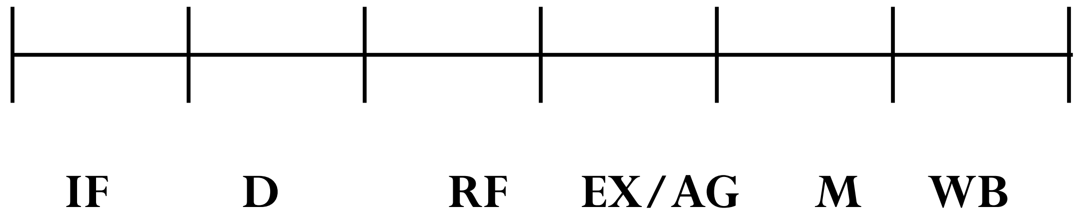
Pipelining

Simple multicycle design :

- Resource sharing across cycles
- All instructions may not take same cycles



- Faster throughput with pipelining

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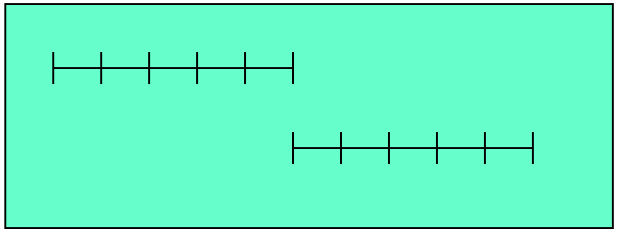
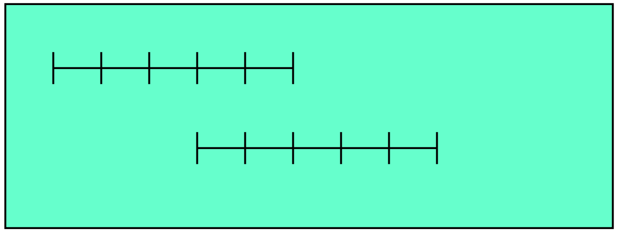
Degree of overlap Depth

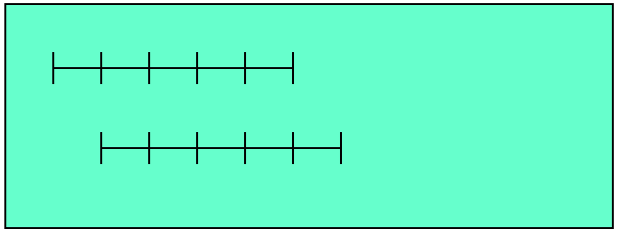
Serial



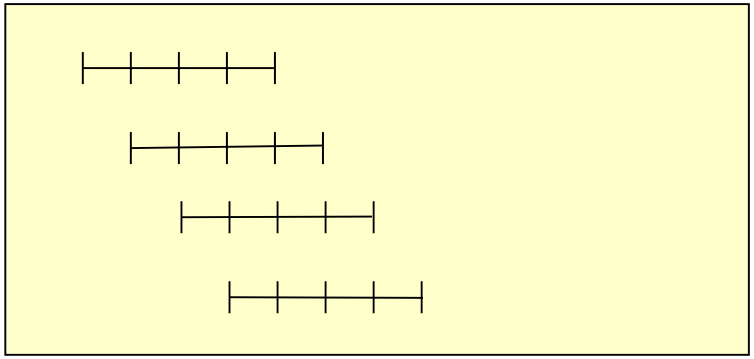
Overlapped



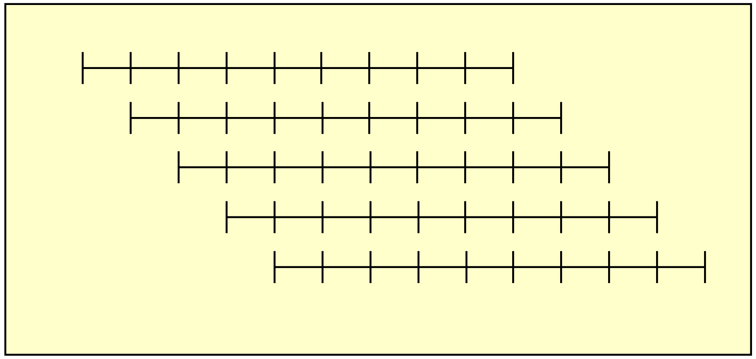
Pipelined



Shallow



Deep



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Hazards in Pipelining

- Procedural dependencies => Control hazards
  - cond and uncond branches, calls/returns
- Data dependencies => Data hazards
  - RAW (read after write)
  - WAR (write after read)
  - WAW (write after write)
- Resource conflicts => Structural hazards
  - use of same resource in different stages

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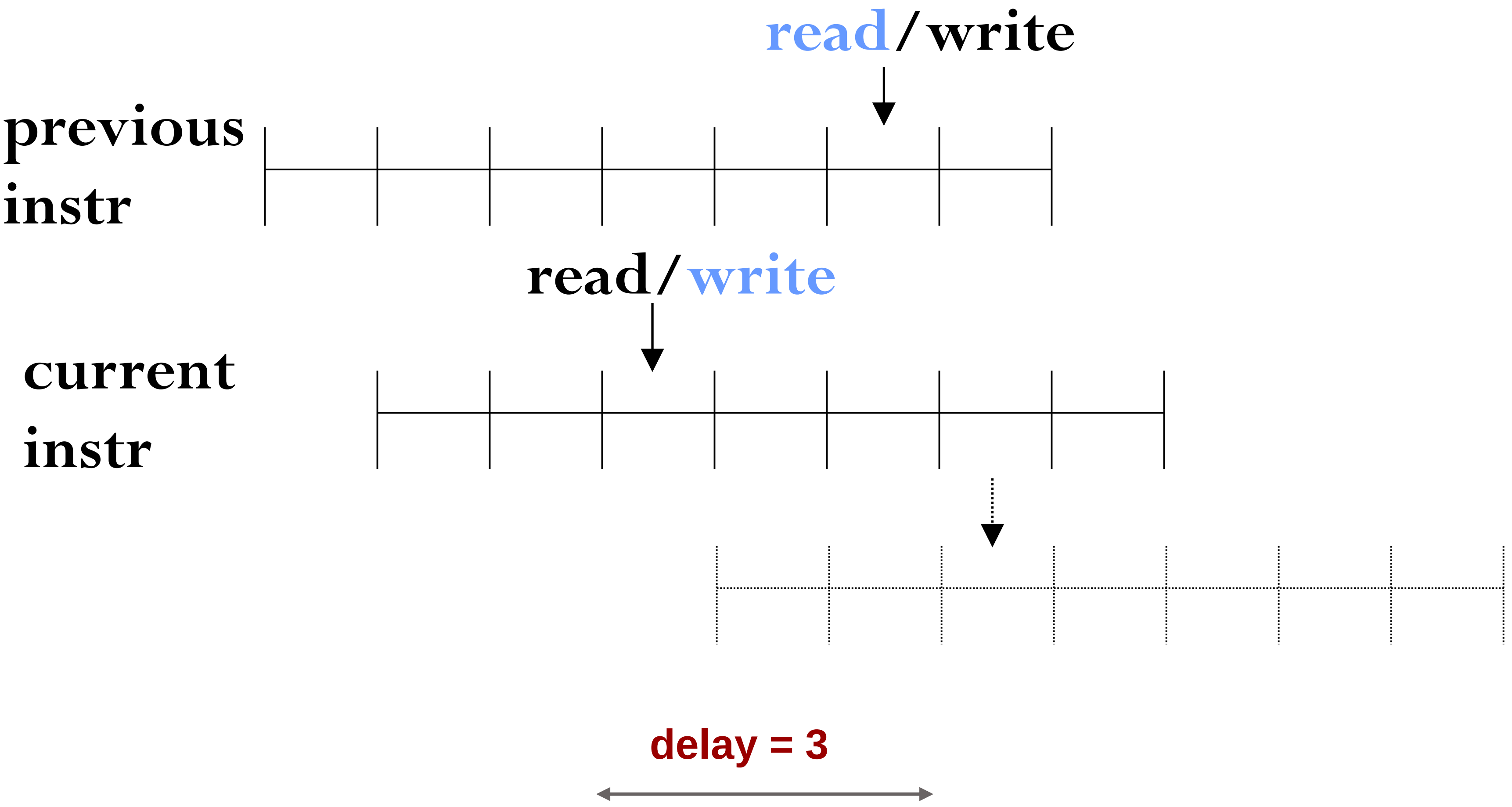
Data Hazards



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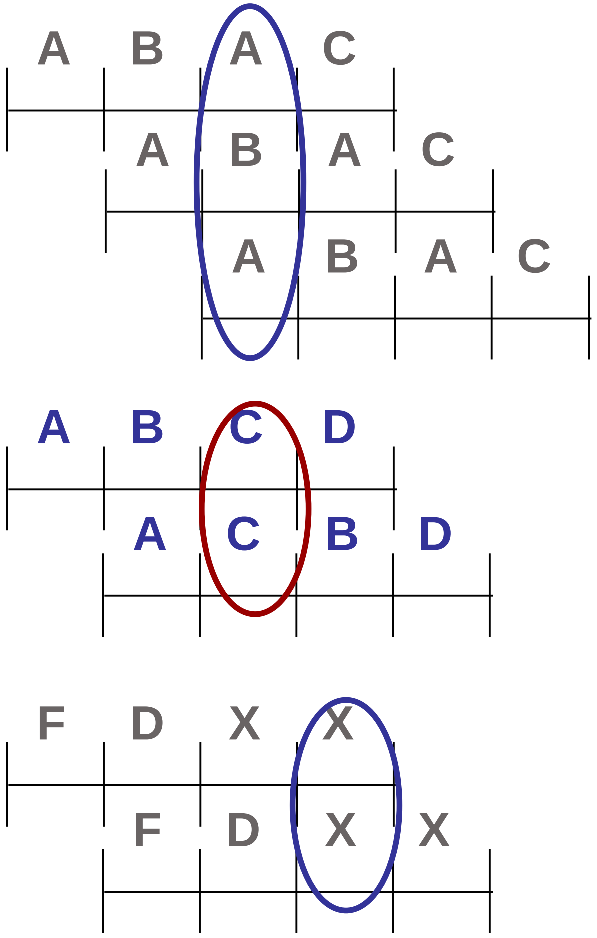
Structural Hazards

Caused by Resource Conflicts

- Use of a hardware resource in more than one cycle
- Different sequences of resource usage by different instructions
- Non-pipelined multi-cycle resources



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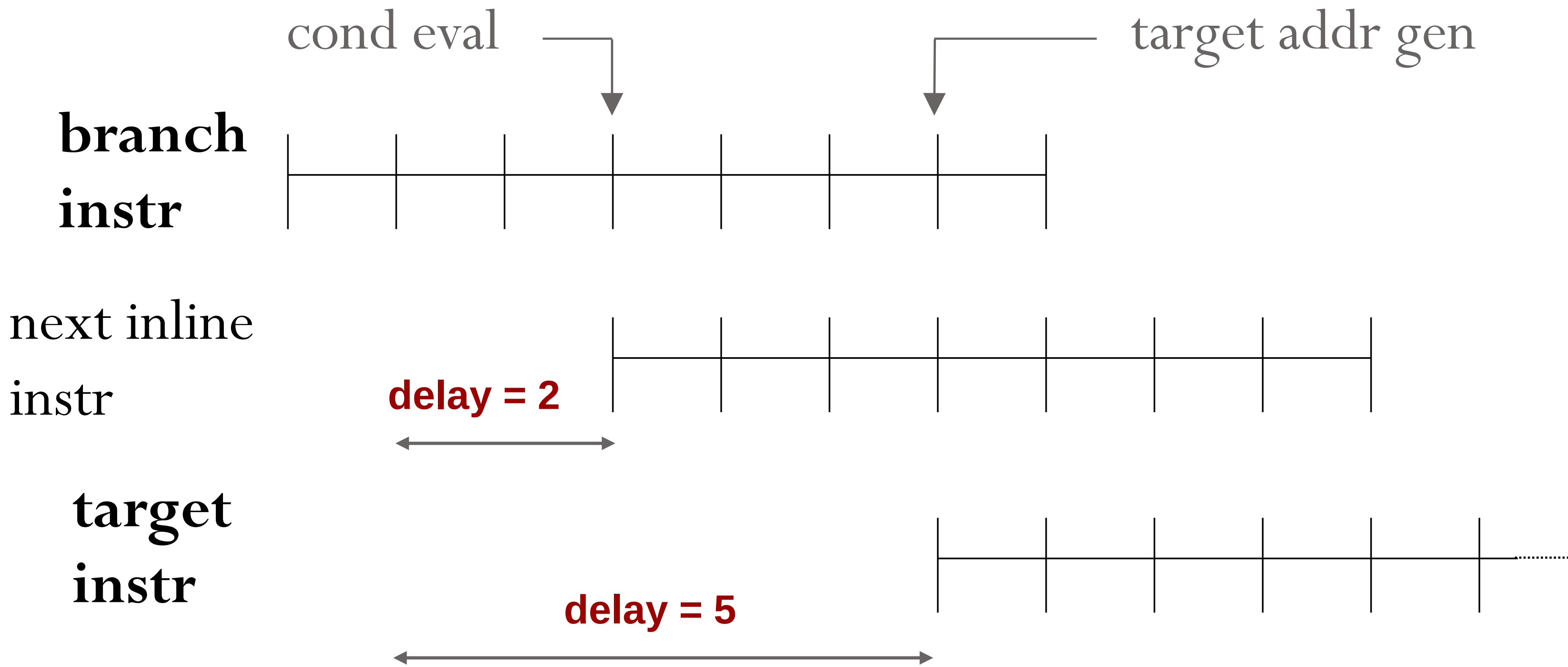
Control Hazards



- the order of *cond eval* and *target addr gen* may be different
- *cond eval* may be done in previous instruction

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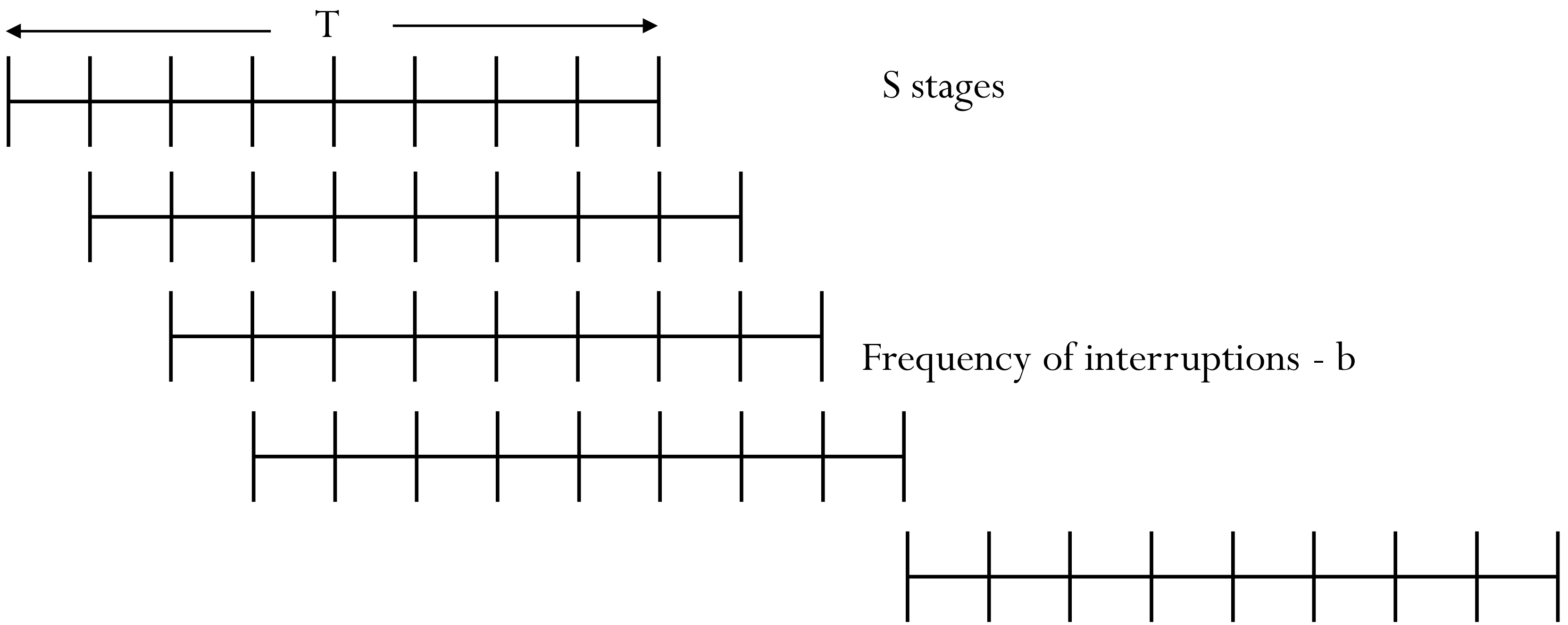
Pipeline Performance



$$CPI = 1 + (S - 1) * b$$

$$Time = CPI * T / S$$

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Improving Branch Performance

- Branch Elimination
  - Replace branch with other instructions
- Branch Speed Up
  - Reduce time for computing CC and TIF
- Branch Prediction
  - Guess the outcome and proceed, undo if necessary
- Branch Target Capture
  - Make use of history

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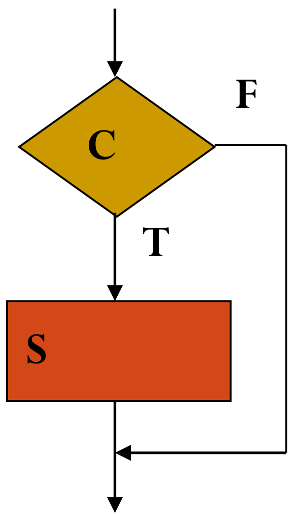
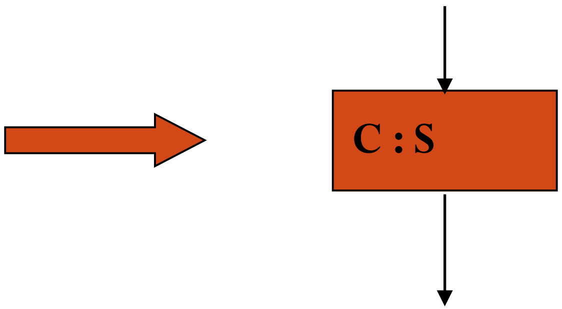
Branch Elimination

Use conditional instructions (predicated execution)





OP1
BC CC = Z, * + 2
ADD R3, R2, R1
OP2

→

OP1
ADD R3, R2, R1, NZ
OP2

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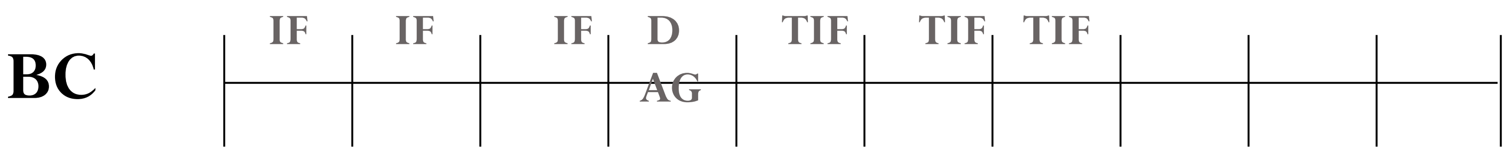
Branch Speed Up :

Early target address generation

- **Assume each instruction is Branch**
- **Generate target address while decoding**
- **If target in same page omit translation**
- **After decoding discard target address if not Branch**



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Branch Prediction

- **Treat conditional branches as unconditional branches / NOP**
- **Undo if necessary**

Strategies:

- **Fixed** ***(always guess inline)***
- **Static** ***(guess on the basis of instruction type)***
- **Dynamic** ***(guess based on recent history)***

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Static Branch Prediction

Instr	%	Guess	Branch	Correct
uncond	14.5	always	100%	14.5%
cond	58	never	54%	27%
loop	9.8	always	91%	9%
call/ret	17.7	always	100%	17.7%

Total 68.2%

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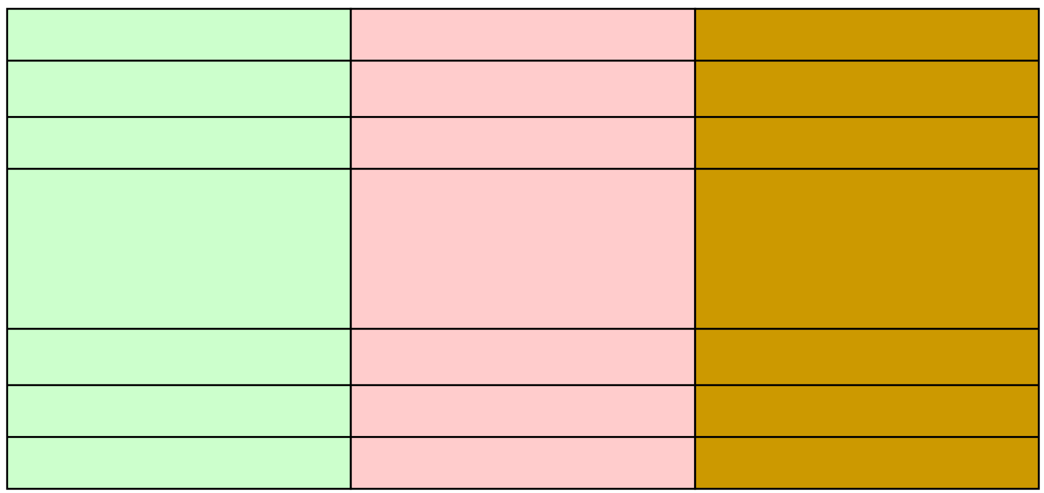
Branch Target Capture

- Branch Target Buffer (BTB)
- Target Instruction Buffer (TIB)



instr addr pred stats target

prob of target change < 5%

target addr
target instr

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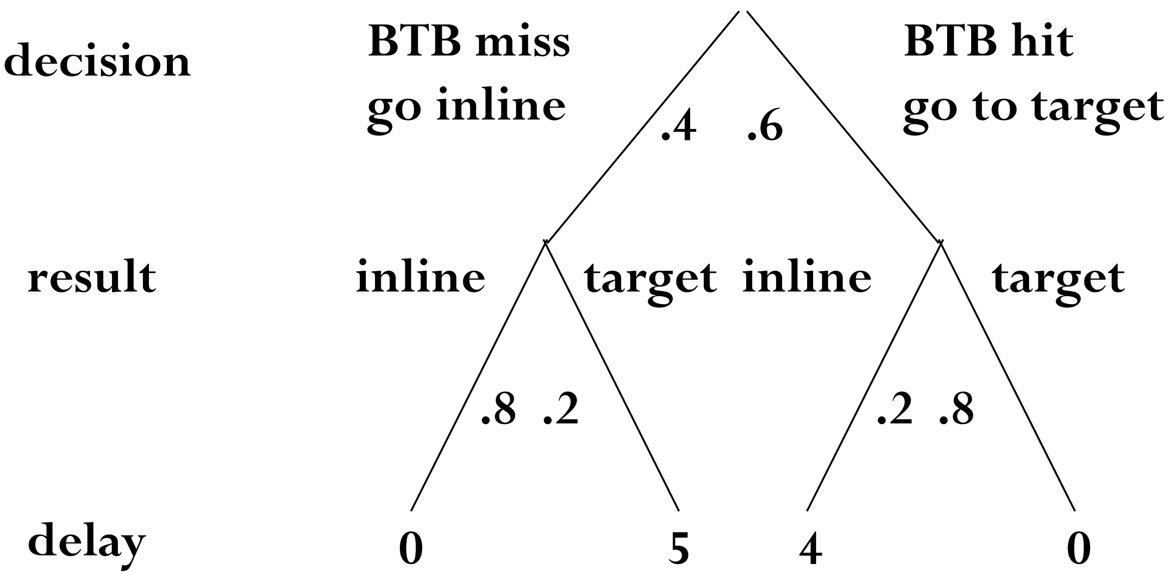
BTB Performance



.4*.8*0 + .4*.2*5 + .6*.2*4 + .6*.8*0 = 0.88 (Eff.Delay)

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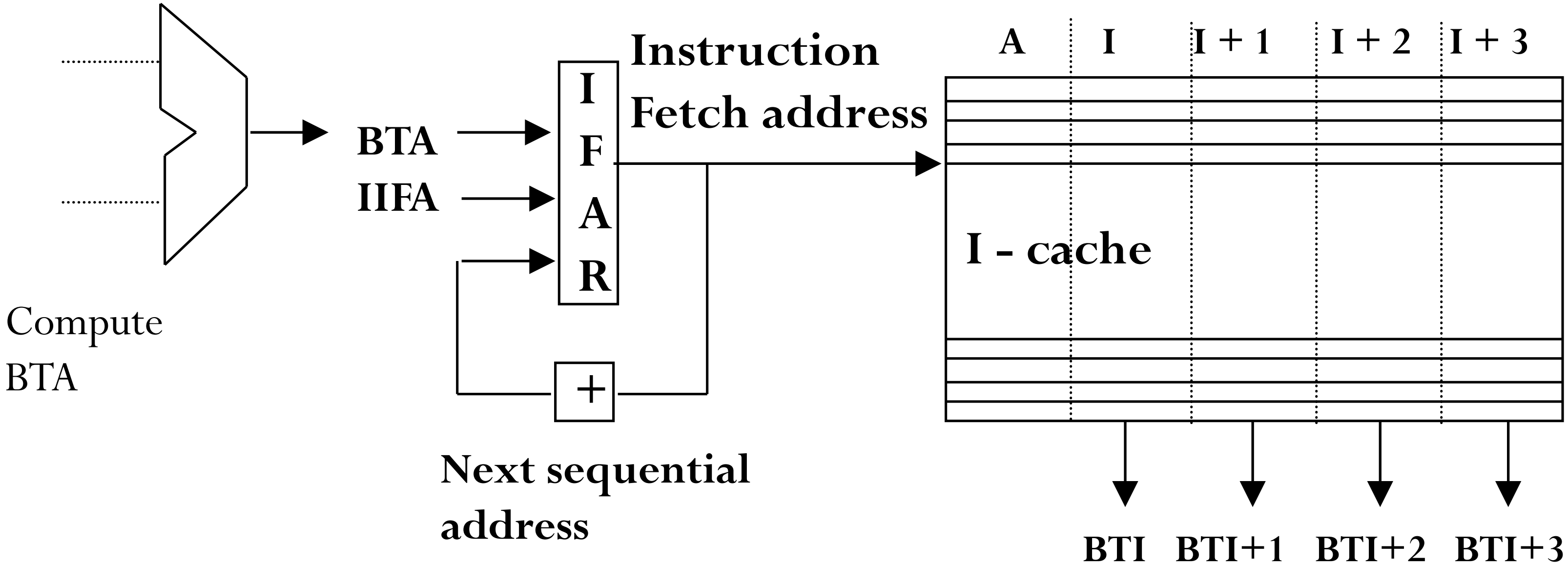
Compute/fetch scheme

(no dynamic branch prediction)



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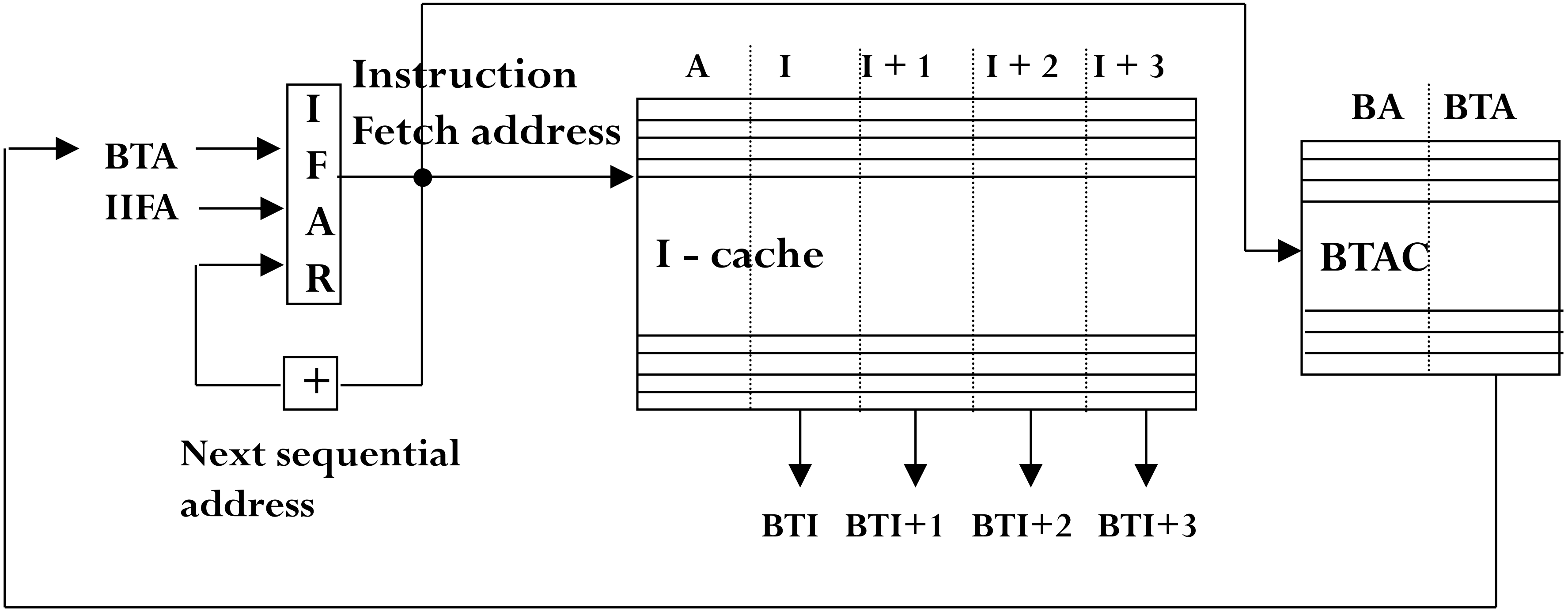
BTAC scheme



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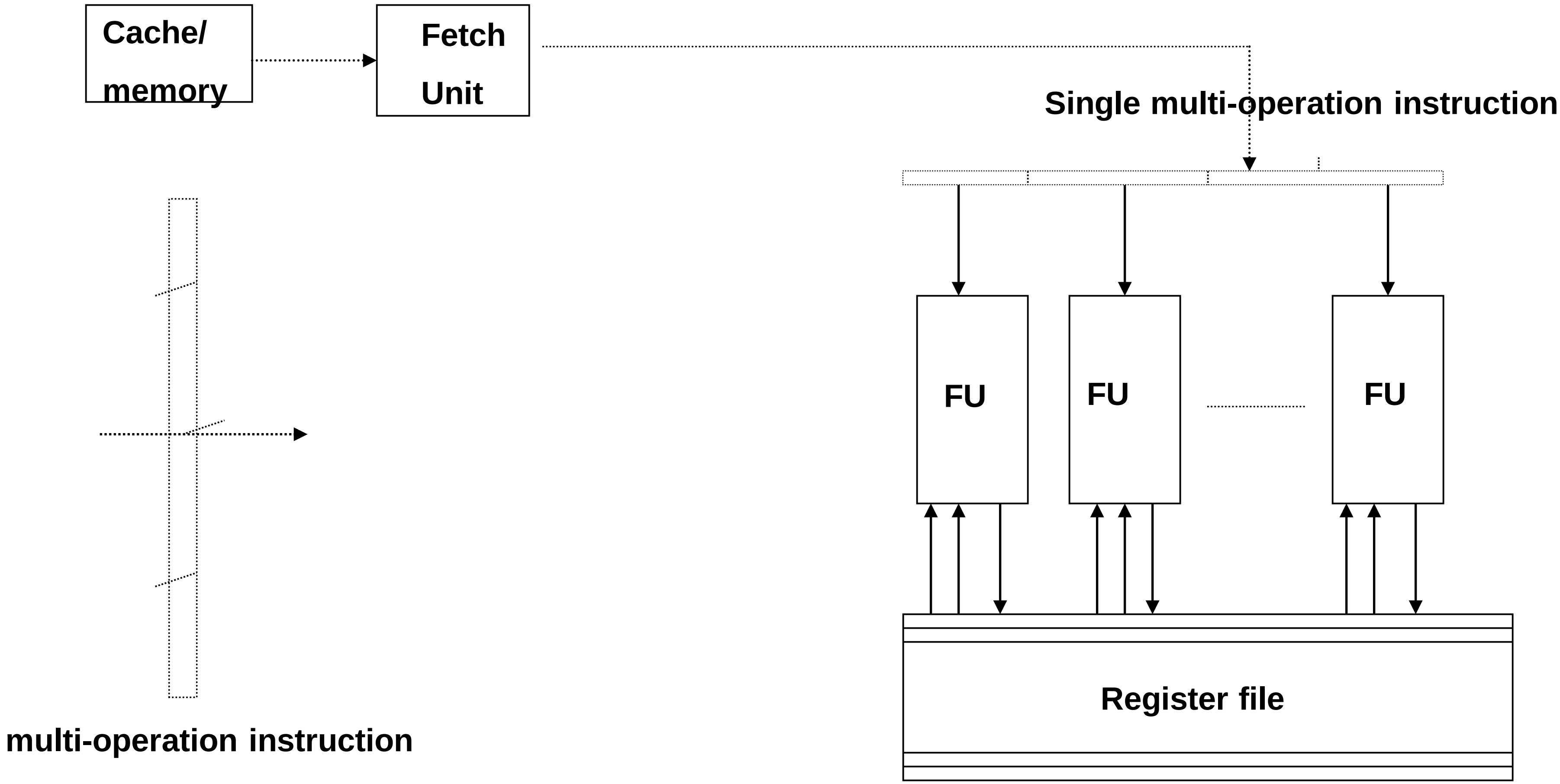
ILP in VLIW processors



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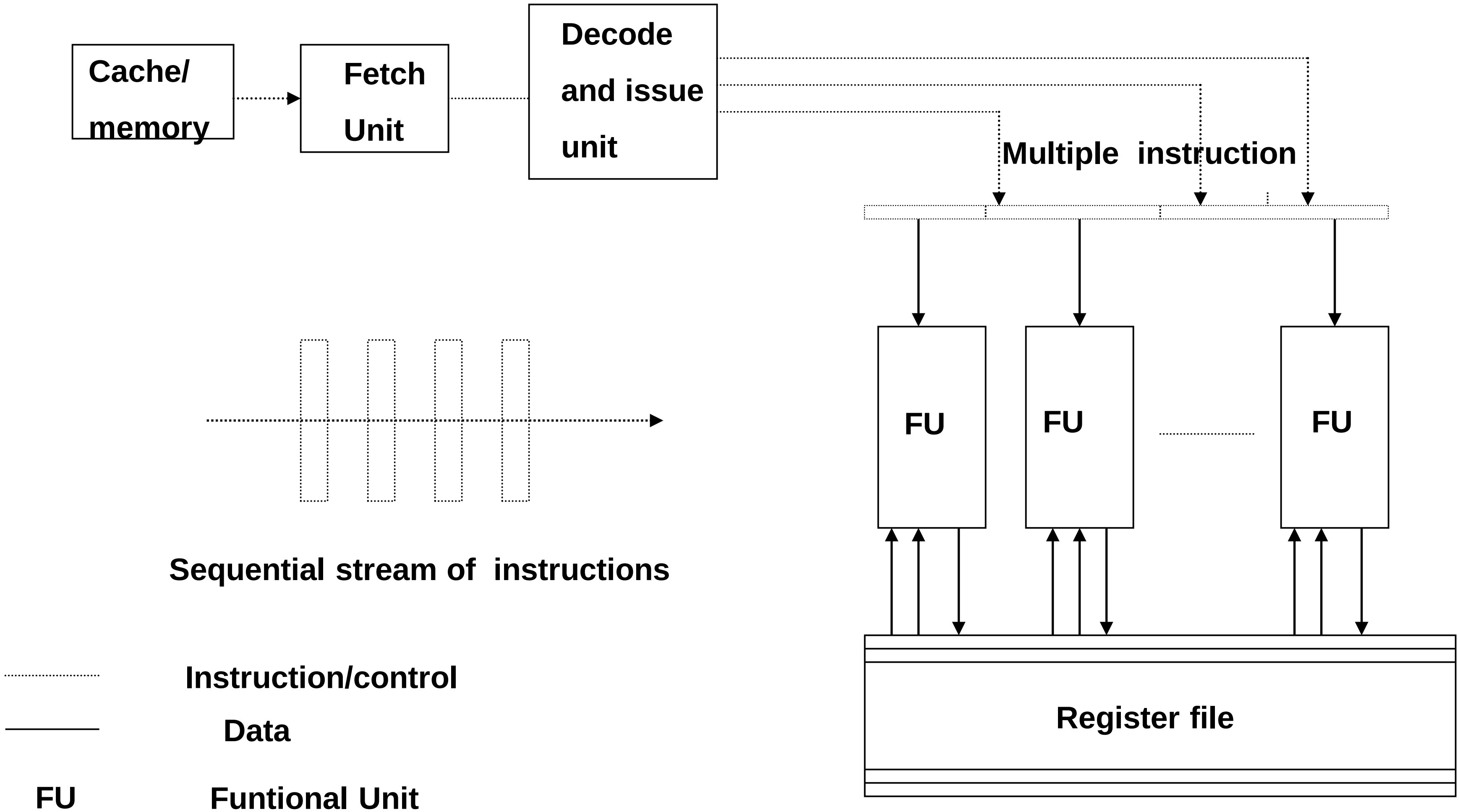
ILP in Superscalar processors



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Why Superscalars are popular ?

- Binary code compatibility among scalar & superscalar processors of same family
- Same compiler works for all processors (scalars and superscalars) of same family
- Assembly programming of VLIWs is tedious
- Code density in VLIWs is very poor - Instruction encoding schemes

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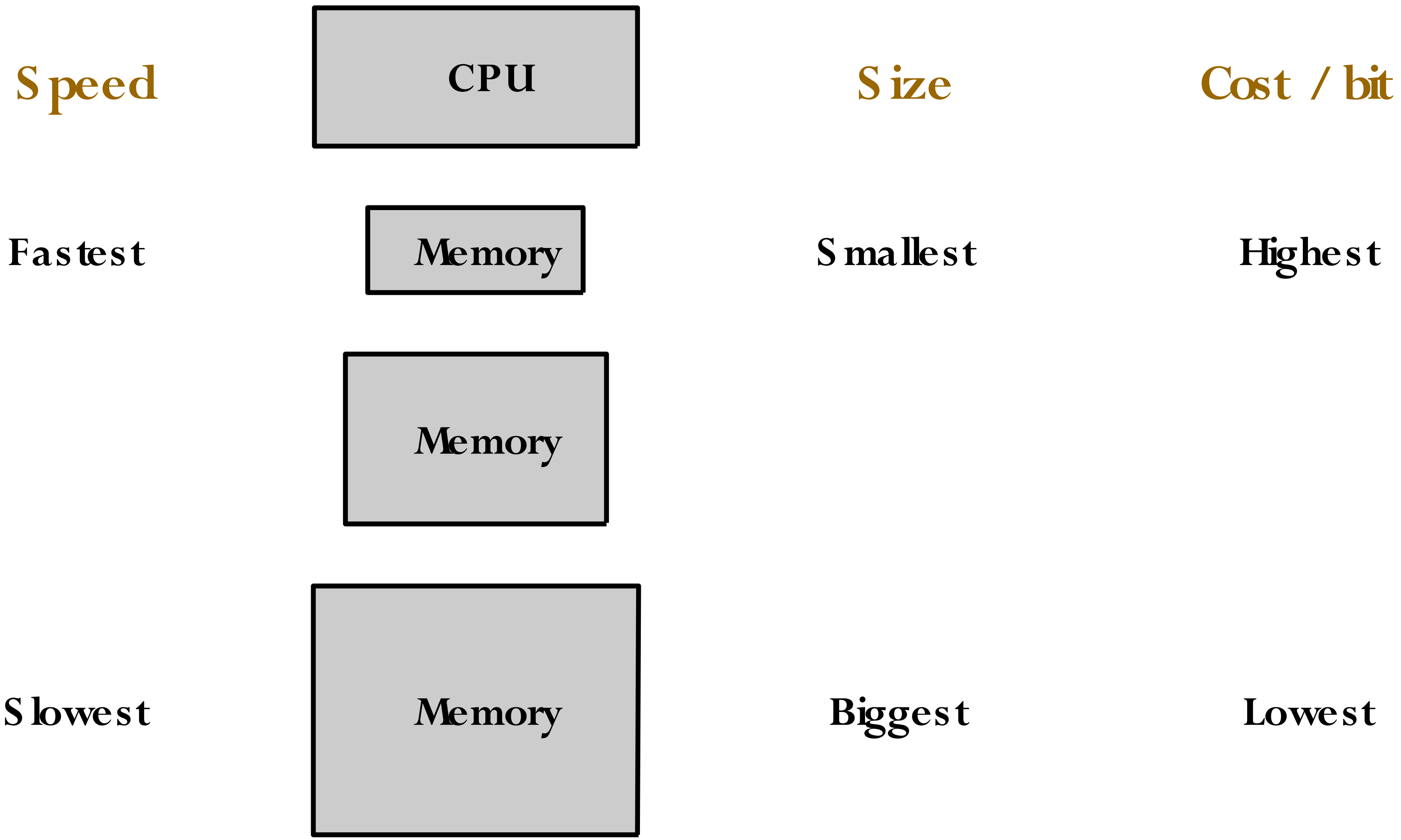
Hierarchical structure



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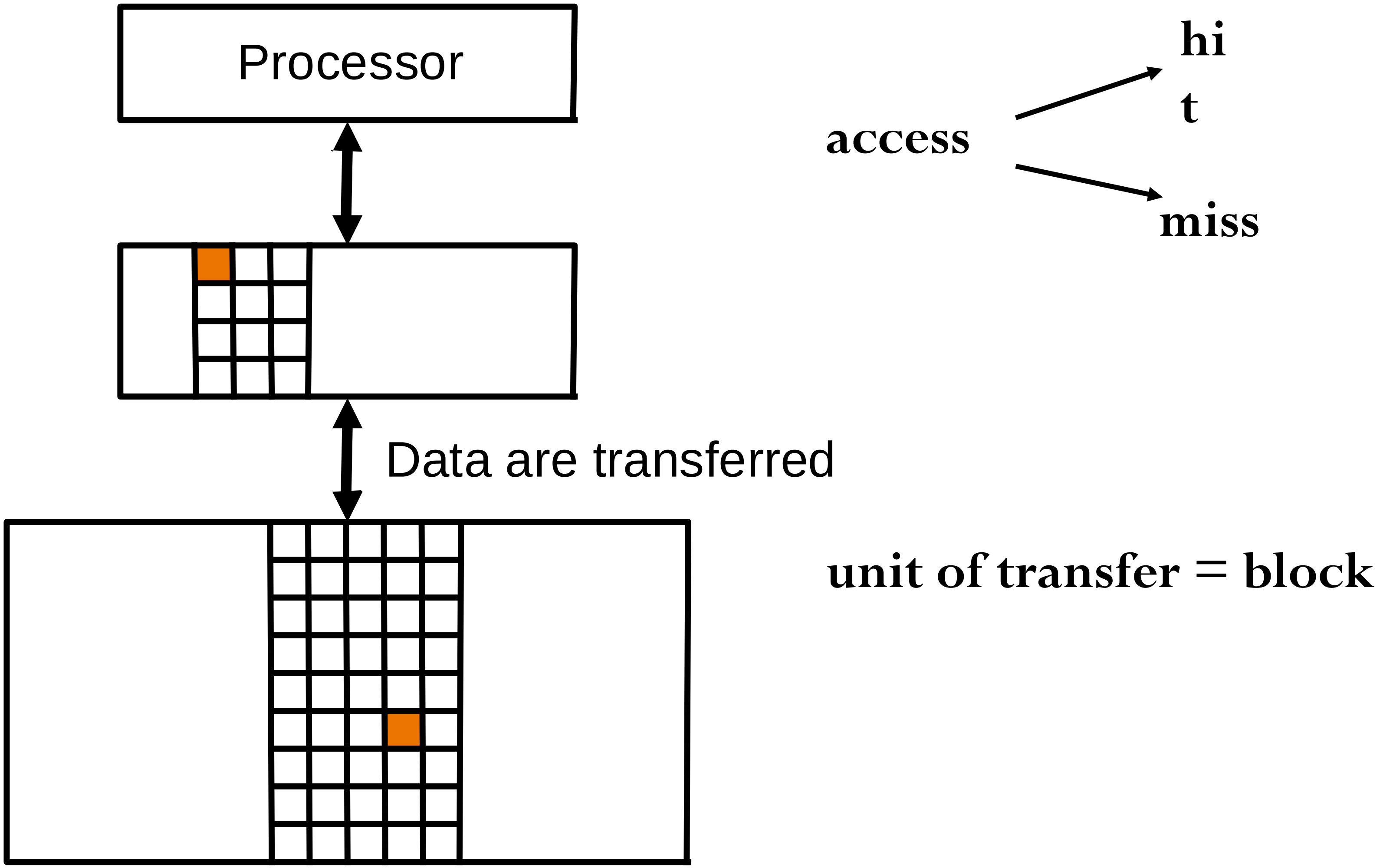
Data transfer between levels



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Principle of locality & Cache Policies

- Temporal Locality
  - references repeated in time
- Spatial Locality
  - references repeated in space
  - Special case: Sequential Locality

==============================

- **Read**
  - **Sequential / Concurrent**
  - **Simple / Forward**
- **Load**
  - **Block load / Load forward / Wrap around**
- **Replacement**
  - **LRU / LFU / FIFO / Random**

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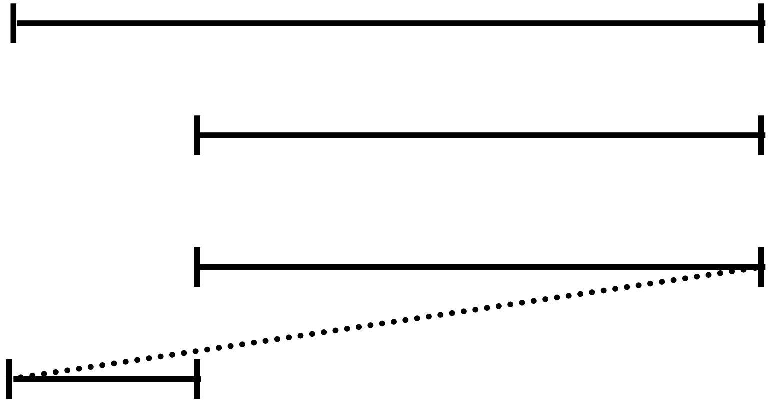
Load policies

Cache miss on AU 1



Block Load

Load Forward

Fetch Bypass (wrap around load)

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Fetch Policies

- Demand fetching
  - fetch only when required (miss)
- Hardware prefetching
  - automatically prefetch next block
- Software prefetching
  - programmer decides to prefetch

questions:

- how much ahead (prefetch distance)
- how often

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Write Policies

- Write Hit
  - Write Back
  - Write Through
- Write Miss
  - Write Back
  - Write Through
    - With Write Allocate
    - With No Write Allocate

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Cache Types

Instruction | Data | Unified | Split

Split vs. Unified:

- Split allows specializing each part
- Unified allows best use of the capacity

On-chip | Off-chip

- on-chip : fast but small
- off-chip : large but slow

Single level | Multi level

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2. Sima, T, FOUNTAIN, P KACSUK, *Advanced Computer Architectures: A Design Space Approach*, Pearson Education, 1998
3. Flynn M J, *Computer Architecture: Pipelined and Parallel Processor Design*, Narosa publishing India, 1999
4. John L. Hennessy, David A. Patterson, Computer architecture: a quantitative approach, 2nd Ed, Morgan Kauffman, 2001

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8085 Architecture &
Its Assembly language programming

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Outline

- 8085 Era and Features
- 8085
  - Pin diagram
  - Block diagram (Data Path)
  - Bus Structure
  - Register Structure
- Instruction Set of 8085
- Sample program of 8085
- Simulator & Kit for 8085

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8085 Microprocessor

- 8 Bit CPU
- 3-6Mhz
- Simpler design: Single Cycle CPU
- 40 Pin Dual line Package
- 16 bit address
- 6 registers: B, C, D, E, H,L
- Accumulator 8 bit

Note: Architecture of 8085 microprocessor - GeeksforGeeks

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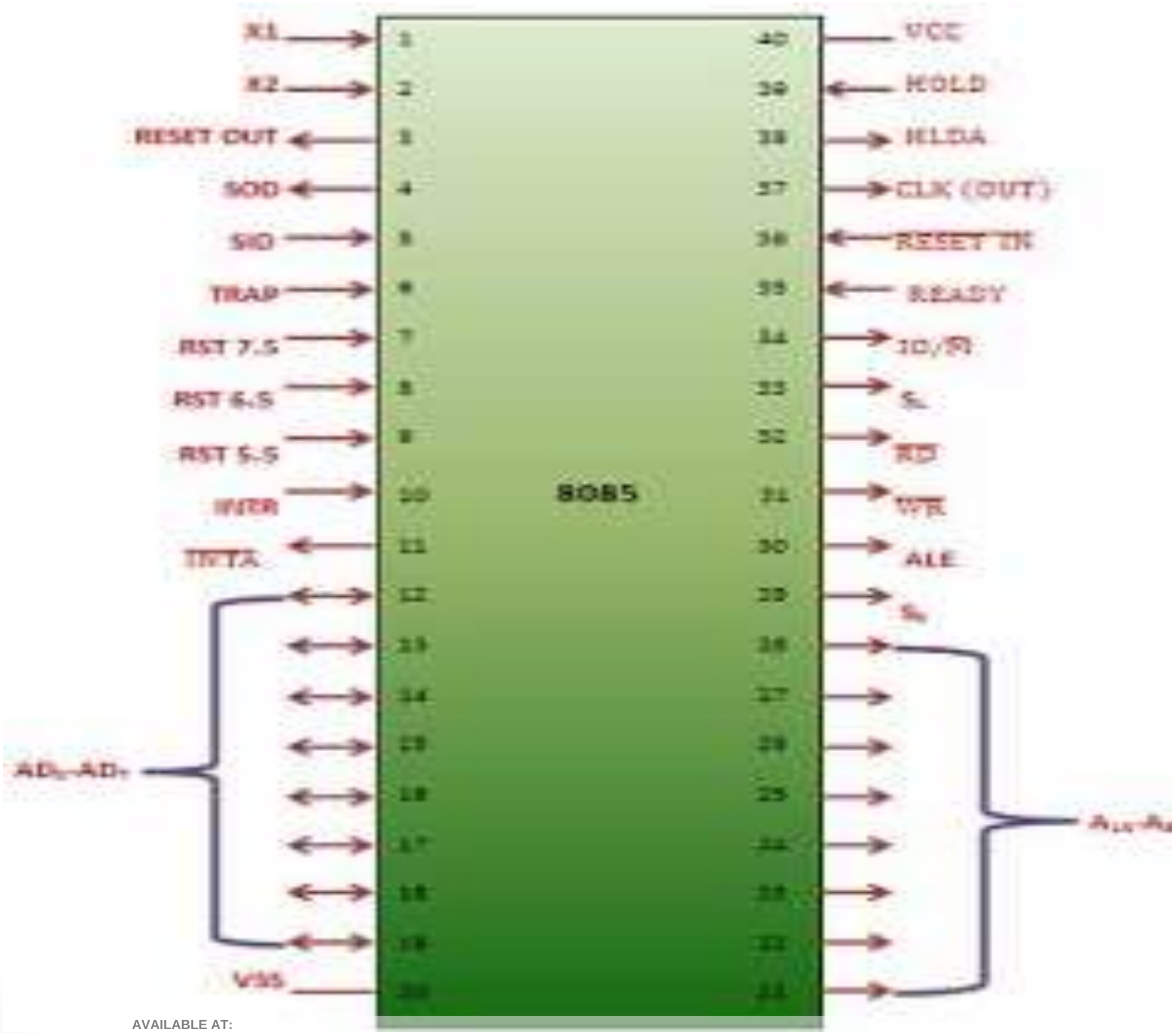
8085 Pin diagram



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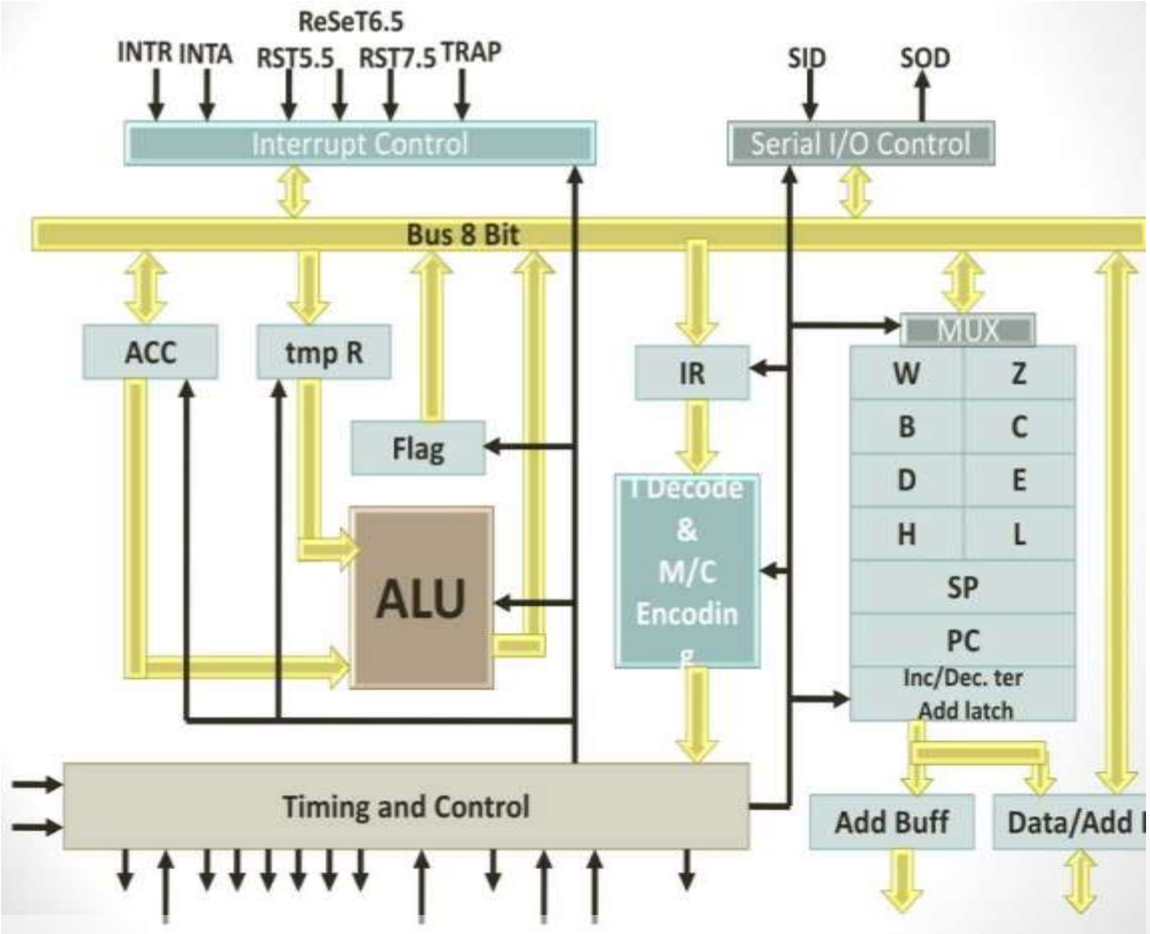
8085 Microprocessor Architecture

The Block Diagram of 8085 Microprocessor



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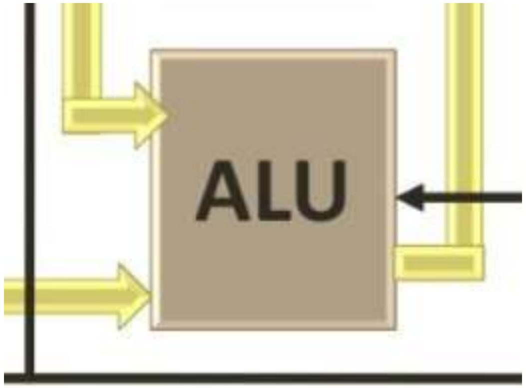
ALU

- **ALU (Arithmetic and Logic Unit):**
- Performs 8-bit operations such as addition, subtraction, AND, OR, and XOR.
- Interacts with the Accumulator (ACC) and Temporary Register (temp R).



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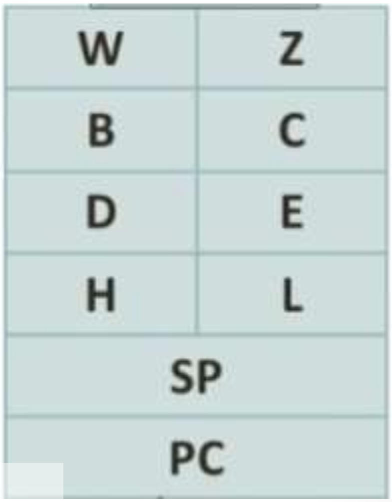
Registers

- **Accumulator (ACC)**
- **Temporary Register (tmp R):** Used internally by the ALU during operations.
- **Flag Register**
- **W, Z Registers:** Temporary storage.
- **General-Purpose Registers**
- **Stack Pointer (SP) and Program Counter (PC)**



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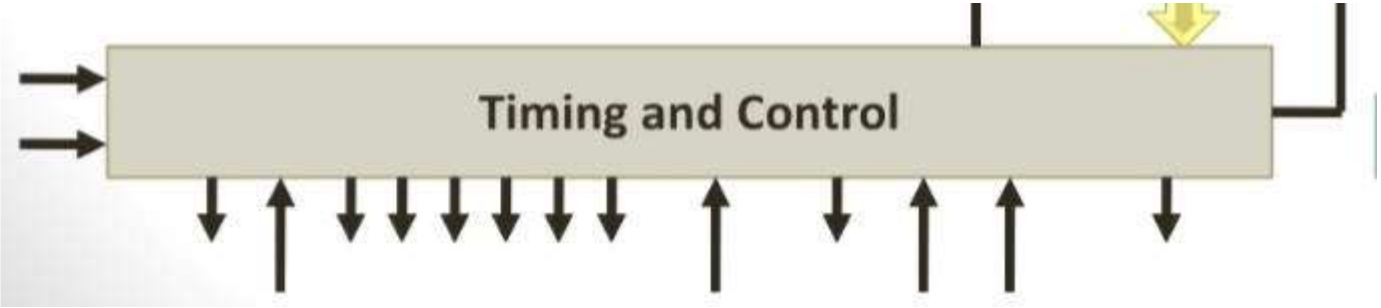
Timing and Control Unit

- Synchronizes and controls the execution of instructions.
- Generates necessary control signals (RD, WR, ALE) and status signals (IO/M, S0, S1).
- Manages the clock cycles and fetch-execute cycle for instructions.



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Interrupt Control Unit

- Manages five interrupt signals: INTR, RST5.5, RST6.5, RST7.5, TRAP.
- TRAP: Non-maskable interrupt with the highest priority.
- RST5.5, RST6.5, RST7.5: Maskable, vectored interrupts.
- INTR and INTA (Interrupt Acknowledge): General-purpose interrupt and its acknowledgement.

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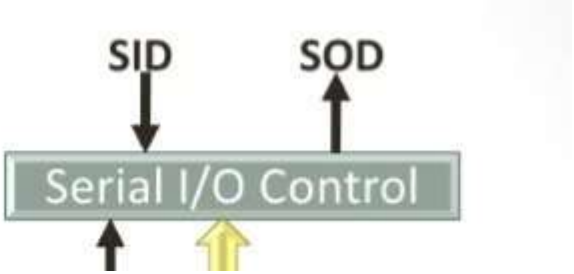
Serial I/O Control Unit

- **Serial I/O Block:**
- Facilitates serial communication through:
- SID (Serial Input Data): Receives serial data.
- SOD (Serial Output Data): Sends serial data.
- Used for communicating with serial peripherals or data transfer over long distances.



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Data and Address Bus System

- **Data Bus (8-bit):**
- **Transports** 8-bit data between the microprocessor and peripherals or memory.
- **Address Bus (16-bit):**
- Carries memory and I/O addresses to access data or instructions.
- **Add Buffer and Data/Address Latches:**
- Temporarily store data and addresses to manage timing during bus transactions.

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Multiplexer and Program Counter

- **Multiplexer (MUX):**
-
- Combines data inputs from various sources like the registers and flags to pass them onto the appropriate internal bus lines.
- **Program Counter (PC):**
-
- Holds the address of the next instruction to be executed.
- Increments automatically as instructions are executed.

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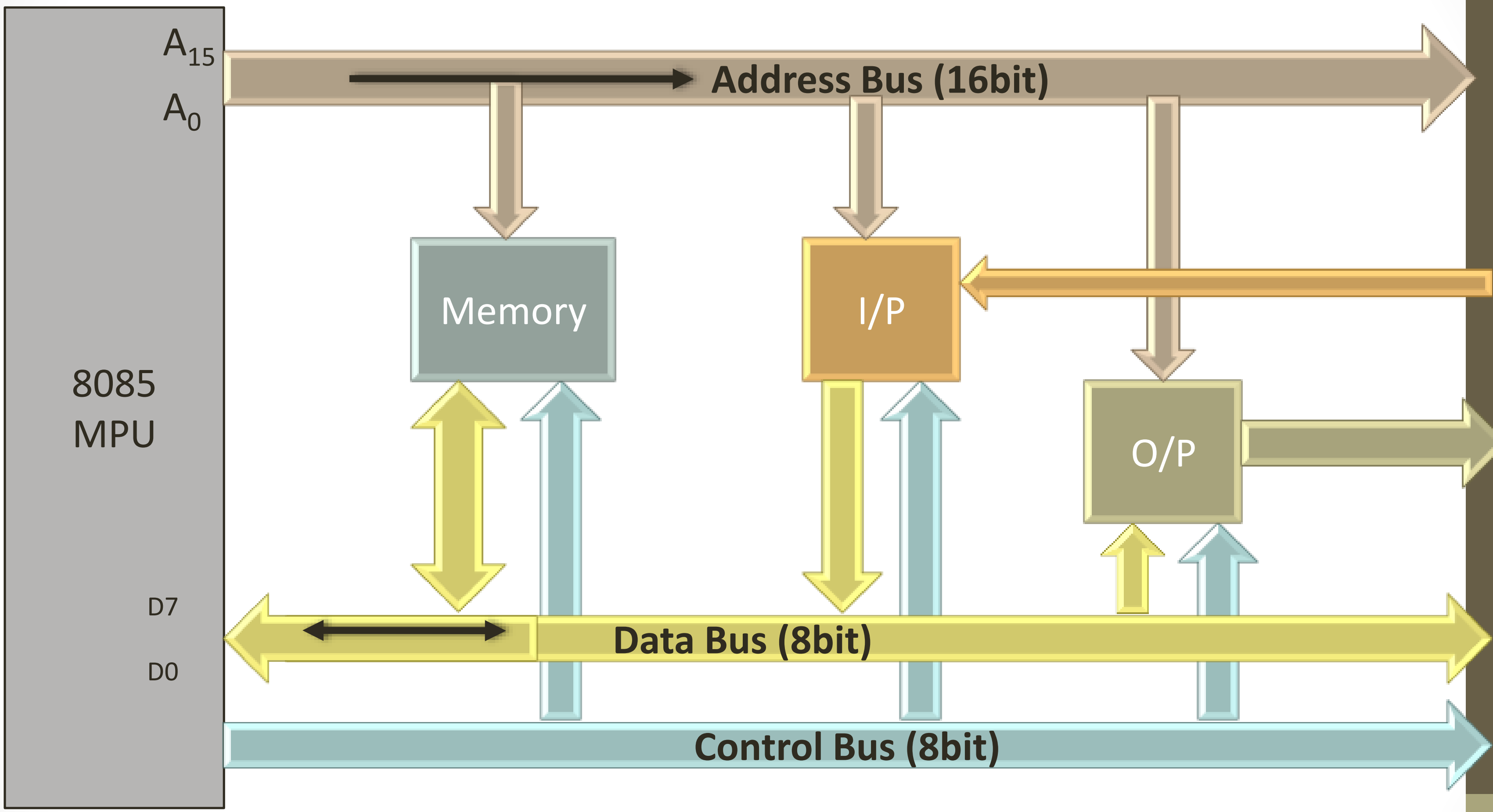
The 8085 Bus Structure



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8085 Bus Structure

1. **Address Bus:** A collection of wires used to identify location in main memory is called Address Bus. It is a group of 16 lines generally marked as A0 to A15. It is unidirectional which flow from microprocessor to Input Output devices. The address bus carries address bits. It is used to identify IO peripheral or a memory location.
2. **Data Bus:** A collection of wires through which data is transmitted from one part of a computer to another is called Data Bus. It is a group of 8 lines used for data flow generally mark as D0 to D7. These lines are bidirectional. This bus connects all the computer components to the CPU and main memory. Data flow in both directions between microprocessor and memory.
3. **Control bus :**

The control bus is a bidirectional bus that is used to carry control signals between the microprocessor and other components such as memory and I/O devices. It is used to transmit commands to the memory or I/O devices

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8085 Bus Structure

performing specific operations.

1. Memory read
2. Memory write
3. I/O read
4. I/O Write
5. Opcode fetch

Why use Bus organization in 8085 microprocessor ?

1. Memory access
2. I/O operations
3. Control signal transfer
4. DMA operations

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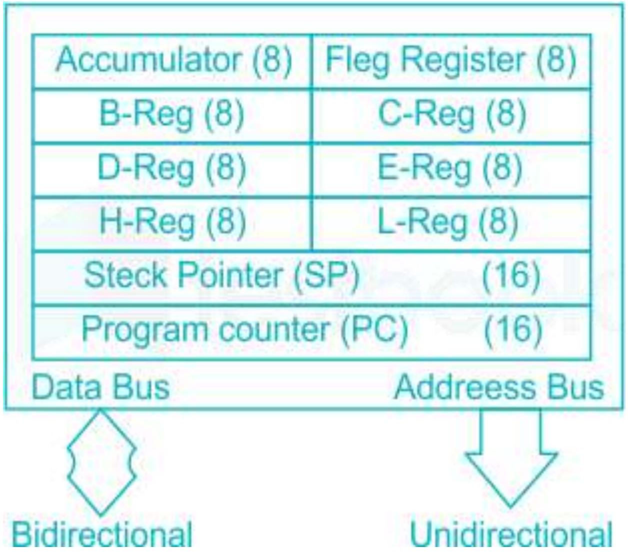
8085 Registers

- **(a) General Purpose Registers**:
  - Six general purpose 8-bit registers: B, C, D, E, H,L
  - Combined as register pairs to perform 16-bit operations: BC, DE, HL
  - Registers are programmable (load, move, etc.)



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Register 1

(b) Specific Purpose Registers –

Accumulator: an 8-bit register

Flag registers:5 flag registers are:

- ***Carry Flag (CF) :*** It occupies the zero th bit of the flag register. If the arithmetic operation results in a carry(if result is more than 8 bit), then Carry Flag is set; otherwise it is reset.
- ***Parity Flag (PF) :*** It occupies the second bit of the flag register. This flag tests for number of 1's in the accumulator. If the accumulator holds even number of 1's, then this flag is set and it is said to even parity. On the other hand if the number of 1's is odd, then it is reset and it is said to be odd parity.

B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
S	Z	—	AC	—	P	—	CY

fig(a)-Bit position of various flags in flag registers of 8085

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Register 2

- ***Auxiliary Carry Flag (AF)*** : AF = 1 if there is a carry out from bit 3 on addition, or a borrow into bit 3 on subtraction.
- ***Sign Flag (SF) :*** It occupies the seventh bit of the flag register, which is also known as the most significant bit. It helps the programmer to know whether the number stored in the accumulator is positive or negative. If the sign flag is set, it means that number stored in the accumulator is negative, and if reset, then the number is positive.
- ***Zero Flag (ZF)*** *:* It occupies the sixth bit of the flag register. It is set, when the operation performed in the ALU results in zero(all 8 bits are zero), otherwise it is reset. It helps in determining if two numbers are equal or not.

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Register 3

(c) Memory Registers – There are two 16-bit registers used to hold memory addresses.

- **Program Counter:** This register is used to sequence the execution of the instructions.
- **Stack Pointer:** It is used as a memory pointer. It points to a memory location in read/write memory, called the stack.

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How instruction executed

- All instructions (of a program) are stored in memory.
- To run a program, the individual instructions must be read from the memory in sequence, and executed.
  - Program counter puts the 16-bit memory address of the instruction on the address bus
  - Control unit sends the Memory Read Enable signal to access the memory
  - The 8-bit instruction stored in memory is placed on the data bus and transferred to the instruction decoder
  - Instruction is decoded and executed

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Instruction Set of 8085

- **Arithmetic Operations**
  - ADD, SUB, INR/DCR
  - Example *:' ADD B', 'SUB C'*
- **Logical operation**
  - AND, OR, XOR, Rotate(RLC,RRC), Compare(CMP), Complement.
  - Example : *'CMP E'*
- **Branch operation**
  - Jump(JMP), CALL, Return(RET)
  - Example *: 'JMP 2000H'*
- **Data transfer/Copy/Memory operation/IO**
  - MOV, MVI, LD, ST, OUT
  - Example : *'MOV A,B'*

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Copy/Mem/IO operation

- **MVI R, 8 bit** *// load immediate data*

  Example: MVI A, 25H
- **MOV R1, R2**

  Example : MOV B, A

- **MOV R M** *// Copy to R from address pointed by (HL Reg)*

  Example : If HL points to '2000H' , 'MOV B,M' load the contents of '2000H' into register B.

- **MOV M R** *// Copy from R to (HL Reg)*

  Example : If HL points to '2000H' and B has '05H', 'MOV M,B' stores '05H' at memory location '2000H'

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Copy/Mem/IO operation

- **LDA 16 bit** *// load A from (16bit)*

  Example: 'LDA 2000H'
- **STA 16 bit** *// Store A to (16bit)*

  Example : 'STA 2000H'
- **LDAX Rp** *// Load A from address pointed by (Rp) Rp=Register Pair*

  Example : If BC = 3000H, 'LDAX B' loads A with the contents of memory location 3000H.
- **STAX Rp** *// Store A to (Rp)*

  Example : If DE = 4000H and A = 0AH, 'STAX D' stores 0AH at memory location 4000H.
- **LXI Rp 16bit** *// load immediate to Rp*

  Example : 'LXI H, 3000H'

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Arithmetic Operation

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- **ADD R** (Add Register to Accumulator) // **SUB R** (Subtract Register from Accumulator)
  - **Description: This instruction adds the content of a specified register (B, C, D, E, H, L) to the Accumulator (A). The result is stored in the Accumulator..**
  - **Syntax: ADD R**
  - **Example: If A = 05H and B = 03H, after executing ADD B, A will become 08H.**
- **ADI 8-bit** (Add Immediate to Accumulator) // **SUI 8-bit** (Subtract Immediate from Accumulator)
  - **Description: This instruction adds an 8-bit immediate value to the Accumulator. The result is stored in the Accumulator.**
  - **Syntax: ADI 20H (data)**
  - **Example: If A = 05H and the immediate data is 03H, after executing ADI 03H, A will become 08H.**

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- **ADD M** (Add Memory to Accumulator) // **SUB M** (Subtract Memory from Accumulator)

  - Description: This instruction adds the content of the memory location pointed to by the HL register pair to the Accumulator. The result is stored in the Accumulator.

  - Syntax: ADD M

  - Example: If A = 05H, and HL points to memory location 2000H which contains 03H, after executing ADD M, A will become 08H.

- **INR R** (Increment Register) // **DCR R** (Decrement Register)

  - **Description: This instruction increments the content of the specified register by 1.**
  - **Syntax: INR R**
  - **Example: If B = 03H, after executing INR B, B will become 04H.**

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- **INR M** (Increment Memory) // **DCR M** (Decrement Memory)

  - Description: This instruction increments the content of the memory location pointed to by the HL register pair by 1.

  - Syntax: INR M

  - **Example: If the memory location 2000H contains 03H and HL points to 2000H, after executing INR M, the memory content at 2000H will become 04H.**

- **INX Rp** (Increment Register Pair) // **DCX Rp** (Decrement Register Pair)

  - Description: This instruction increments the content of the specified register pair (BC, DE, HL, or SP) by 1.

  - Syntax: INX Rp

  - Example: If HL = 2000H, after executing INX H, HL will become 2001H.

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Other Operations

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Logic Operations

- **ANA R**

  Example: If A = 0AH and B = 03H, after executing ANA B, A will become 02H

- **ANI 8bit**

  Example: If A = 0AH and the immediate value is 03H, after executing ANI 03H, A will become 02H

- **ANA M**

  Example: If A = 0AH and the memory location pointed to by HL contains 03H, after executing ANA M, A will become 02H.

- **ORA, ORI, XRA, XRI**

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- **CMP R** (Compare Register with Accumulator) // **CPI 8-bit** (Compare Immediate with Accumulator)

- Description: This instruction compares the content of the specified register with the Accumulator. The result is not stored, but the flags are set based on the comparison.

- Syntax: CMP R

- Example: If A = 05H and B = 03H, after executing CMP B, the Zero (Z) flag will be reset, indicating that A is greater than B.

(A – B) == 02H	ZF	CF	SF
A > B	0	0	0
A = B	1	0	0
A < B	0	1	1

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Branch Operations

- JMP 16-bit (Jump to Address) **Syntax:** JMP address   like : goto keyword in c++
- CALL 16-bit (Call Subroutine) **Syntax:** CALL address like : int sum(int a, int b) return a + b; in c++
- JZ 16-bit (Jump if Zero) **Syntax:** JZ address if(a == 0)
- JNZ 16-bit (Jump if Not Zero) **Syntax:** JNZ address if(a != 0)
- JC 16-bit (Jump if Carry) **Syntax:** JC address if(carry == 0)
- JNC 16-bit (Jump if No Carry) **Syntax:** JNC address if(carry != 0)
- RET (Return from Subroutine) **Syntax:** RET

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Machine Control Operations

- HLT (Halt) **Syntax:** HLT (Executing HLT will stop the microprocessor.) like : exit
- NOP (No Operation) **Syntax:** NOP
- POP (Pop Data Off Stack) **Syntax:** POP Rp
- PUSH (Push Data Onto Stack) **Syntax:** PUSH Rp

INTERRUPTED = (DI, EI…….) disable

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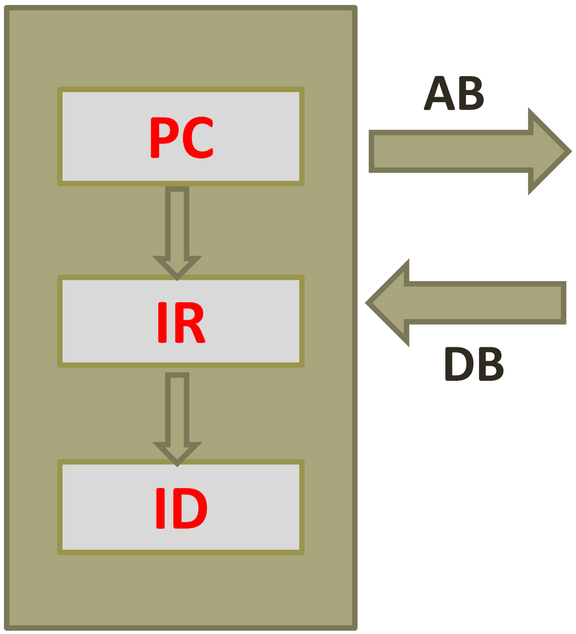
How Program Works



Instruction			Address
I1	MVI	A, 24H	1000
I2	MVI	B , 56H	1001
I3	ADD	B	1002

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Simple Assembly Program

Addition of Two 8-bit Numbers

if perform any (Add, Subtract, Multiply etc.) Operation one operand or value must be store accumulated register . And others value store temporary register.

```
MVI A, 0x12      ;  Load 0x12 into Accumulator
MVI B, 0x34      ;  Load 0x34 into register B
ADD B            ;  Add the content of B to Accumulator (A = A + B)
OUT 01H          ;  Display Result on port 01H
HLT              ;  Halt the program
```

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Q1: If I want to take input from user?

In 8085 assembly programming, the microprocessor does not have built-in support for direct input from a user (like Scanf() function in C langauge). Instead, user input is typically handled via **I/O ports** that connect to input devices.

1. **Input via IN Instruction**
2. **Example:**

```
MVI A, 00H      ; Load the port address into the Accumulator
IN 00H          ; Read data from port 00H into the Accumulator
MOV B, A        ; Move the input data from Accumulator to register B
HLT             ; Halt the program
```

3. **Input/Output Devices Setup**

- Connect input device to a particular I/O port on the 8085 microprocessor.
- Ensure that the device is mapped to a specific I/O port address (00H, 01H etc.)

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Q2: If I want to Add Two 16 bit Number ?

Steps to Add Two 16-bit Numbers:

- Split the 16-bit numbers into two 8-bit parts
- Add the lower bytes of both numbers and store the result
- Add the higher bytes of both numbers and store the result
- Store the result.

Example :

The **first** 16-bit number is stored in two consecutive memory locations

- Lower byte at memory location 2000H
- Higher byte at memory location 2001H

The **Second** 16-bit number is stored in two consecutive memory locations

- Lower byte at memory location 2002H
- Higher byte at memory location 2003H

The **result** of the addition will be stored in two consecutive memory locations

- Lower byte at memory location 2002H
- Higher byte at memory location 2003H

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Code to Add two 16 Bit number

```
//Load the First Number:
LXI H, 2000H
MOV A, M
INX H
MOV B, M

//Load and Add the Second Number:
LXI H, 2002H
ADD M
MOV L, A
INX H
ADC M
MOV H, A

//Store the Result:
LXI D, 2004H
MOV M, L
INX D
MOV M, H

HLT
```

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Multiplication & Division

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Flowchart to multiply two number

Start

```
LDA   2000     // Load multiplicant to accumulator
MOV  B,A       // Move multiplicant from A(acc) to B register
```

```
LDA   2001    // Load multiplier to accumulator
MOV  C,A      // Move multiplier from A to C
```

```
MOV  C,A      // Move multiplier from A to C
MVI   A,00    // Load immediate value 00 to ACC
```

```
ADD    B     // Add B(multiplier) with A
DCR    C     // Decrement C, it act as a counter
```

```
JNZ     L   // Jump to L if C!=0
```

```
STA    2010   // Store result in to memory
HLT           // End
```

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Code to multiply two number

```
    LDA   2000    // Load multiplicant to accumulator
    MOV  B,A      // Move multiplicant from A(acc) to B register
    LDA   2001   // Load multiplier to accumulator
    MOV  C,A     // Move multiplier from A to C
    MVI   A,00   // Load immediate value 00 to a
L:   ADD    B     // Add B(multiplier) with A
    DCR    C      // Decrement C, it act as a counter
    JNZ     L      // Jump to L if C reaches 0
    STA    2010  // Store result in to memory
    HLT            // End
```

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Code to get division of two number

```
LDA 3000      ; Load the dividend from memory location 3000 to accumulator (A)
MOV B, A      ; Move the dividend to register B
LDA 3001      ; Load the divisor from memory location 3001 to accumulator (A)
MOV C, A      ; Move the divisor to register C
MVI A, 00     ; Clear accumulator (A) for the quotient (A = 0)

L: CMP B      ; Compare the dividend (B) with the divisor (C)
JC END        ; If B < C (dividend < divisor), jump to END (division done)
SUB C         ; Subtract the divisor from the dividend (B)
INR A         ; Increment the accumulator (A), which holds the quotient
JMP L         ; Jump back to the label L and continue subtracting

END: STA 3010 ; Store the quotient in memory location 3010
MOV A, B      ; Move the remainder (B) to accumulator
STA 3011      ; Store the remainder in memory location 3011
HLT           ; Halt the program
```

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Factorial of a Program

```
       LXI SP, 27FFH ; Initialize stack pointer
       LDA 2200H ; Get the number
       CPI 02H ; Check if number is greater than 1
       JC LAST
       MVI D, 00H ; Load number as a result
       MOV E, A
       DCR A
       MOV C,A ; Load counter one less than number
       CALL FACTO ; Call subroutine FACTO
       XCHG ; Get the result in HL  // HL with DE
       SHLD 2201H ; Store result in the memory   // store HL at 0(16bit)
       JMP END
LAST:  LXI H, 000lH ; Store result = 01
END:   SHLD 2201H
       HLT
```

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Sub Routine for FACTORIAL

```
FACTO:      LXI H, 0000H
            MOV B, C ; Load counter
BACK:       DAD D   // double add ; HL=HL+DE
            DCR B
            JNZ BACK ; Multiply by successive addition
            XCHG ; Store result in DE // HL with DE
            DCR C ; Decrement counter
            CNZ FACTO ; Call subroutine FACTO
            RET ; Return to main program
```

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8085 Simulator & Kit

- 8085 Simulator is available
  - Course website
- 8085 Kit is available in HW Lab (CS422)
  - First test the program on Simulator and then go for the HW
  - Sometime Kit have Driver, IDE and Assembler

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8085 Architecture &
Its Assembly language programming

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Outline

- 8085
  - Block diagram (Data Path)
  - Instruction Set of 8085
- Sample program of 8085
- Counter & Time Delay
- Stack and Sub Routine
- Assignment on 8085
- Introduction to 8086 and 30x86 architecture
- 8085 and 8086 Comparison

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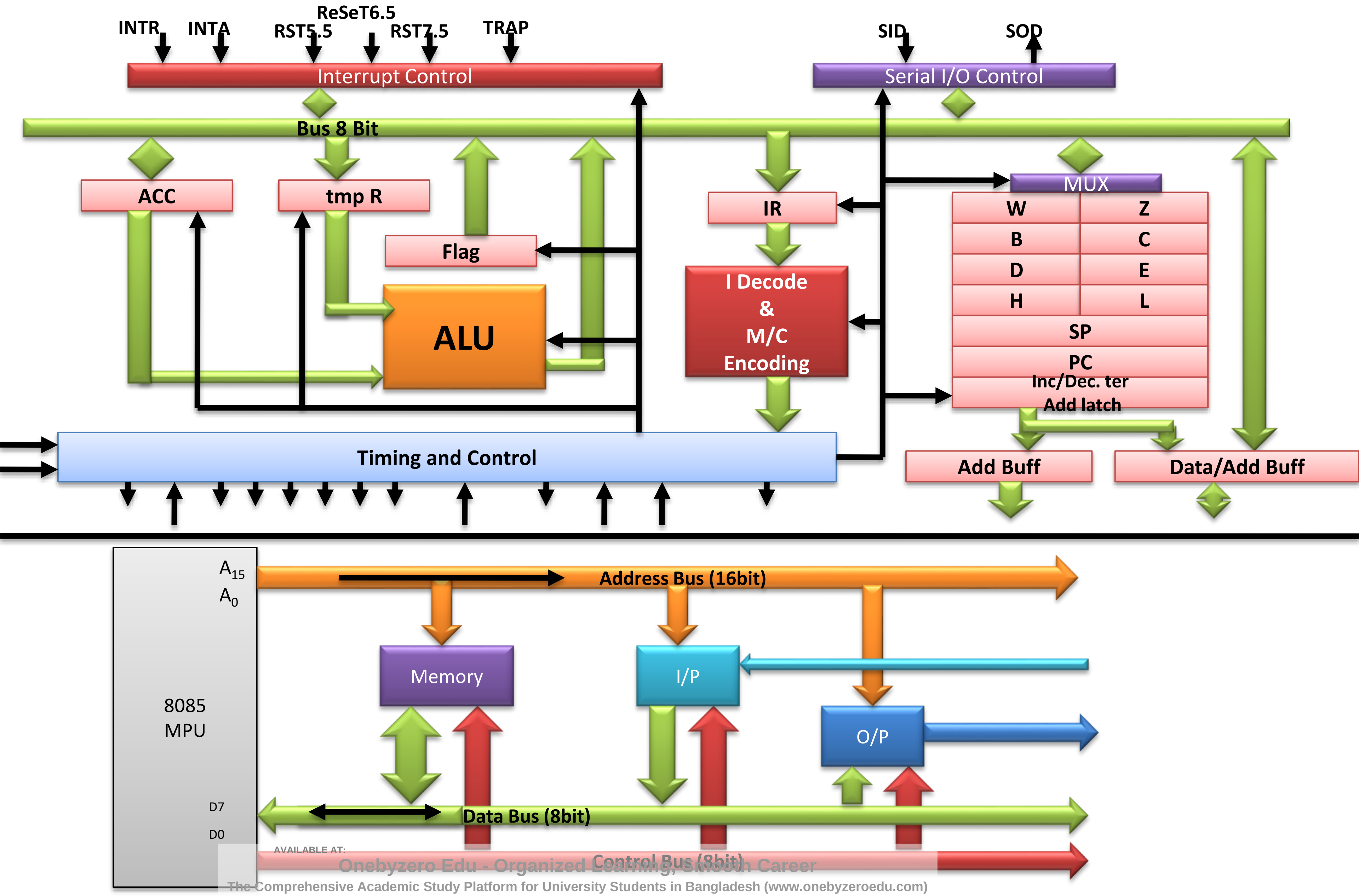
8085 Microprocessor Architecture



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The flow of an Instruction Cycle in 8085 Architecture :

- Program Counter starts program execution with the next address field .It fetches an instruction from the memory location pointed by Program Counter.

- For address fetching from the memory, multiplexed address/data bus acts as an address bus and after fetching instruction this address bus will now acts as a data bus and extract data from the specified memory location and send this data on an 8-bit internal bus. For multiplexed address/data bus Address Latch Enable(ALE) Pin is used. If ***ALE = 1 (Multiplexed bus is Address Bus otherwise it acts as Data Bus).***

- After data fetching data will go into the Instruction Register it will store data fetched from memory and now data is ready for decoding so for this Instruction decoder register is used.

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The flow of an Instruction Cycle in 8085 Architecture :

- After that timing and control signal circuit comes into the picture. *It sends control signals all over the microprocessor to tell the microprocessor whether the given instruction is for READ/WRITE and whether it is for MEMORY/I-O Device activity.*

- Hence according to timing and control signal pins, logical and arithmetic operations are performed and according to that data fetching from the different registers is done by a microprocessor, and mathematical operation is carried out by ALU. And according to operations Flag register changes dynamically.

- With the help of Serial I/O data pin(SID or SOD Pins) we can send or receive input/output to external devices .in this way execution cycle is carried out.

- ***While execution is going on if there is any interrupt detected then it will stop execution of the current process and Invoke Interrupt Service Routine (ISR)*** Function. Which will stop the current execution and do execution of the current occurred interrupt after that normal execution will be performed.

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Simple Assembly Program

```
MVI   A, 24H      // load Reg  ACC with 24H
MVI   B , 56H     // load Reg B with 56H
ADD   B           // ACC= ACC+B
OUT 01H           // Display ACC contents on port 01H
HALT              // End the program
```

Result: 7A (All are in Hex)

DAA operation for Decimal Adjust   A+6=10H

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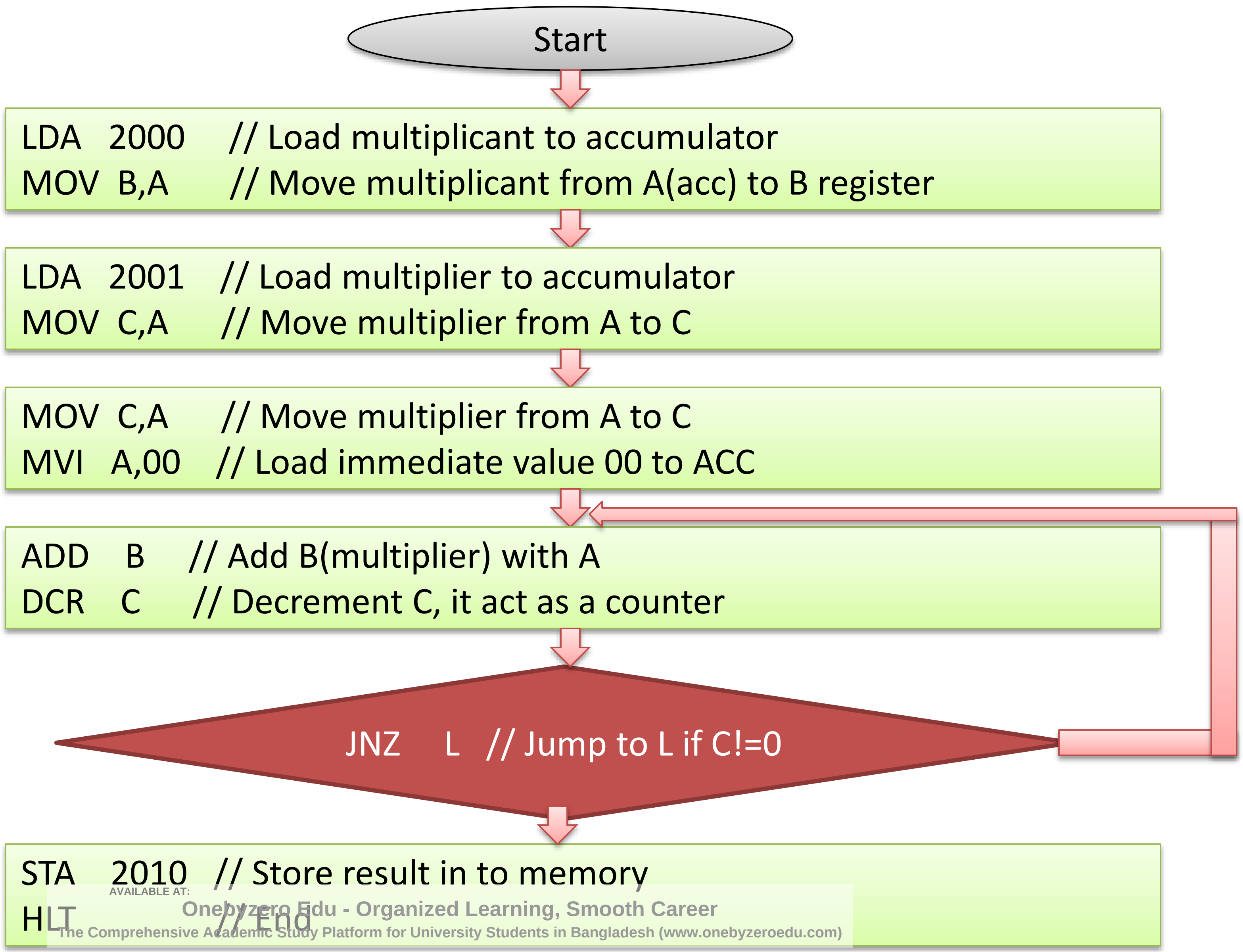
Flowchart to multiply two number



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Code to multiply two number

```
    LDA   2000     // Load multiplicant to accumulator
    MOV  B,A       // Move multiplicant from A(acc) to B register
    LDA   2001    // Load multiplier to accumulator
    MOV  C,A      // Move multiplier from A to C
    MVI   A,00    // Load immediate value 00 to a
L:  ADD    B      // Add B(multiplier) with A
    DCR    C       // Decrement C, it act as a counter
    JNZ    L       // Jump to L if C reaches 0
    STA    2010   // Store result in to memory
    HLT            // End
```

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Delay of Instructions

- Performance/delay of each instruction

MVI C, FFH	F R	7 T-State
LOOP: DCR C	F	4 T-State
JNZ LOOP	F R R	7/10 T-State

- Performance of other INS

ADD R	F	4 T-State
ADD M	F R	7 T-State
CALL addr	S R R W W	18 T-State

- F=Fetch with 4 State, S=Fetch with 6 State, R=Memory Read, W=Memory Write

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Time Delay Loop

- Performance/delay of each instruction

	MVI C, FFH	F R	7 T-State
LOOP:	DCR C	F	4 T-State
	JNZ LOOP	F R R	7/10 T-State

- Time delay in loop

T_L= T x Loop T-States x N_{10}

where T=System clock period

N_{10}= Equiv. decimal value of count loaded to C

$T_L = 0.5 \times 10^{-6} \times (14 \times 255) = 1.8$ms (ignore 10 T-State)

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Time Delay: Nested Loop

- Performance/delay of each instruction

MVI C, FFH	F R	7 T-State
MVI D, FFH	F R	7 T-State
LOOP1: DCR C	F	4 T-State
LOOP2: DCR D	F	4 T-State
JNZ LOOP2	F R R	7/10 T-State
JNZ LOOP1	F R R	7/10 T-State

- Time delay in Nested loop

$$T_{NL} = N1_{10} \text{ x } T \text{ x } (L1\_TStates + L2\_TStates \text{ x } N2_{10})$$

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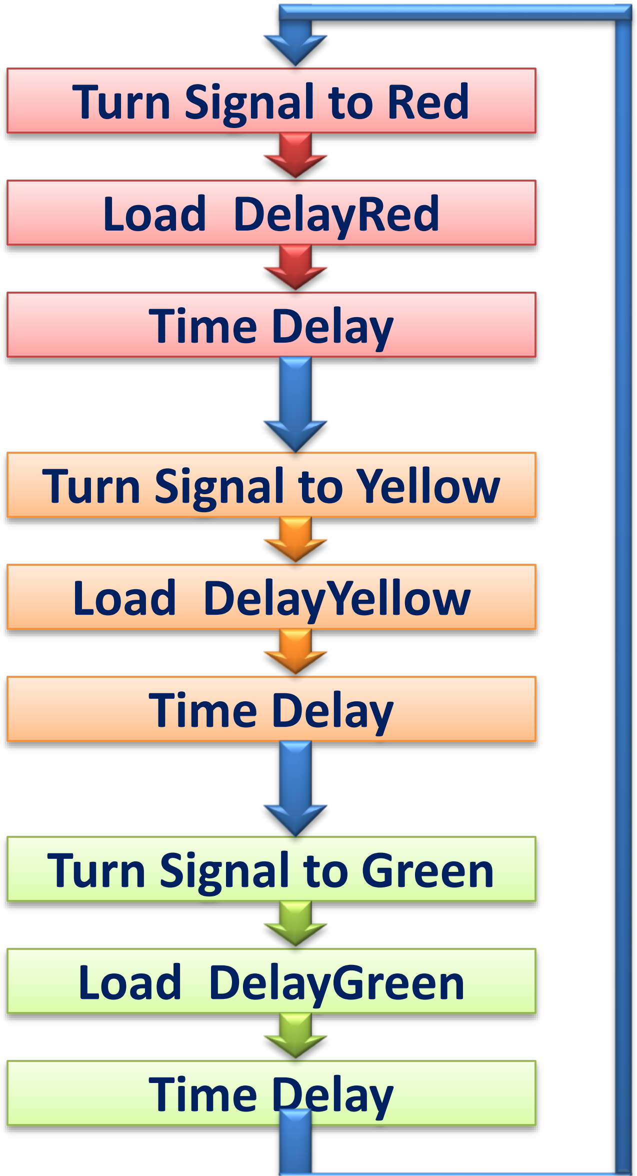
Traffic Light Control: Counter & Delay




```
LOOP:   MVI A 01H
        OUT 01H
        LD  B  DELAY_RED
        CALL DELAY

        MVI A 02H
        OUT 01H
        LD  B  DELAY_YELLOW
        CALL DELAY

        MVI A 03H
        OUT 01H
        LD  B  DELAY_GREEN
        CALL DELAY

        JMP  LOOP
```

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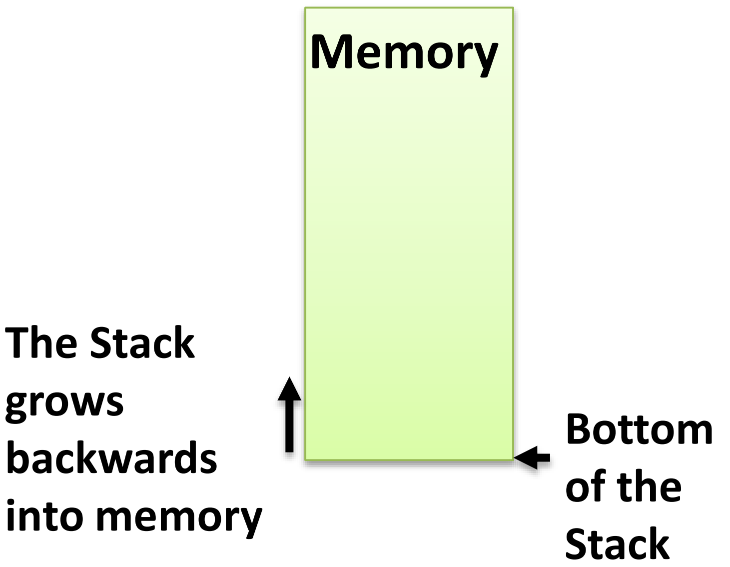
Stack Pointer (SP) & Stack Memory

- The stack is an area of memory identified by the programmer for temporary storage of information.
- The stack is a LIFO structure.
- The stack normally grows backwards into memory.
  - Programmer can defines the bottom of the stack (**SP**) and the stack grows up into reducing address range.



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Stack Memory

- Grows backwards into memory
- Better to place the bottom of the stack at the end of memory
- To keep it as far away from user programs as possible.
- Stack is defined by setting the SP (Stack Pointer) register.

  LXI SP, FFFFH
- This sets SP to location FFFFH (end of memory for 8085).

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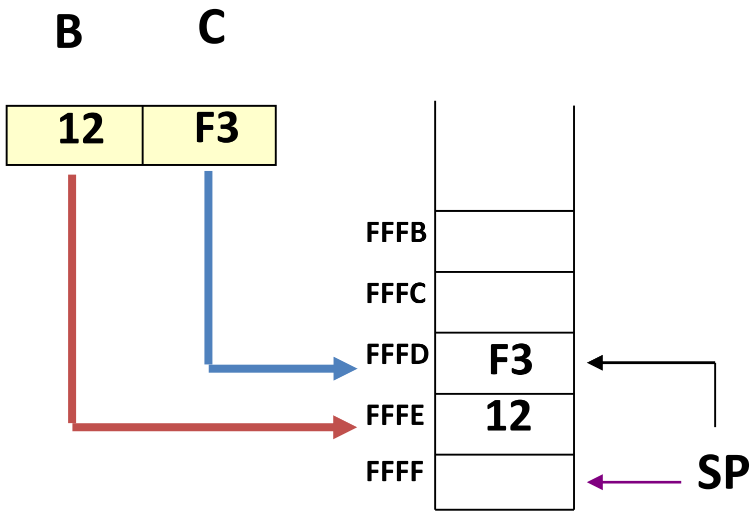
Saving Information on the Stack

- Save information by PUSHing onto STACK
- Retrieved from STACK by POPing it off.
- PUSH and POP work with register pairs only.
- Example "PUSH B"
  - Decrement SP, Copy B to 0(SP)
  - Decrement SP, Copy C tp 0(SP)
- Example "POP B"
  - Copy 0(SP) to C, Increment SP
  - Copy 0(SP) to B, Increment SP



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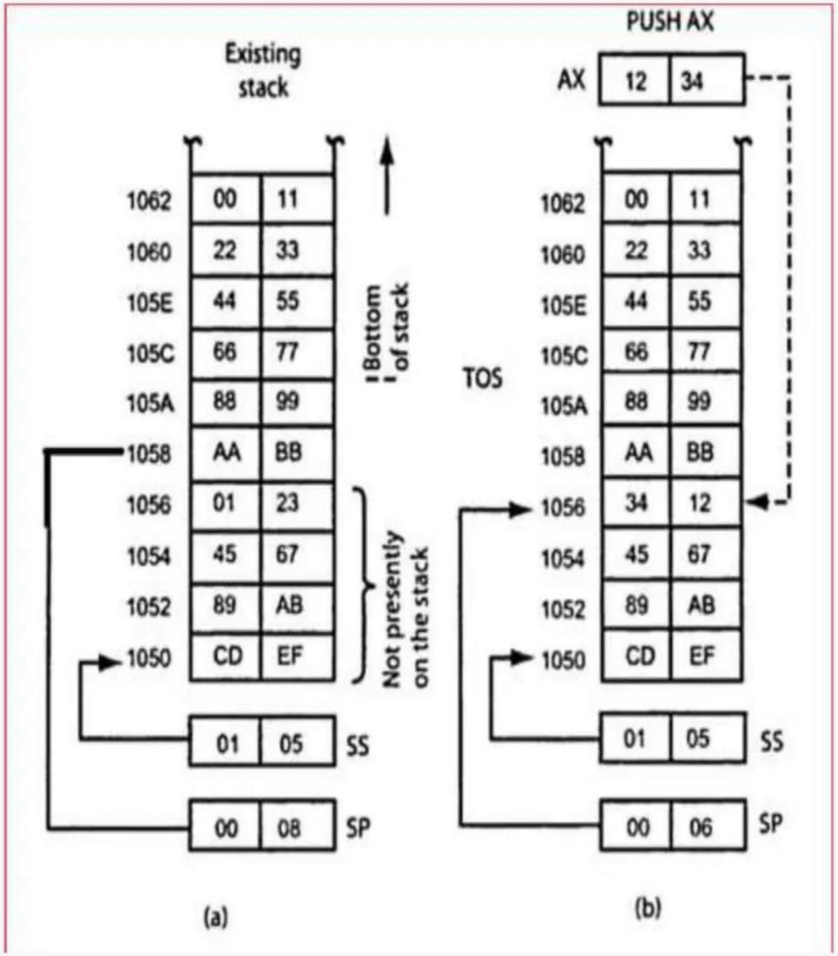
STACK STRUCTURE OF 8086: PUSH OPERATION

AX initially contains the number 1234H.

Execution of push instruction causes the stack pointer to be decremented by two.

Therefore the next stack access is to the location corresponding to address 1056H. This location is where the value in AX is pushed.

The MSB of AX (ie,12H) resides in memory address 1057H and LSB of AX (ie, 34H) is held in memory address 1056H



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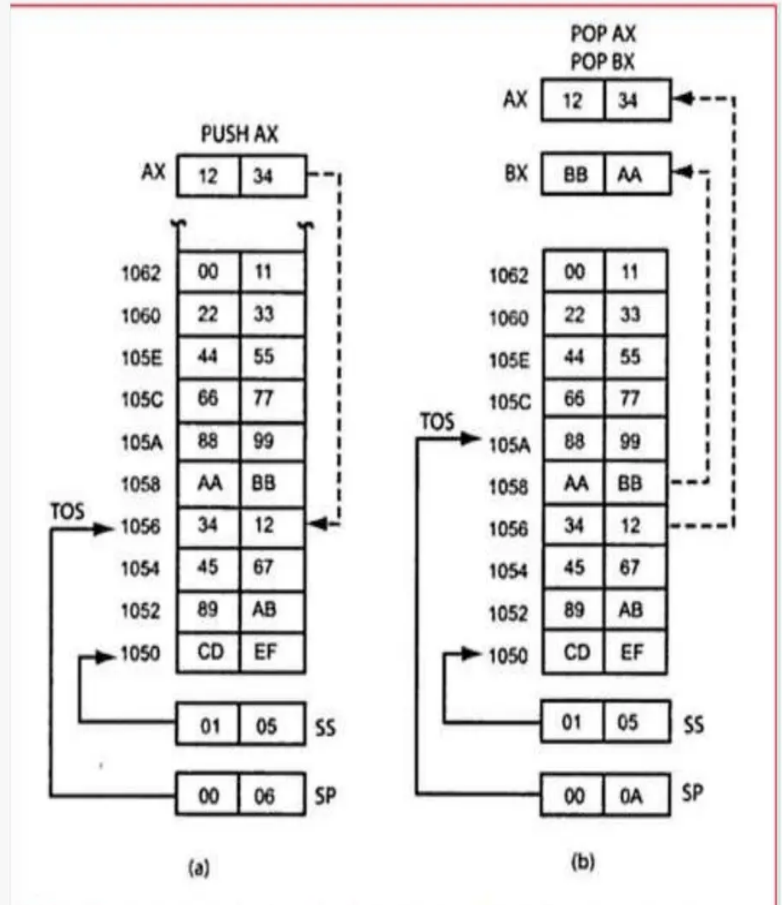
STACK STRUCTURE OF 8086: POP OPERATION

The execution of the first instruction POP AX, causes the 8086 to read the value from the Top of the stack and put it in to AX register as 1234H

SP is incremented to give 0008H and the other read operation POP BX, causes the value BBAAH to be loaded into the BX register.

SP is incremented once more and now equals 000AH. Therefore , the new top of stack is at address 105AH



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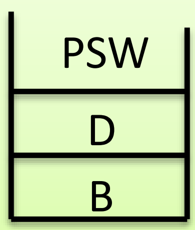
Stack/LIFO use in CALL/RET

- Retrieve information back into its original location
  - The order of PUSHs and POPs must be opposite
- 8085 recognizes one additional register pair
  - PSW (Prog Status word) = ACC and Flag

Before any routine CALL do this

PUSH B
PUSH D
PUSH PSW



After RETURN from call do this

POP PSW
POP D
POP B

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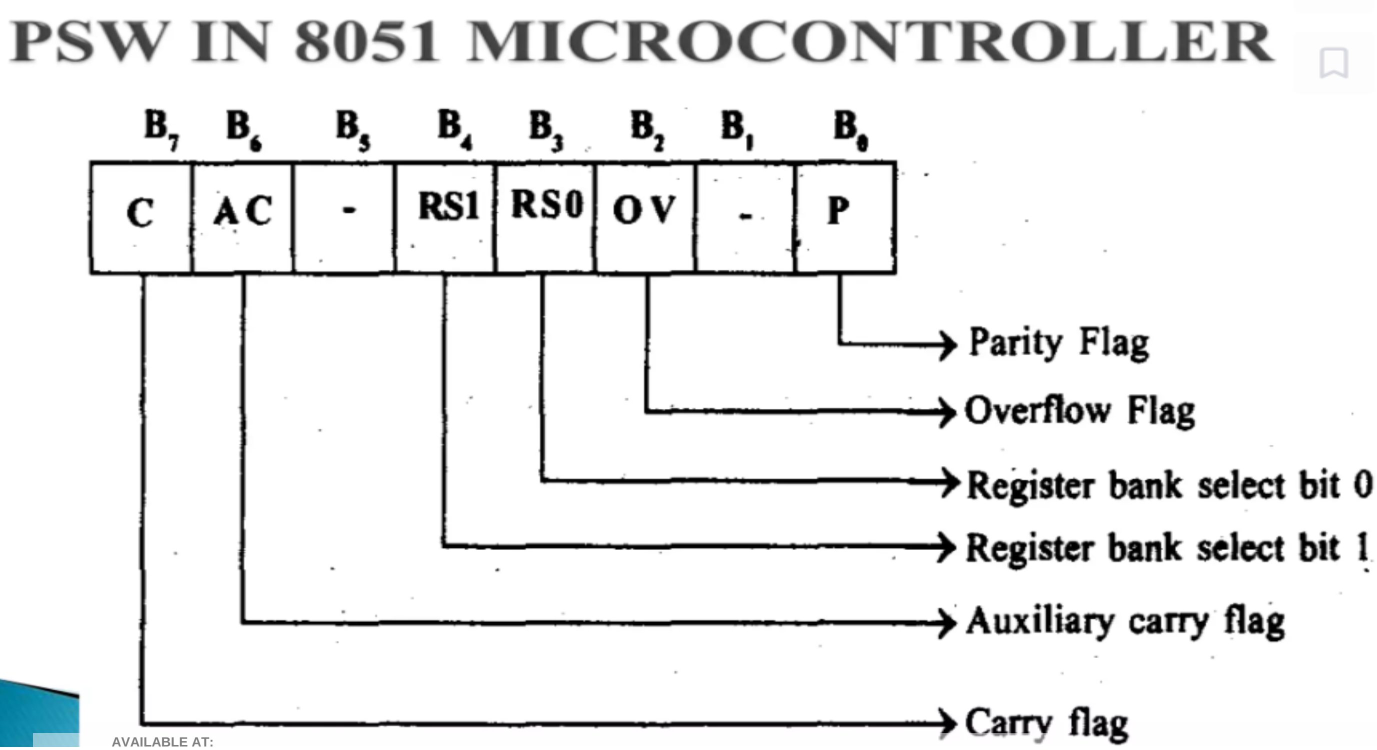
PSW

- Program Status Word stores the processor's current condition (PSW).
- It combines accumulator A and flag register F.
- 8 bits register



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Subroutines

- A subroutine is a group of instructions
  - That is used repeatedly in different places of the program.
  - Rather than repeat the same instructions several times
  - It can be grouped into a subroutine and call from the different locations.
- Instructions for dealing with subroutines.
  - The CALL instruction is used to redirect program execution to the subroutine.
  - The RET instruction is used to return the execution to the calling routine.

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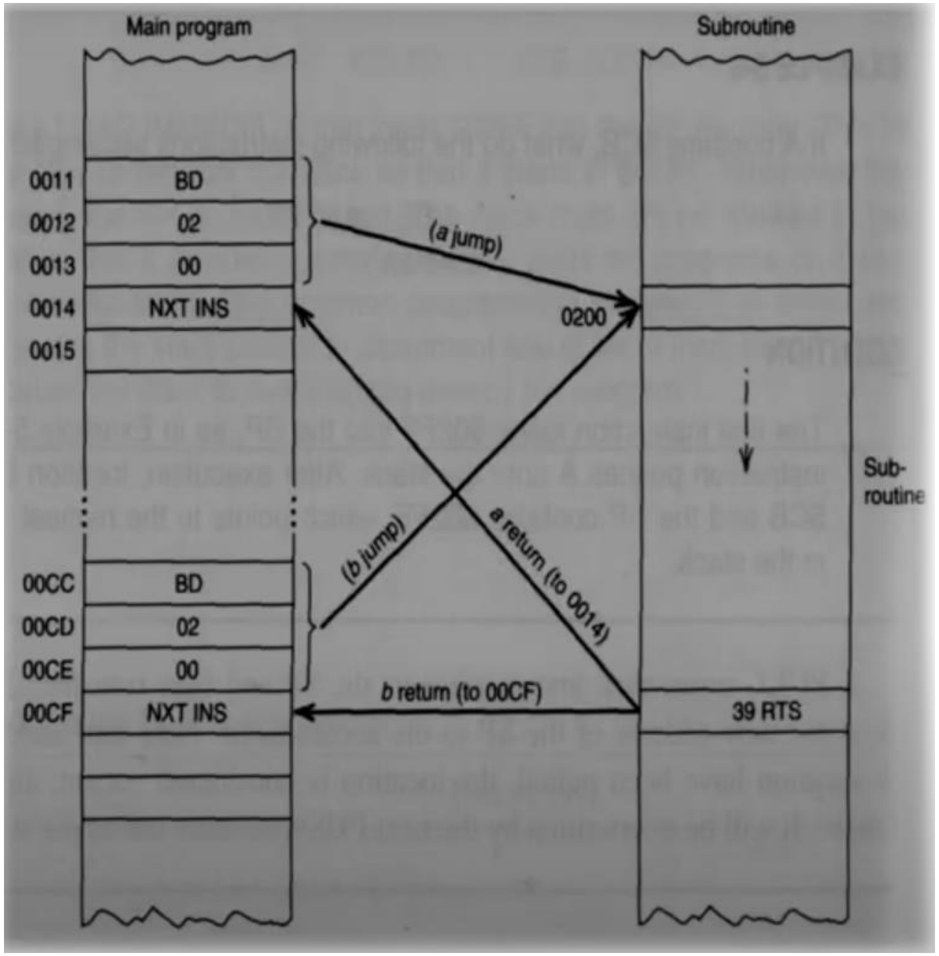
Subroutines



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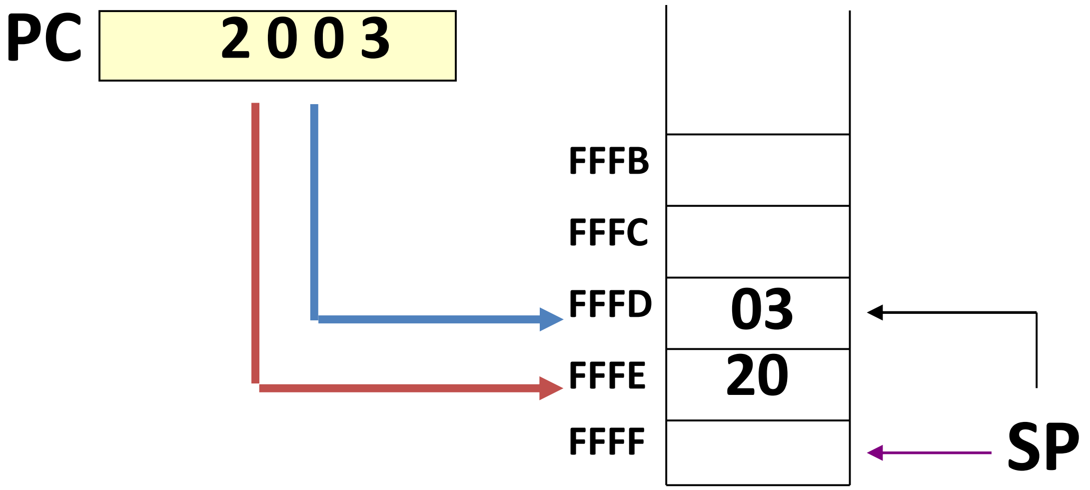
CALL/RET Instruction

- You must set the SP correctly before using CALL
- CALL 5000H
  - Push the PC value onto the stack
  - Load PC with 16-bit address supplied CALL ins.
- RET : Load PC with stack top;   POP PC

2000   CALL 5000

2003



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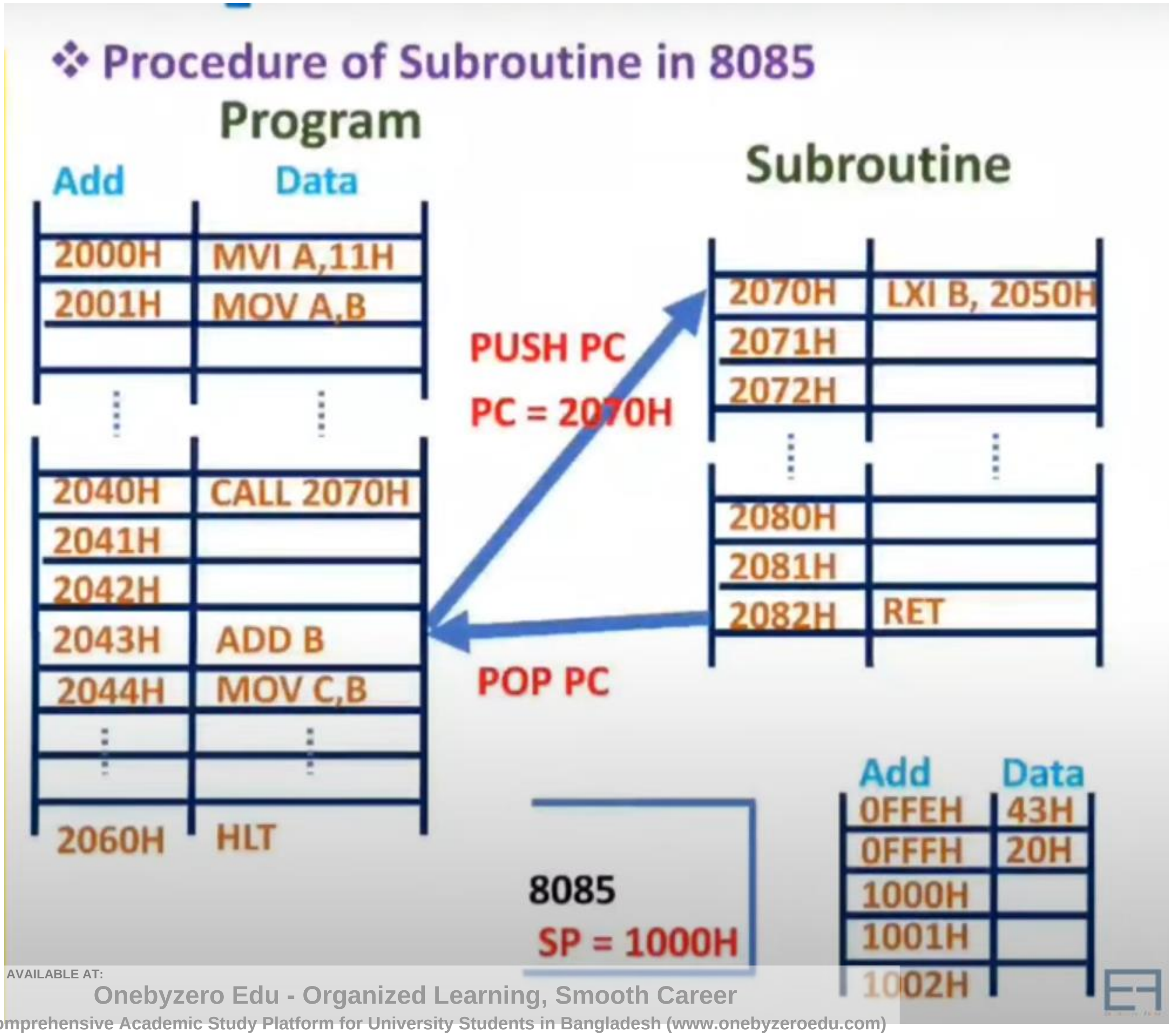
CALL/RET instruction



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Call by References

- Subroutines often manipulate data stored in registers.
- Changes made in the subroutine affect the calling program when returned.

Managing Changes:

- Use PUSH to save register states before entering the subroutine.
- Use POP to restore register states after the subroutine completes

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Stack and LIFO in Subroutine Calls

- PUSH commands save necessary registers before subroutine execution.
- POP commands restore registers after returning from the subroutine.

Example sequence:

Before Subroutine Call:
- ✓ PUSH B // Base Register
- ✓ PUSH D // Data Register
- ✓ PUSH PSW //Program Standard Word

After Subroutine Call:
- ✓ POP PSW
- ✓ POP D
- ✓ POP B

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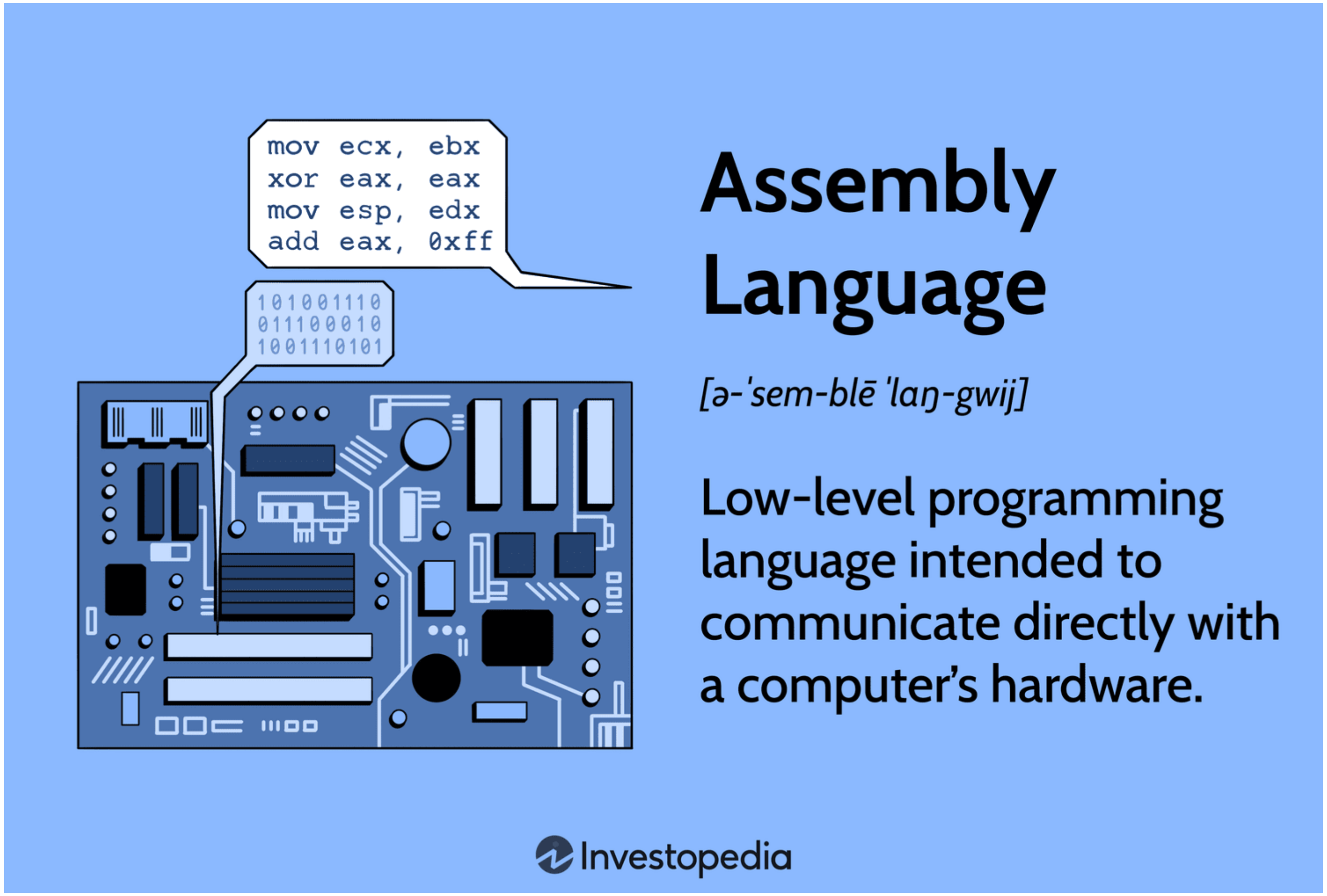
Assembly Language



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Factorial of a number

```
        LXI SP, 27FFH  // Initialize stack pointer
        LDA 2200H // Get the number
        CPI 02H // Check if number is greater than 1
        JC LAST
        MVI D, 00H  // Load number as a result
        MOV E, A
        DCR A
        MOV C,A  // Load counter one less than number
        CALL FACTO // Call subroutine FACTO
        XCHG  // Get the result in HL // HL with DE
        SHLD 2201H  // Store result // store HL at 0(16bit)
        JMP END
LAST:   LXI H, 000lH  // Store result = 01
END:    SHLD 2201H
        HLT
```

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Factorial Number using recursion

C factorial.c > main()

```c
#include<stdio.h>
long long int fact(long long int n)
{
    //base case
    while(n==0){
        return 1;
     }
     long long int ans=fact(n-1);
      return n*ans;

}
int main()
{
    long long int n;
    scanf("%lld",&n);
    long long int x =  fact(n);

 printf("%lld",x);
return 0;
}
```

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Sub Routine for FACTORIAL

```
FACTO:LXI H, 0000H
        MOV B, C  // Load counter
BACK:   DAD D   // double add ; HL=HL+DE
        DCR B
        JNZ BACK  //Multiply by successive addition
        XCHG  // Store result in DE // HL with DE
        DCR C  // Decrement counter
        CNZ FACTO  // Call subroutine FACTO
        RET   // Return to main program
```

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Assignment I

- Write and execute 8085 assembly language program to find value of N_{th} Fibonacci number (Recursive version: using recursive subroutine call)
- 16 bit can support up to 65356 > F_{24}

- Deadline: 12th Aug 2010, 11.55Mid night
- After deadline grading: Max 5 out of 10
- Send TXT version of program with file name RollNo.txt to asahu@iitg.ernet.in with Assignment one as subject of email
- Don't submit copied one: will get Negative marks

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Introduction to 8086 & i386 processor

- 16 bit Microprocessor
- All internal registers as well as internal and external data buses were 16 bits wide
- 4 Main Register, 4 Index Register, 4 Segment Register, Status Reg, Instr Ptr.
- Not compatible with 8085, but with successors
- Two Unit works in parallel:
  - Bus Interface Unit (BIU)
  - Execution Unit (EI)

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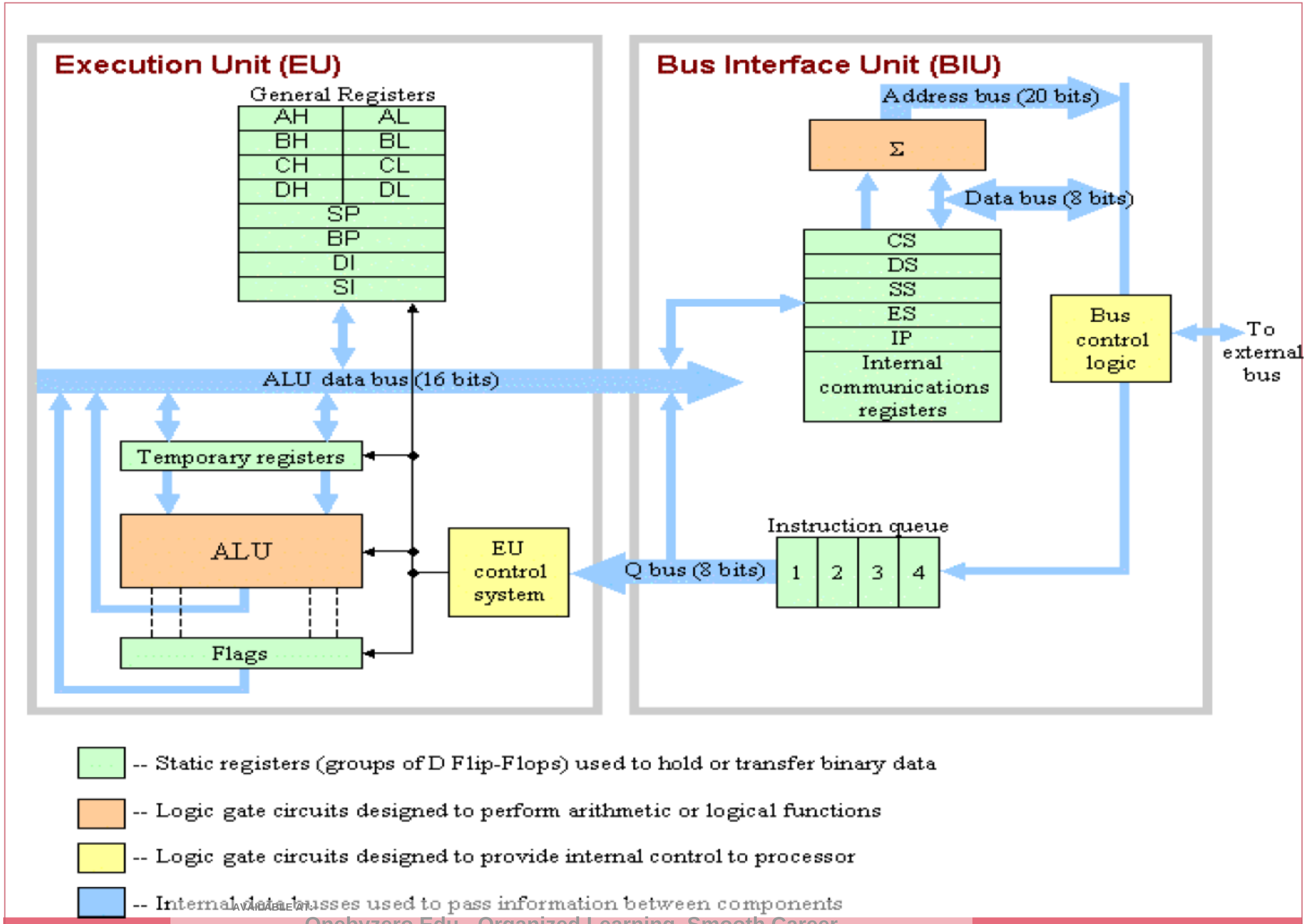
8086 Architecture



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Internal Architecture of 8086

- The 8086 microprocessor is internally divided into two separate functional units.
- These are the Bus Interface Unit (BIU) and the Execution Unit (EU). The BIU fetches instructions, reads data from memory and ports, and writes data to memory and I/O ports. The EU executes instructions that have already been fetched by the BIU. The BIU and EU function independently.
- The BIU's instruction queue is a First-In First-out (FIFO) group of registers in which up to six bytes of instruction code are perfected from memory ahead of time.
- The BIU contains a dedicated adder, which is used to produce the 20-bit address.
- The bus control logic of the BIU generates all the bus control signals such as read and write signals for memory and I/O.

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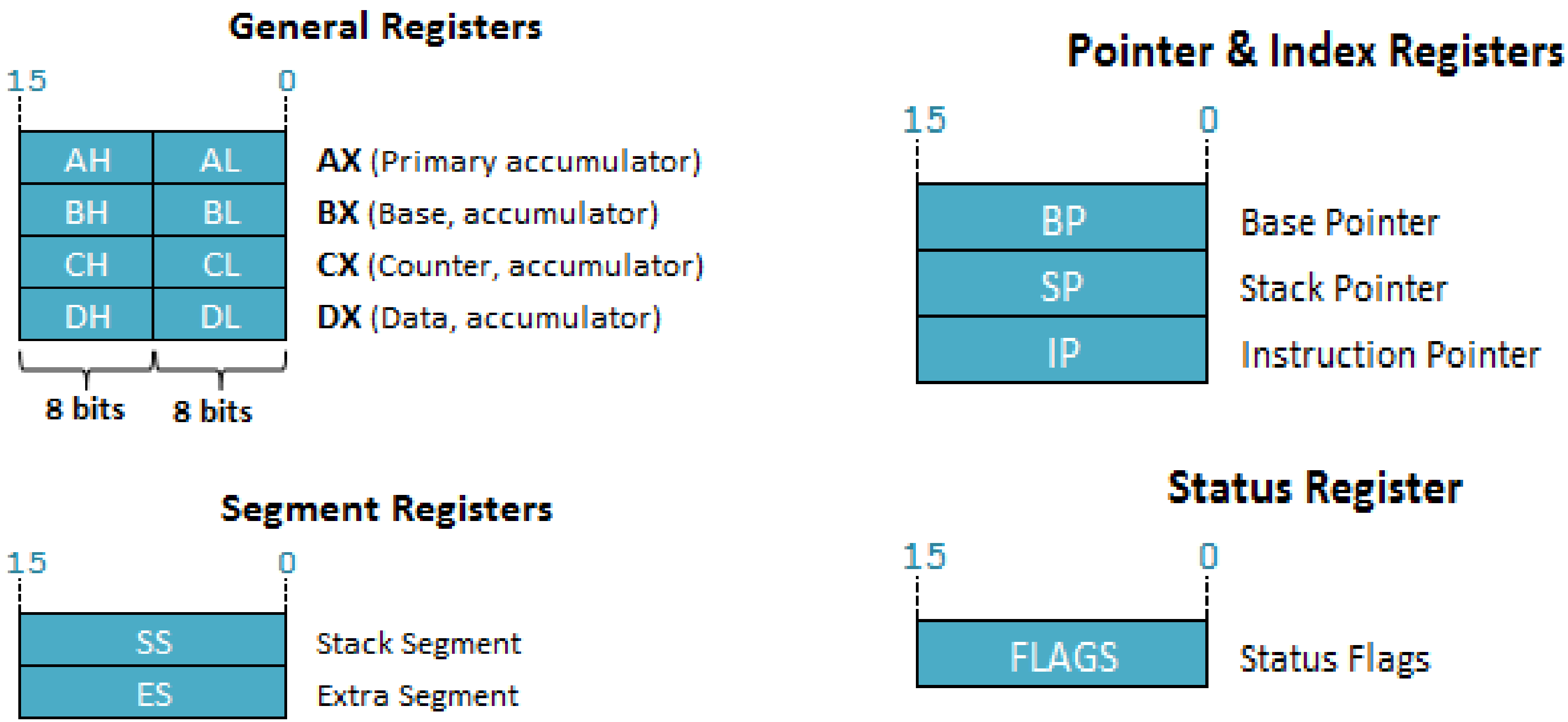
8086 Registers



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General Purpose Register

- **AX - the accumulator register (divided into AH / AL):**
  - Generates shortest machine code
  - Arithmetic, logic and data transfer
  - One number must be in AL or AX
  - Multiplication & Division
  - Input & Output
- **BX - the base address register (divided into BH / BL).**
- **CX - the count register (divided into CH / CL):**
  - Iterative code segments using the LOOP instruction
  - Repetitive operations on strings with the REP command
  - Count (in CL) of bits to shift and rotate
- **DX - the data register (divided into DH / DL):**
  - DX:AX concatenated into 32-bit register for some MUL and DIV operations
  - Specifying ports in some IN and OUT operations

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Segment Registers

- CS - points at the segment containing the current program.
- DS - generally points at segment where variables are defined.
- ES - extra segment register, it's up to a coder to define its usage.
- SS - points at the segment containing the stack.
- IP - the instruction pointer:
  - Always points to next instruction to be executed

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Pointer and Index Registers

- **SI - source index register:**
  - Can be used for pointer addressing of data
  - Used as source in some string processing instructions
- **DI - destination index register:**
  - Can be used for pointer addressing of data
  - Used as destination in some string processing instructions
- **BP - base pointer:**
  - Primarily used to access parameters passed via the stack
- **SP - stack pointer:**
  - Always points to top item on the stack
  - An empty stack will had SP = FFFEh

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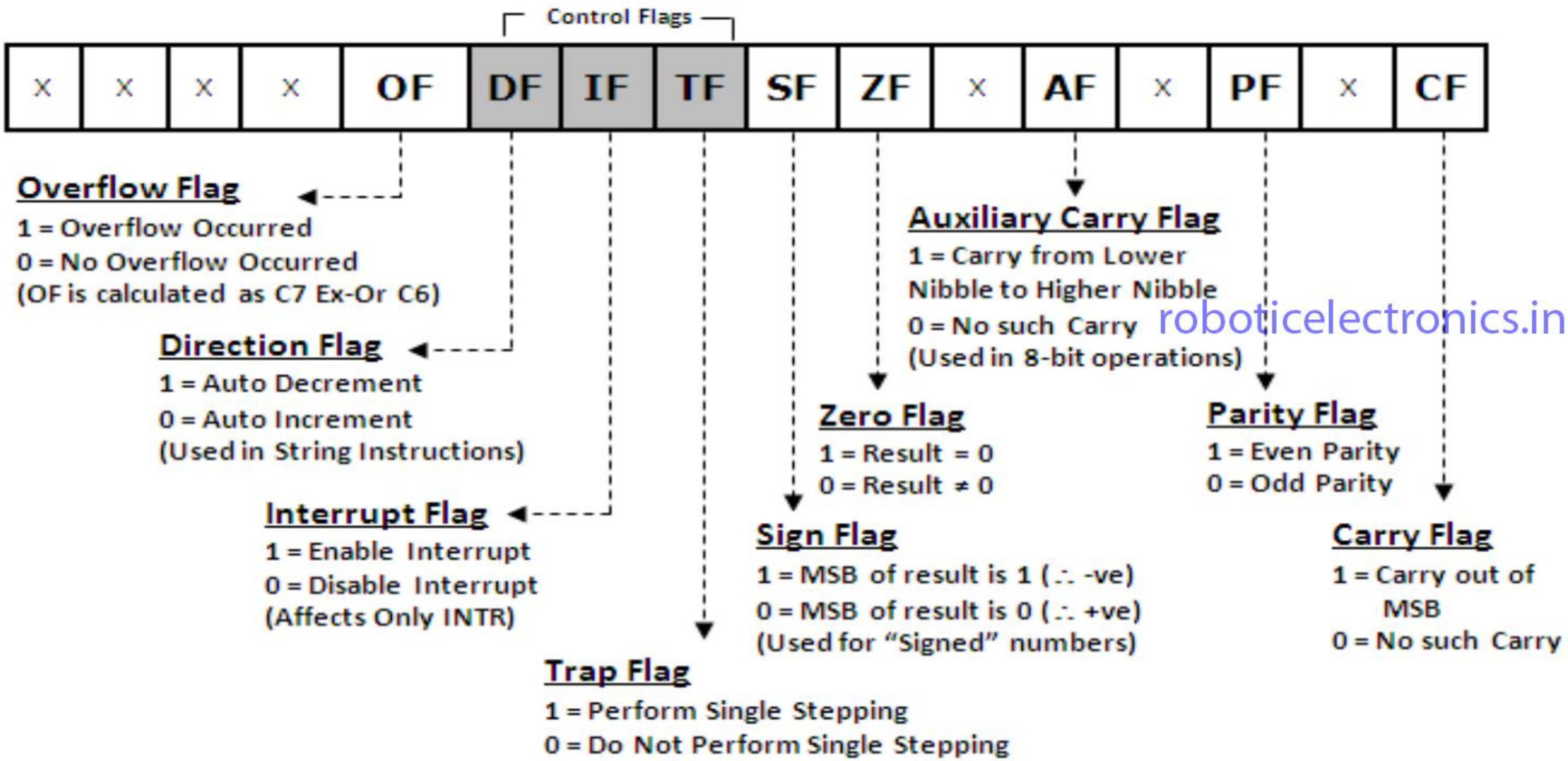
Flag Register



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8085 VS 8086

8085 Microprocessor	8086 Microprocessor
• Is an 8 Bit Microprocessor	• Is a 16 Bit Microprocessor
• Has 8 bit data bus	• Has 16 bit data bus
• Has 16 bit address line	• Has 20 bit address line
• Only 64kB of memory can be used (2^{16})	• 1MB of memory can be used (2^{20})
• Has 5 Flags (Carry, Parity, Sign, Zero, Auxillary Carry)	• Has 9 Flags (Carry, Parity, Sign, Zero, Auxillary Carry, Direction, Trap, Interrupt, Overflow)
• It is Accumulator based processor	• It is General Purpose Register Based Processor
• It has no MIN mode or MAX mode	• It can operate in any one of MIN or MAX Mode
• Does not support Pipelining	• Supports Pipelining
• Does not support Memory Segmentation	• Supports Memory Segmentation
• Has 6500 transistors	• Has 29000 transistors

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Thanks

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Welcome To Our Presentation

8085 Architecture &
Its Assembly language programming

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- Md. Mehedi Hasan (20CSE016)
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Presented To

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University of Barisal

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Outline

- Review of 8086 Architecture
  - Block diagram (Data Path)
- Similarity with x86 (i386, Pentium,)
  - Very IMP for interview/knowledge
  - Not part of Examination
- x86 Assembly language program
  - Memory model
  - Example programs
  - Data Segment
  - Loop and Nested Loop
- Next Class: Detail of assembly language
  - Summary of 8085/8086/i386 Arch & programming

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Introduction to 8086 & i386 processor

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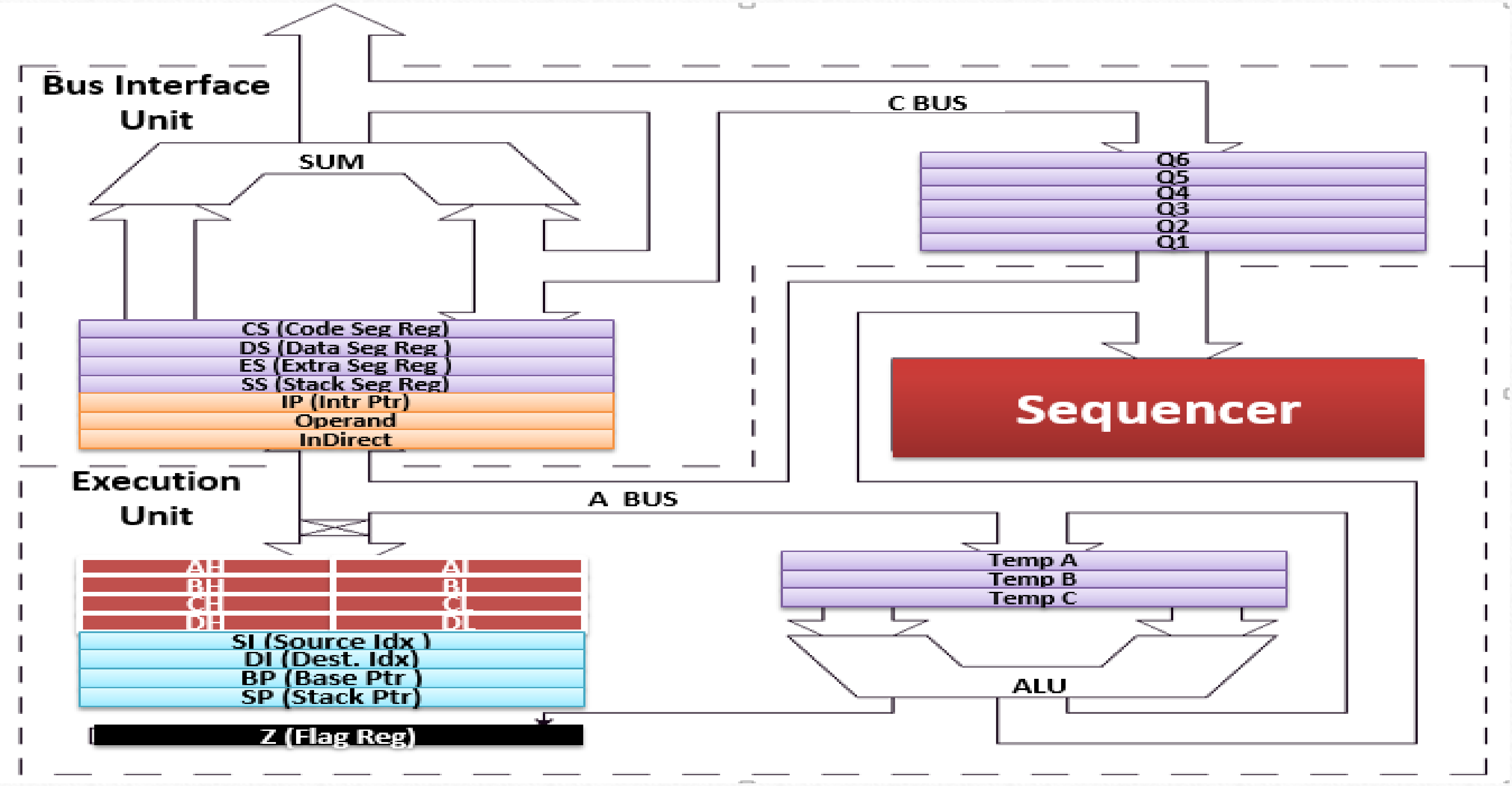
8086 Architecture



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8086 Architecture

- Execution Unit :
  - ALU may be loaded from three temp registers (TMPA, TMPB, TMPC)
  - Execute operations on bytes or 16-bit words.
  - The result stored into temp reg or registers connected to the internal data bus.
- Bus Interface Unit
  - BIU is intended to compute the addresses.
  - Two temporary registers
  - indirect addressing
  - four segment registers (DS, CS, SS and ES),
  - Program counter (IP - Instruction Pointer),
  - A 6-byte Queue Buffer to store the pre-fetched opcodes and data.
  - This Prefetch Queue optimize the bus usage.
  - To execute a jump instruction the queue has to be flushed since the pre-fetched instructions do not have to be executed.

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History of Intel Architectures

- 1978: 8086 (16 bit architecture)
- 1980: 8087
  - Floating point coprocessor is added
- 1982: 80286
  - Increases address space to 24 bits
- 1985: 80386:
  - 32 bits Add,
  - Virtual Mem & new add modes
  - Protected mode (OS support)
- 1989-95: 80486/Pentium/Pro
  - Added a few instructions of base MMX

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History of Intel Architectures

- 1997: Pentium II
  - 57 new “MMX” instructions are added,
- 1999: Pentium III:
  - Out of Order, added another 70 Streaming SIMD Ext (SSE)
- 2001: Pentium 4
  - Net burst, another 144 instructions (SSE2)
- 2003: PI4 HT, Trace Cache
- 2005: Centrino, low power
- 2007: Core architecture, Duo
- 2008: Atom, Quad core with HT….
- 2009---:Multi core (Large chip multiprocessor)

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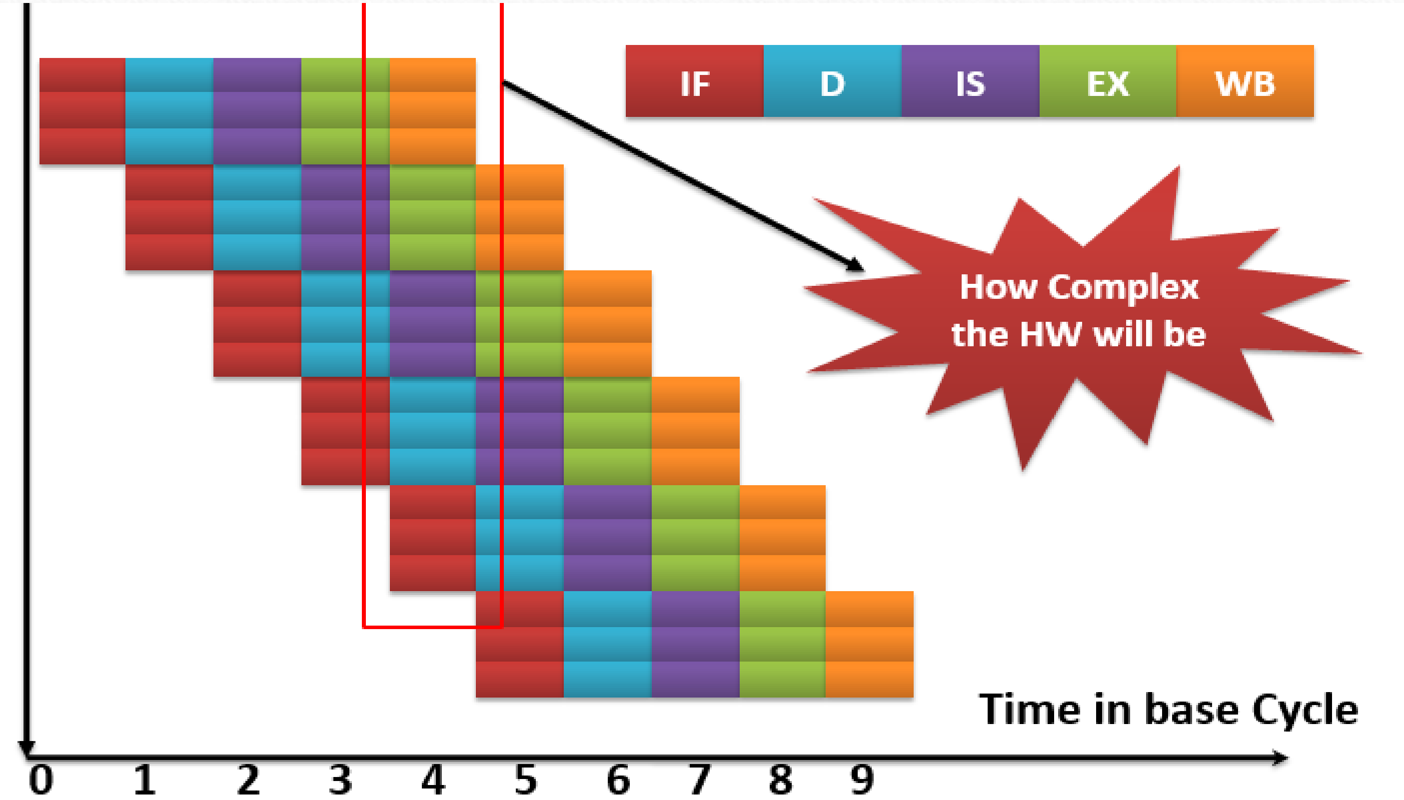
Superscalar Pipeline



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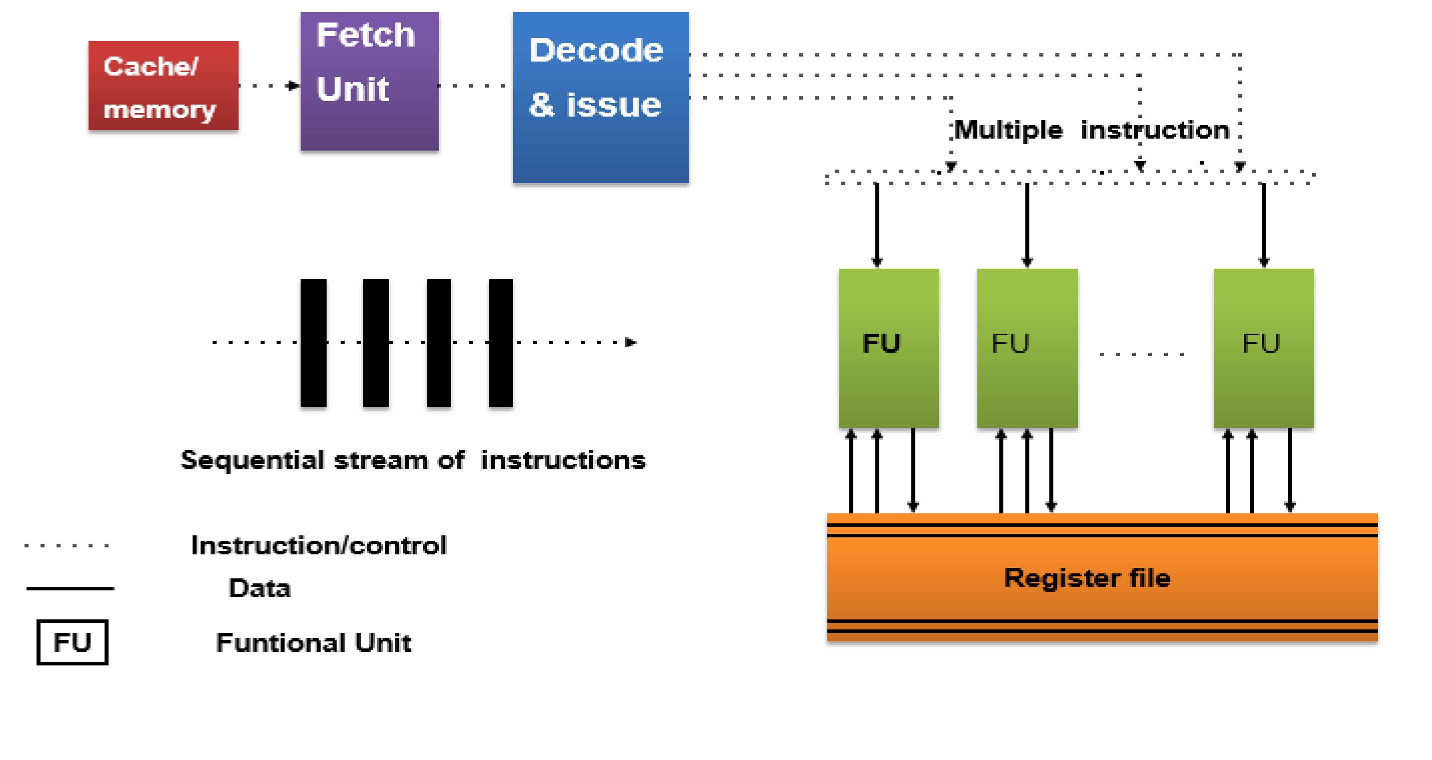
ILP in Superscalar processors



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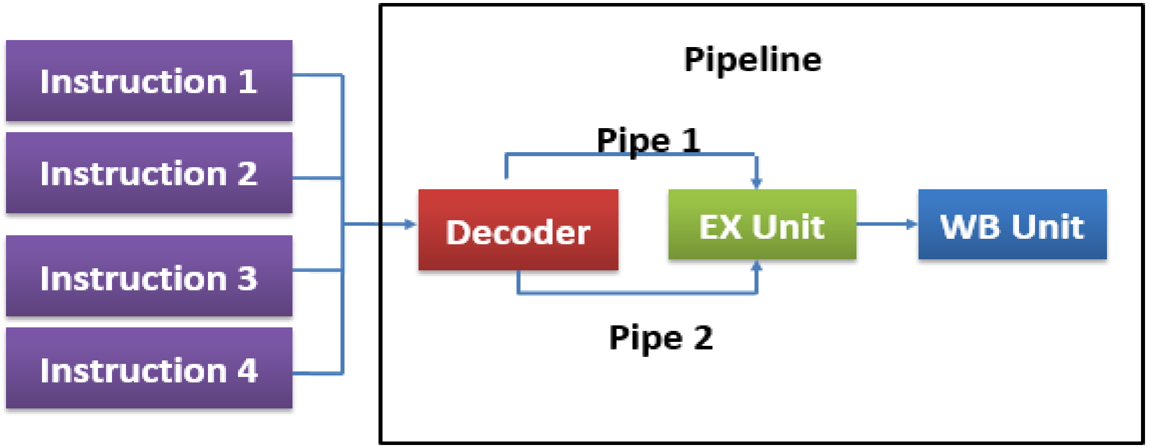
Intel P5 Architecture (Generation 5)



- Used in initial Pentium processor
- Could execute up to 2 instructions simultaneously
- Instructions sent through the pipeline in order - if the next two instructions had a dependency issue, only one instruction (pipe) would be executed and the second execution unit (pipe) went unused for that clock cycle.

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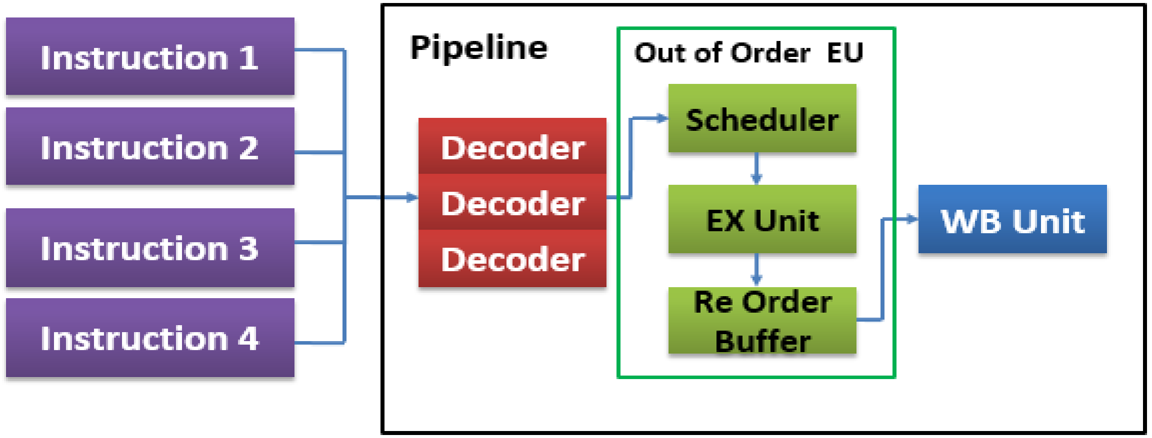
Intel P6 Architecture (Generation 6)



- Used in the Pentium II, III and Pro processors
- 3 instruction decoders, which break each CISC instruction (macro-op) into equivalent micro-operations (µops) for the Out-of-Order Execution unit
- 10 stage instruction pipeline utilized in this architecture

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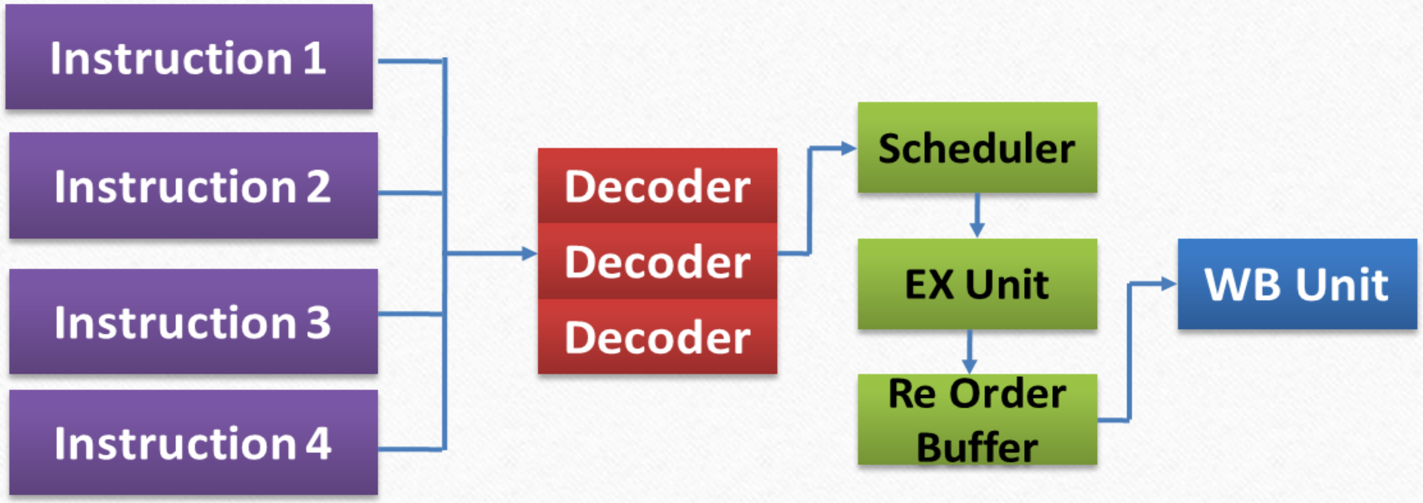
Intel NetBurst MicroArchitecture



- Used in the Pentium II, III and Pro processors.
- 3 instruction decoders, which break each instruction into equivalent micro-operations for the Execution unit .

- 10 stage instruction pipeline utilized in this architecture.

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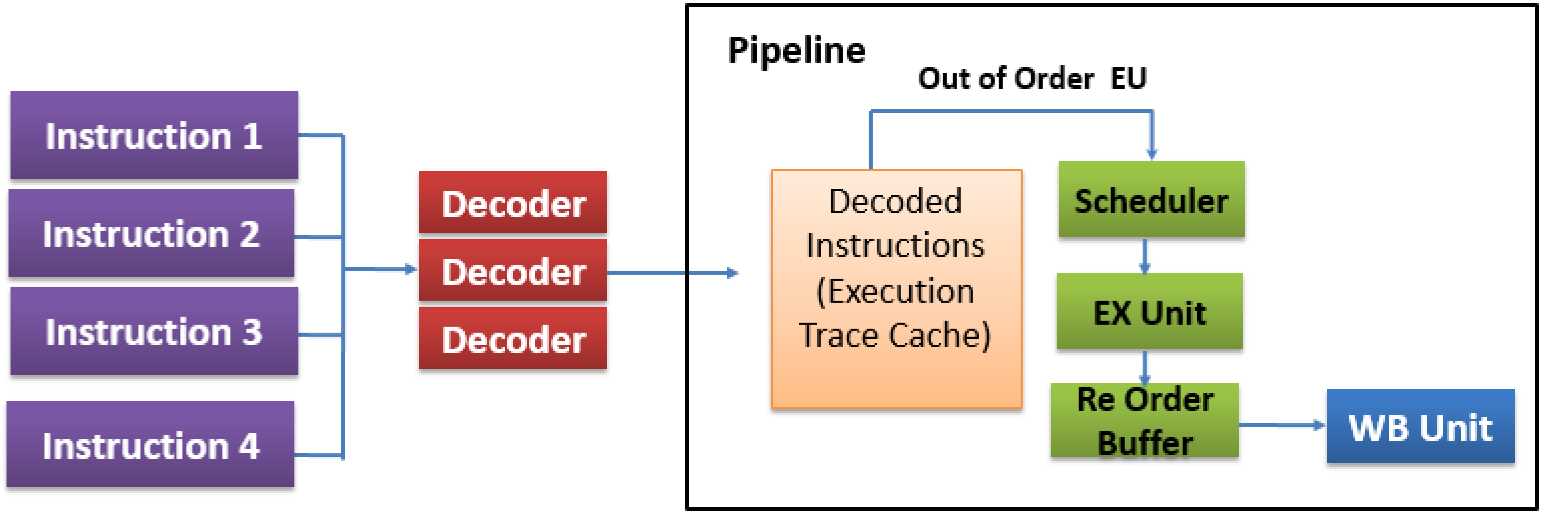
Intel NetBurst MicroArchitecture



- New architecture used for the Intel Pentium IV and Pentium Xeon processors

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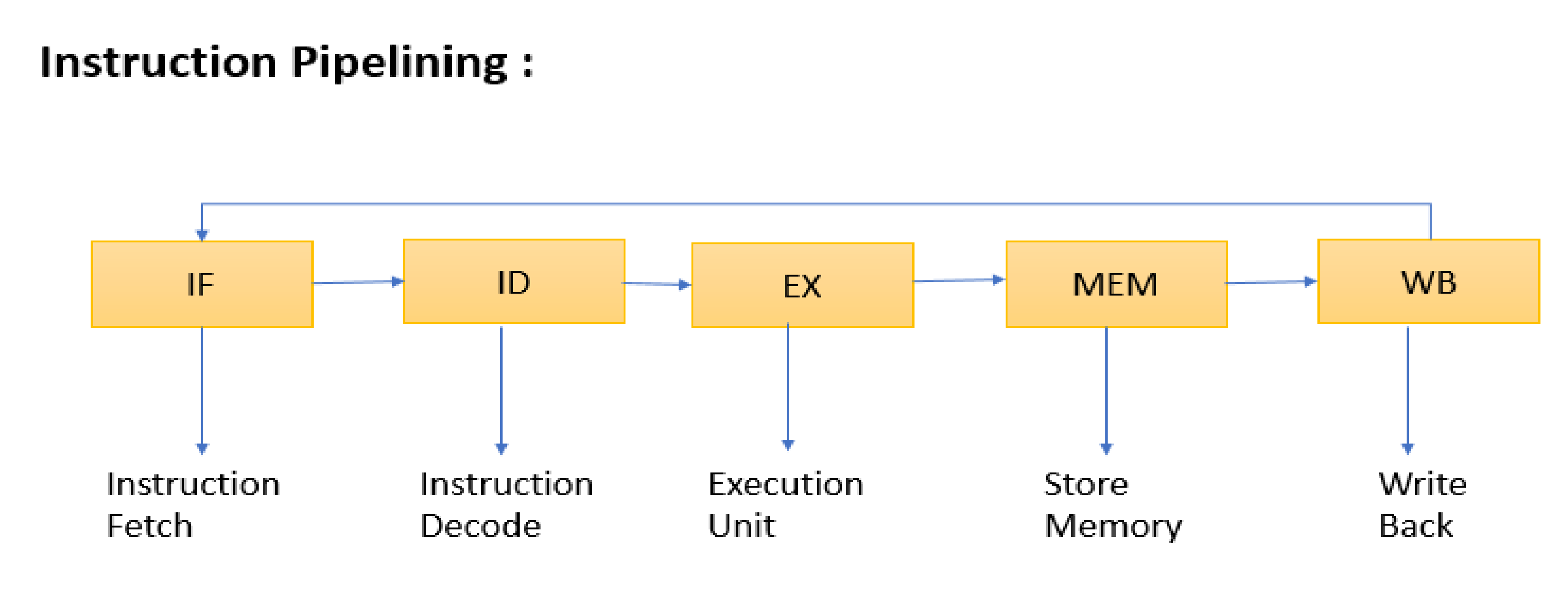
Task of SuperScalar Processing



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SuperScalar Decode & Issue

Let's explain it with an example:

IF	ID	EX	MEM	WB					
IF	ID	EX	MEM	WB					
	IF	ID	EX	MEM	WB				
	IF	ID	EX	MEM	WB				
		IF	ID	EX	MEM	WB			
		IF	ID	EX	MEM	WB			
			IF	ID	EX	MEM	WB		
			IF	**ID**	**EX**	**MEM**	**WB**		
				IF	ID	EX	MEM	WB	
				IF	ID	EX	MEM	WB	

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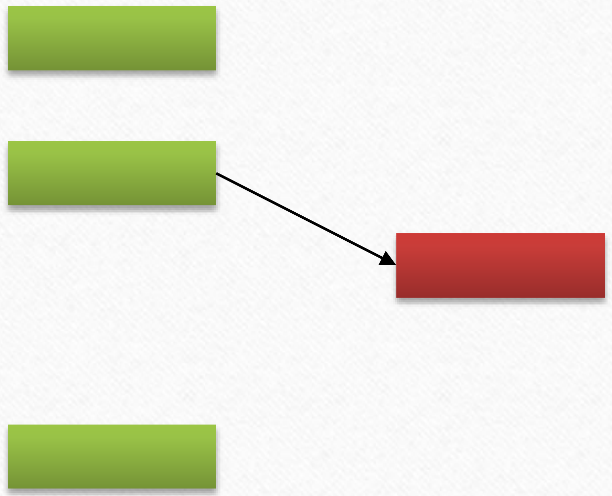
Dependent/Independent Instruction

- ADD T A B T= A+B
- ADD W C D W= C+D
- LD A, 0(W) A=M[W]
- ST C, 0(B) M[B]=C



Read After Write (RAW), W after W, W after R

RAW (Ins2-Ins3): True dependency

WAW, WAR (Ins1 ot Ins3) : false dependency

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Issue vs Dispatch

Blocking Issue

- Decode and issue to EU

Instructions may be blocked due to data dependency

Non-blocking Issue

- Decode and issue to buffer
- From buffer dispatch to EU

Instructions are not blocked due to data dependency

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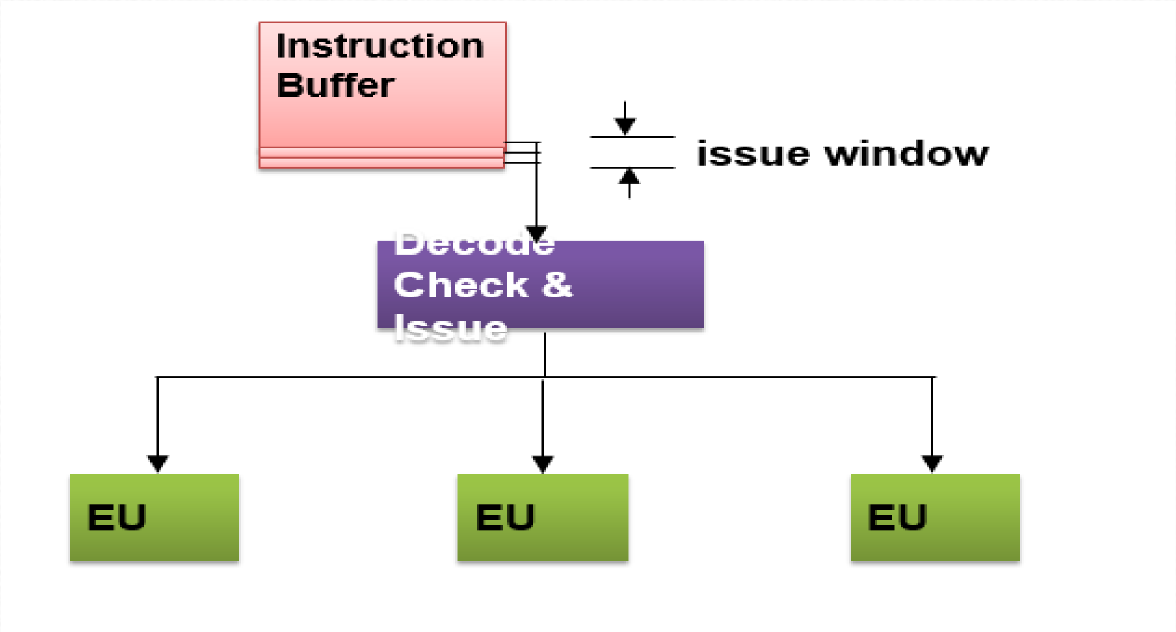
Blocking Issue



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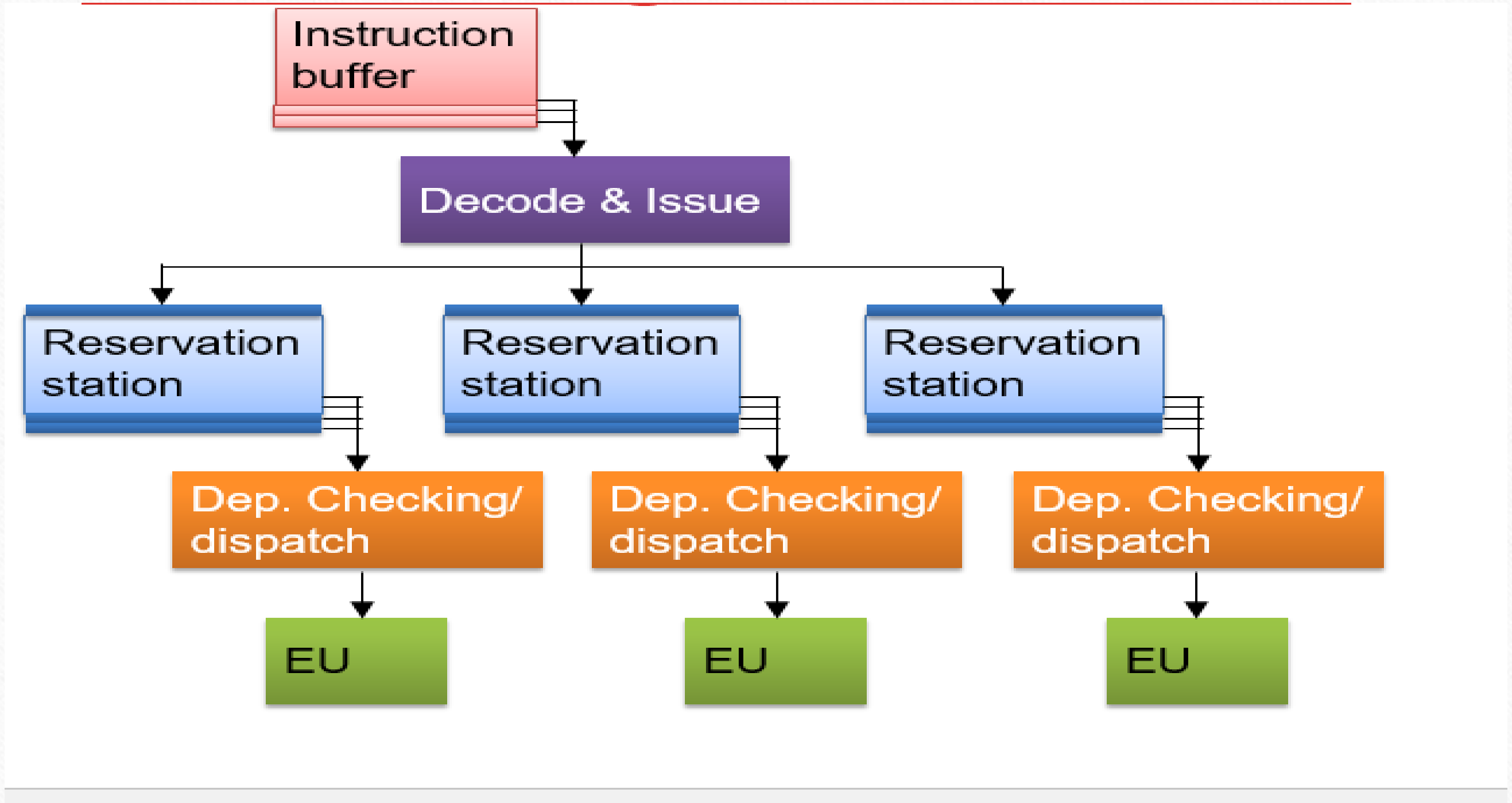
Non-blocking (shelved) Issue



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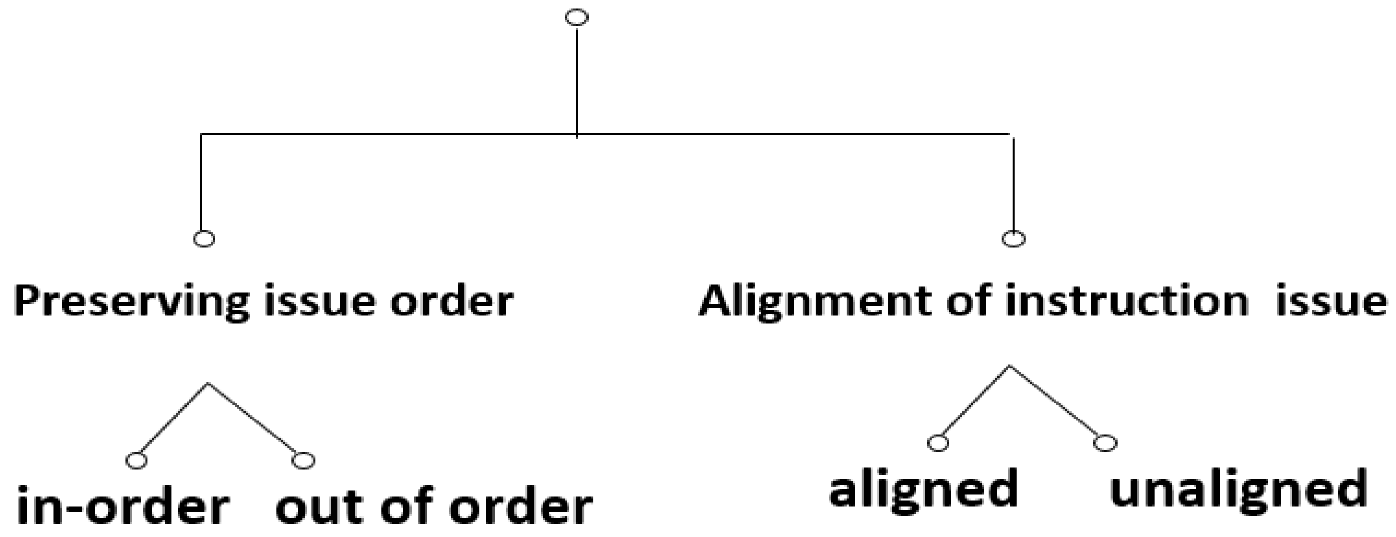
Handling of Issue Blockages



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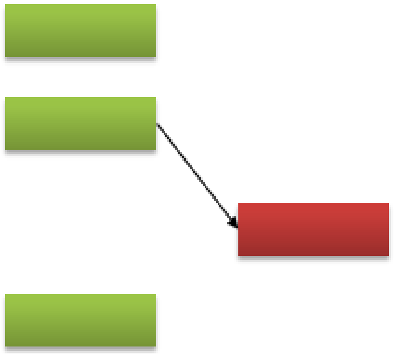
Dependent/Independent Instructions

- ADD T A B — T= A+B
- ADD W C D — W= C+D
- LD A, 0(W) — A=M[W]
- ST C, 0(B) — M[B]=C



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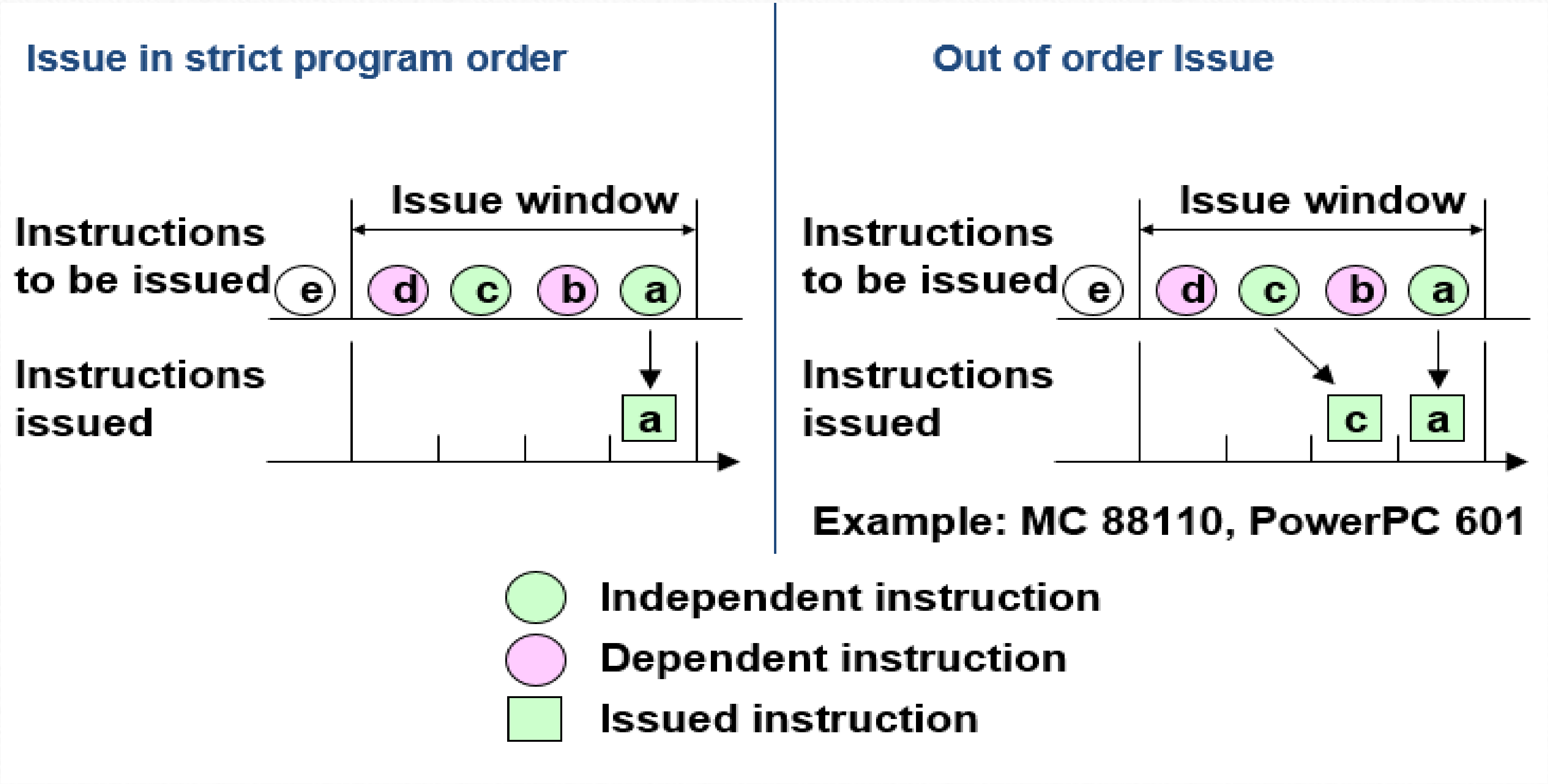
Issue Order



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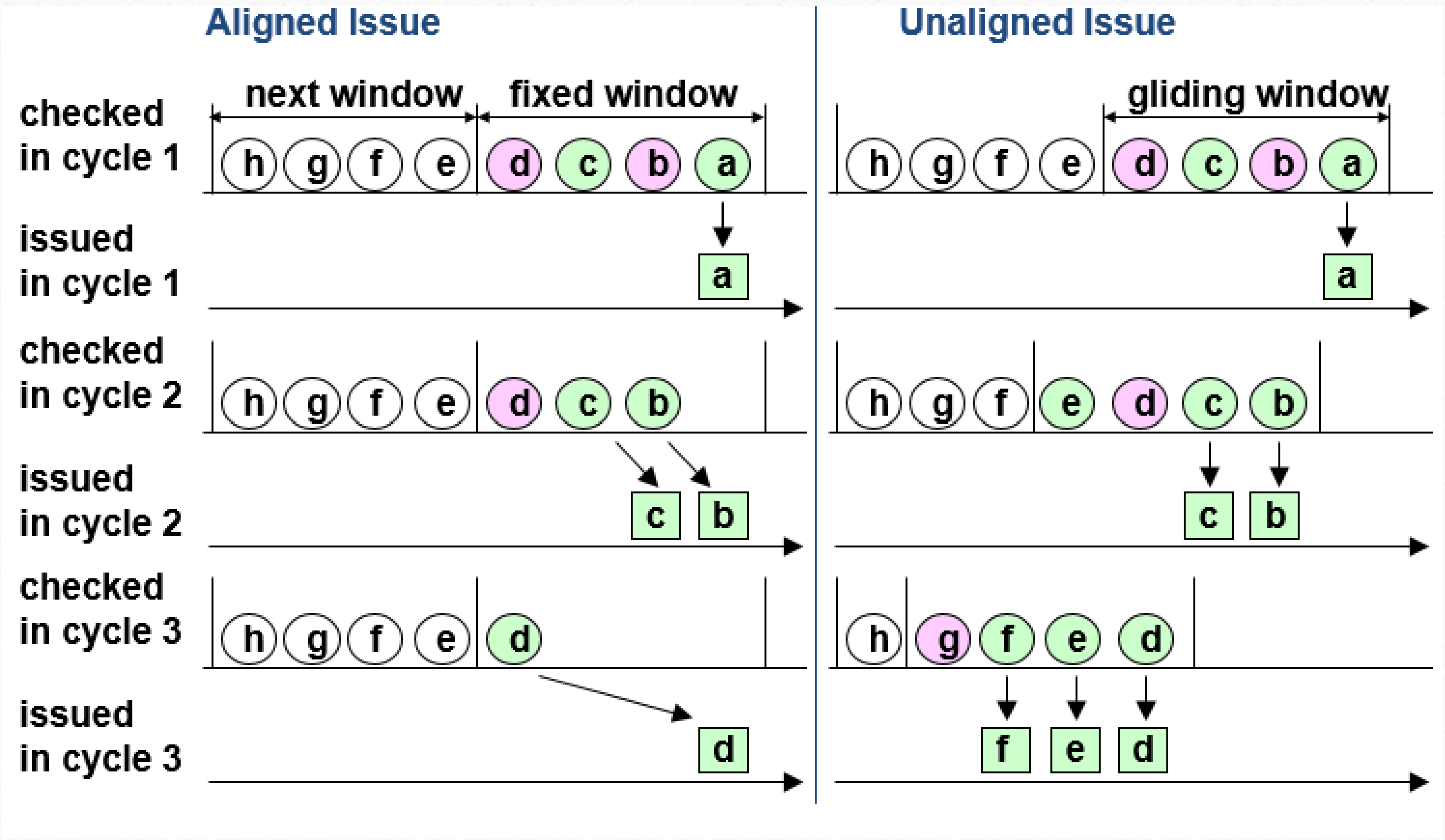
Alignment



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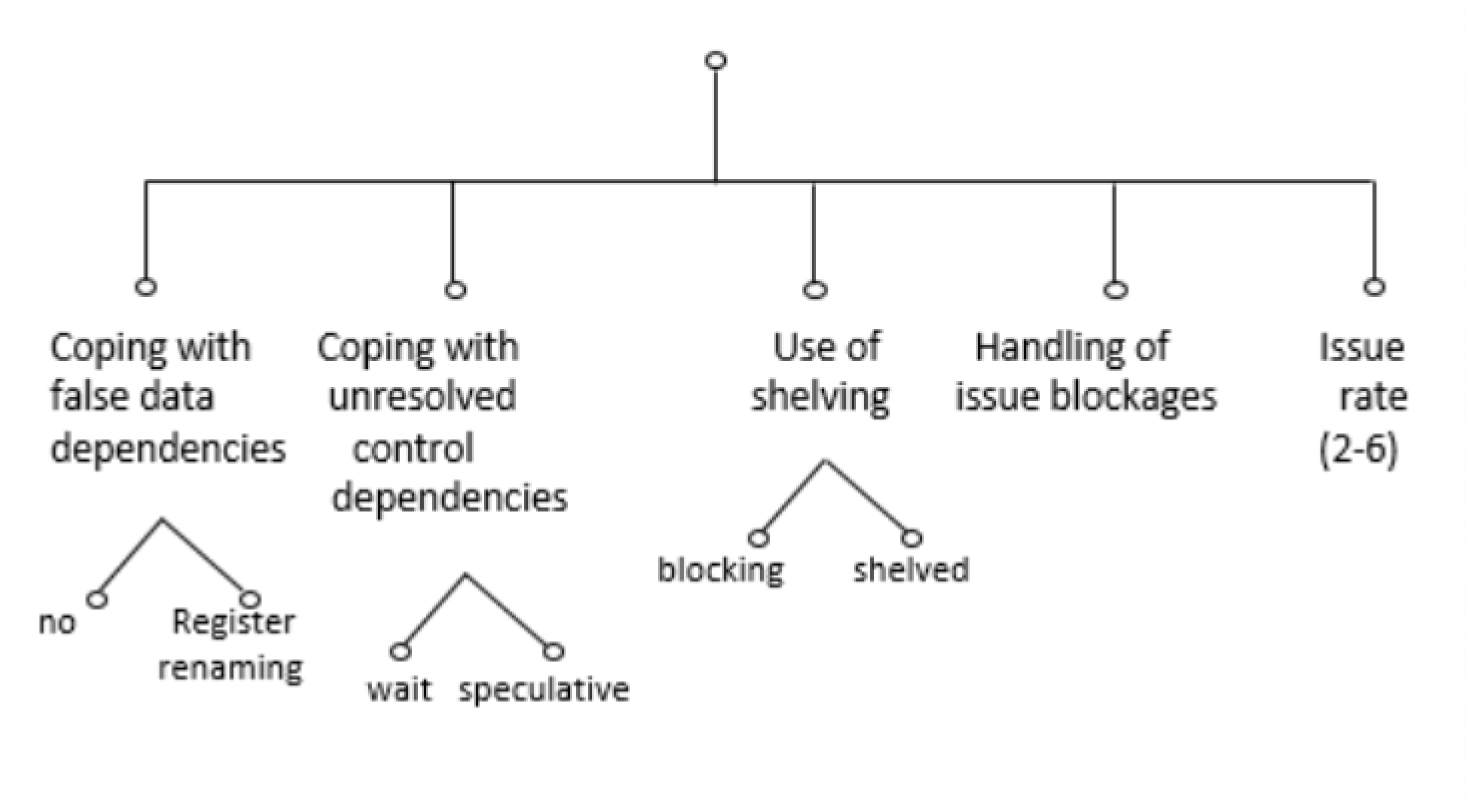
Design choices in instruction issue



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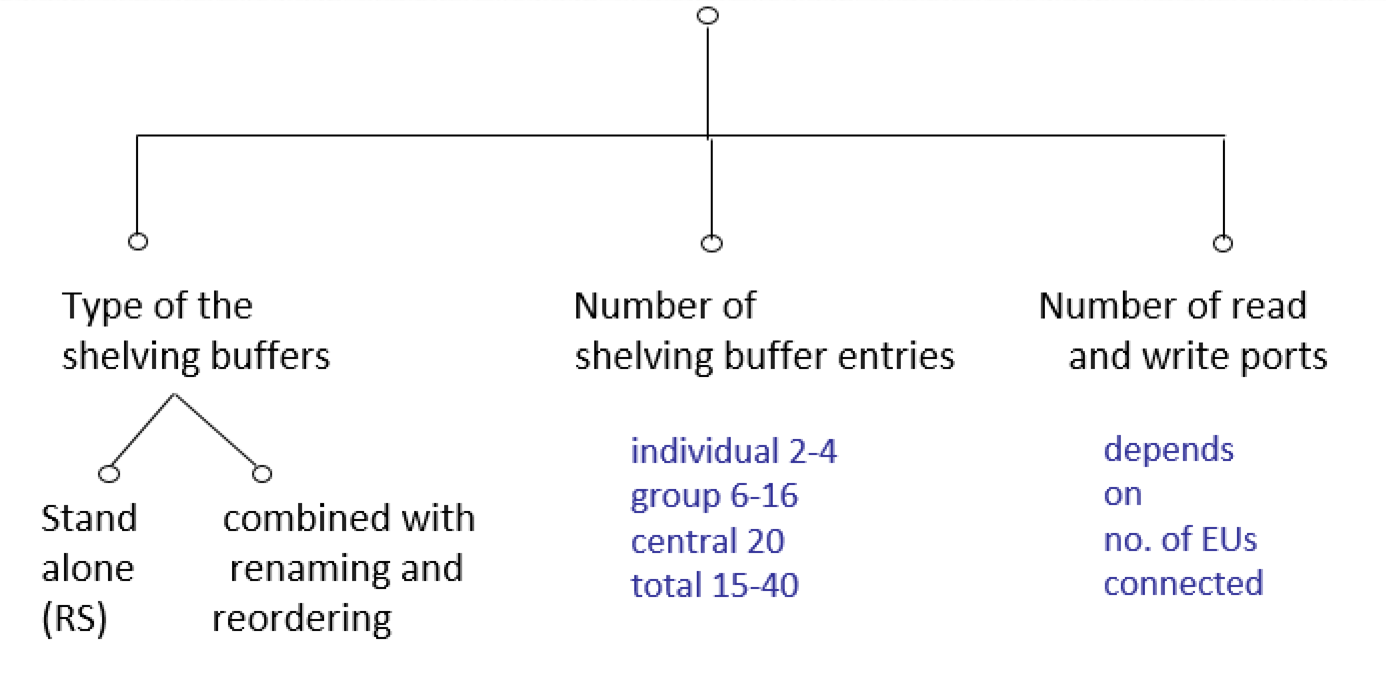
Layout of Shelving Buffers



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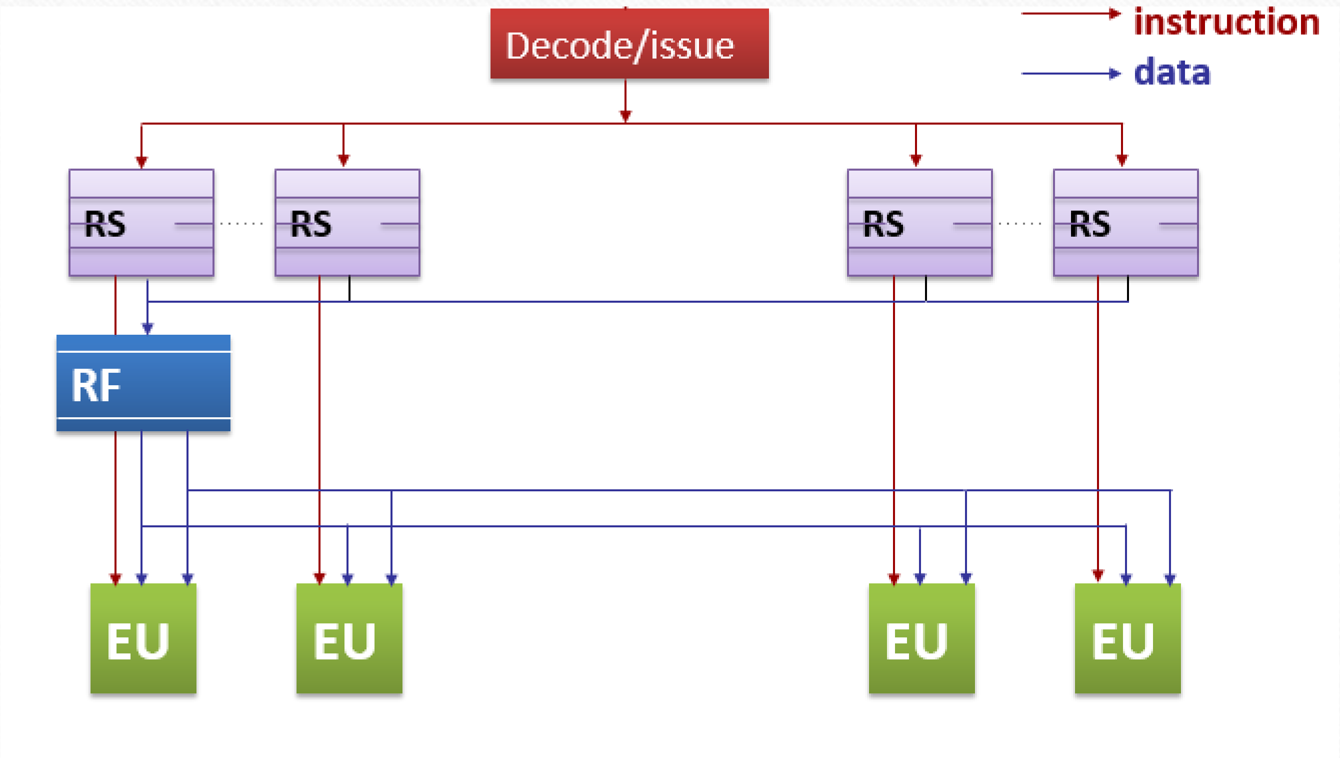
Reservation Stations (RS)



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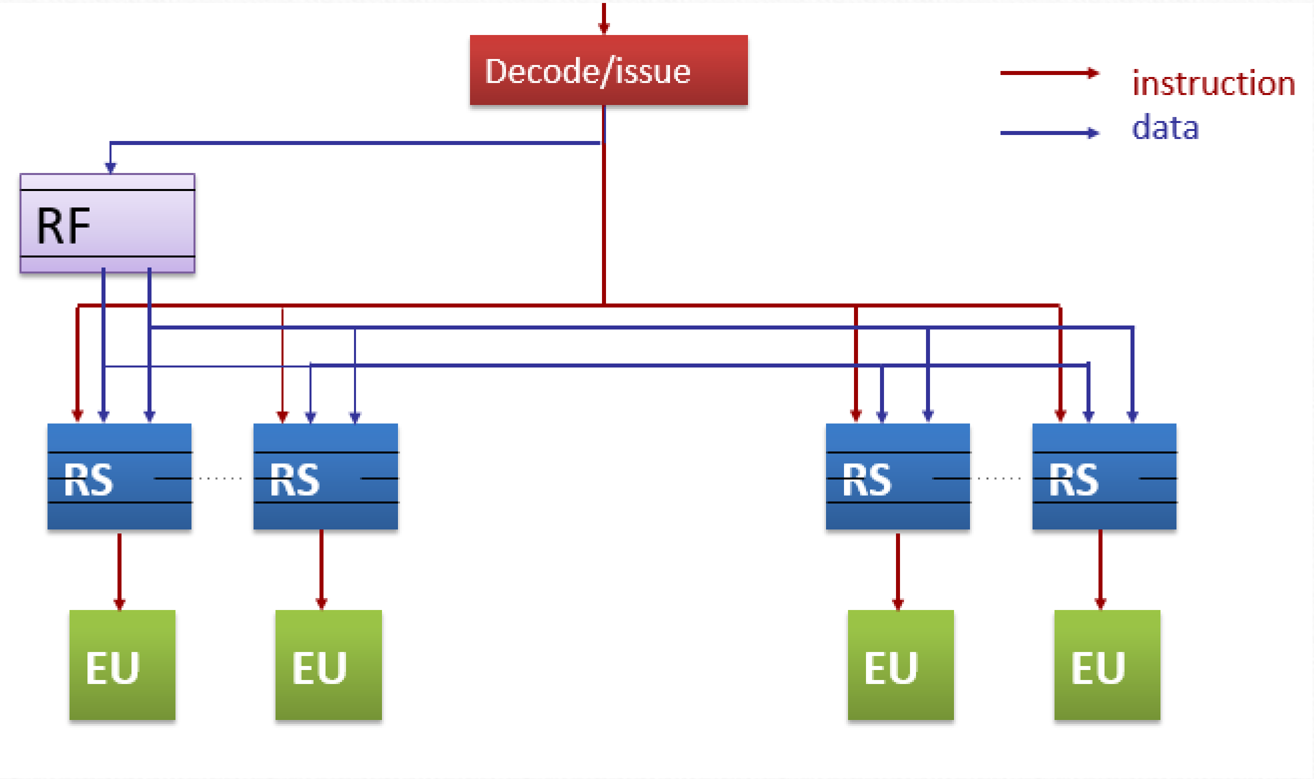
Issue bound operand fetch (with single register file)



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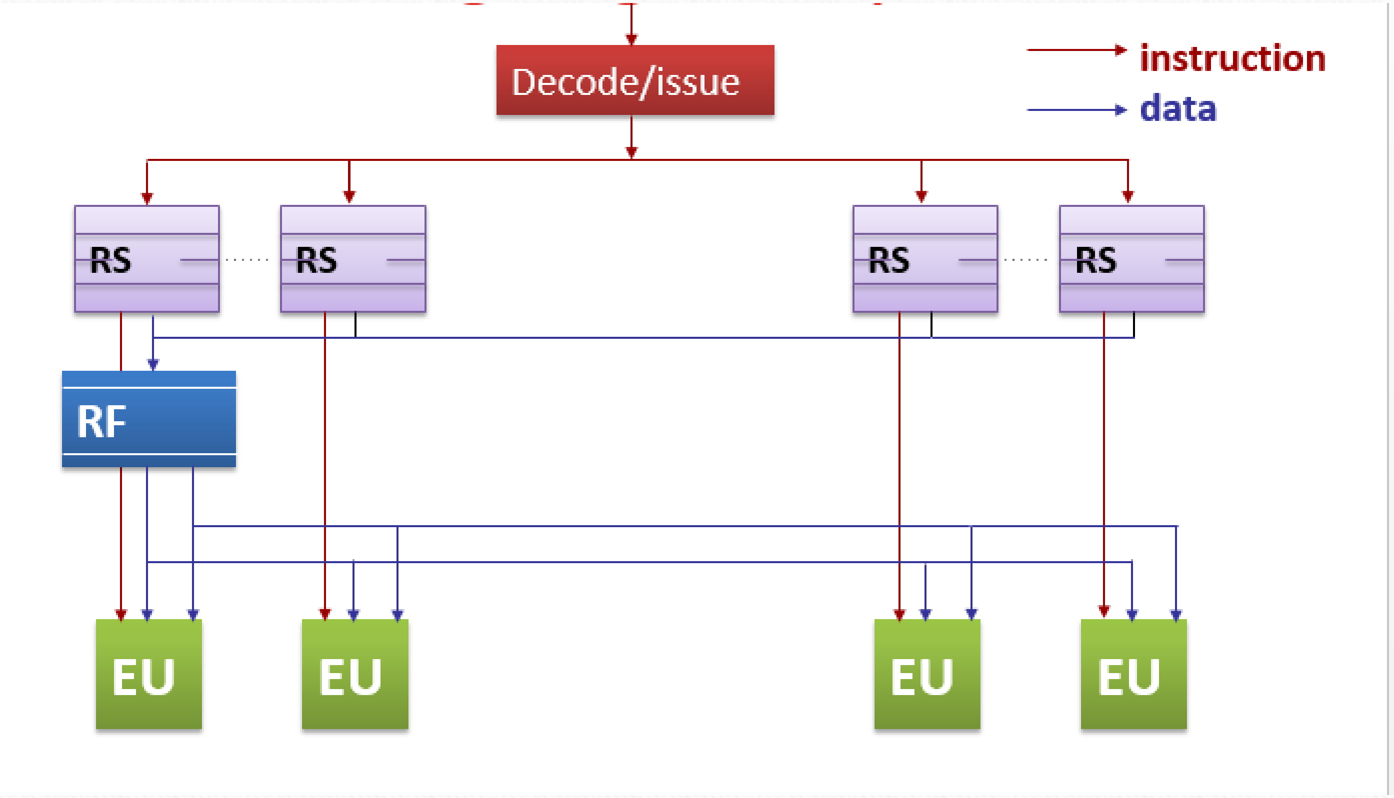
Dispatch bound operand fetch (with single register file)



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Why Renaming and Reordering?

- Register Renaming
  - Removes false dependencies (WAR and WAW)
- Reordering Buffer (ROB) : ***Pentitum Out of order instruction processing***
  - Ensures sequential consistency of interrupts (precise vs imprecise interrupts)
  - Facilitates speculative execution
    - Branch execution
    - Execute both path and discard after getting CC Value

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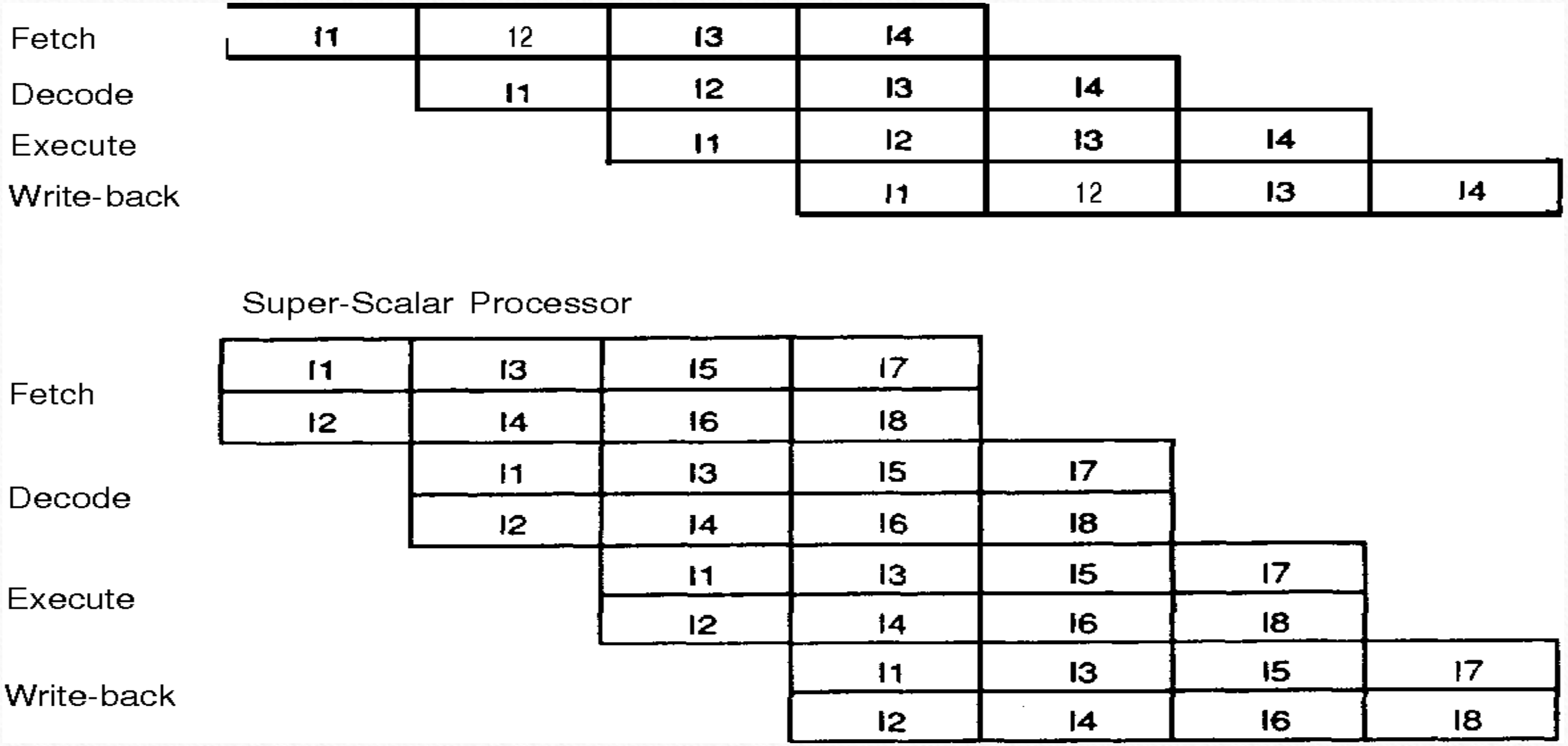
Register renaming



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Who does renaming?

- Compiler
  - Done statically
  - Limited by registers visible to compiler
- Hardware
  - Done dynamically
  - Limited by registers available to hardware

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X86 Assembly Language Program

An assembly language is a type of programming language that translates high-level languages into machine language.

X86 architecture is based on Intel's 8086 microprocessor.

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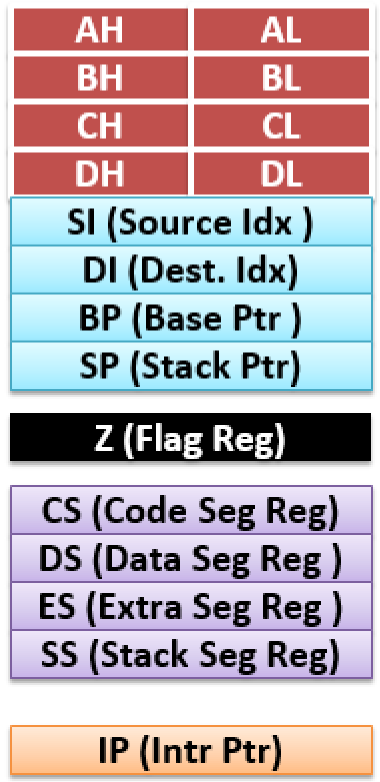
8086 Registers

AX - the accumulator register (divided into **AH** / **AL**)
BX - the base address register (divided into **BH** / **BL**)
CX - the count register (divided into **CH** / **CL**)
DX - the data register (divided into **DH** / **DL**)

SI - source index register.
DI - destination index register.
BP - base pointer.
SP - stack pointer.



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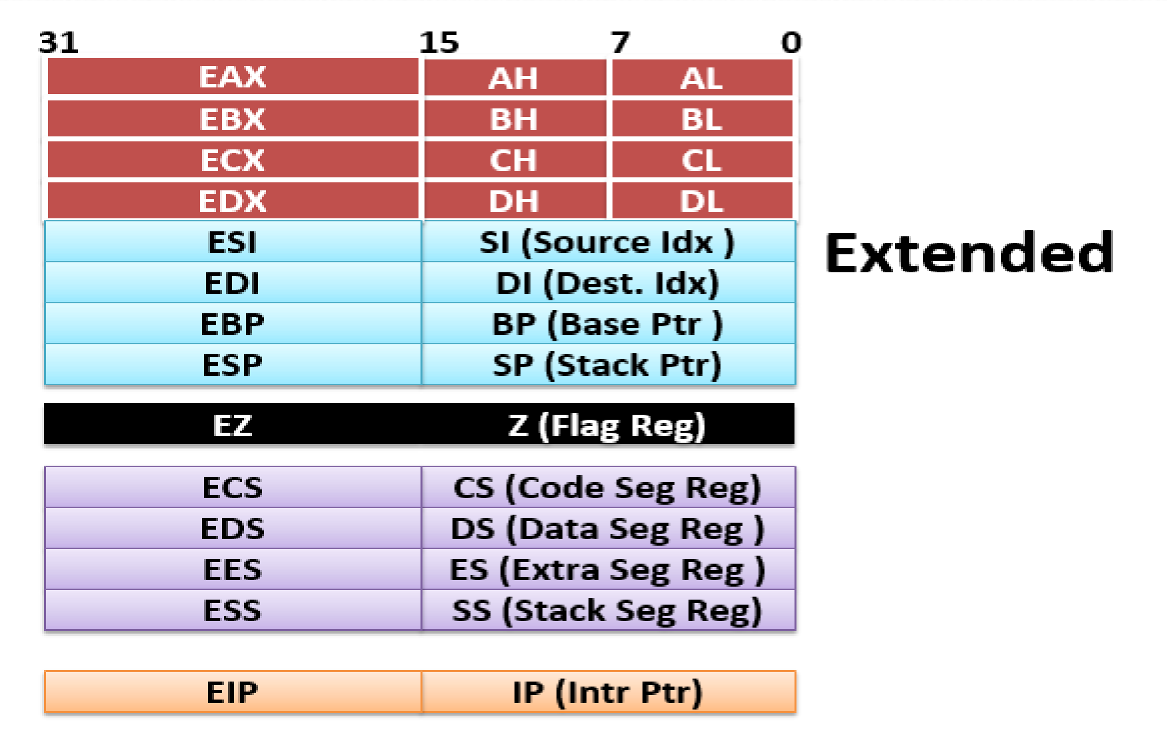
i386/i486/i686 Registers



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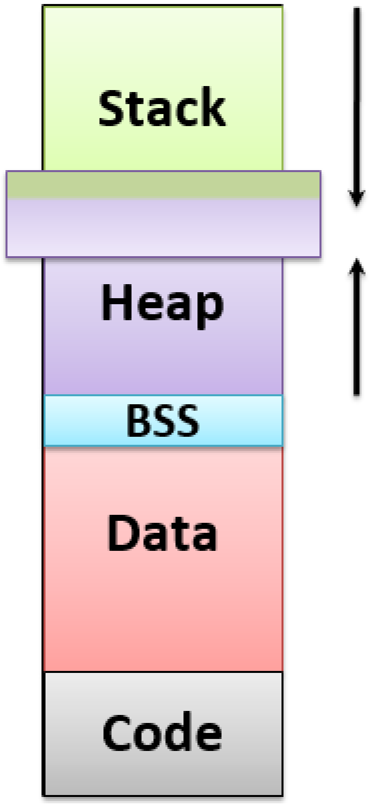
Memory layout of C program

- Stack
  - automatic (default), local
  - Initialized/uninitialized
- Data
  - Global, static, extern
  - BSS: Block Started by Symbol
  - BBS: Uninitialized Data Seg.
- Code
  - program instructions
- Heap
  - malloc, calloc



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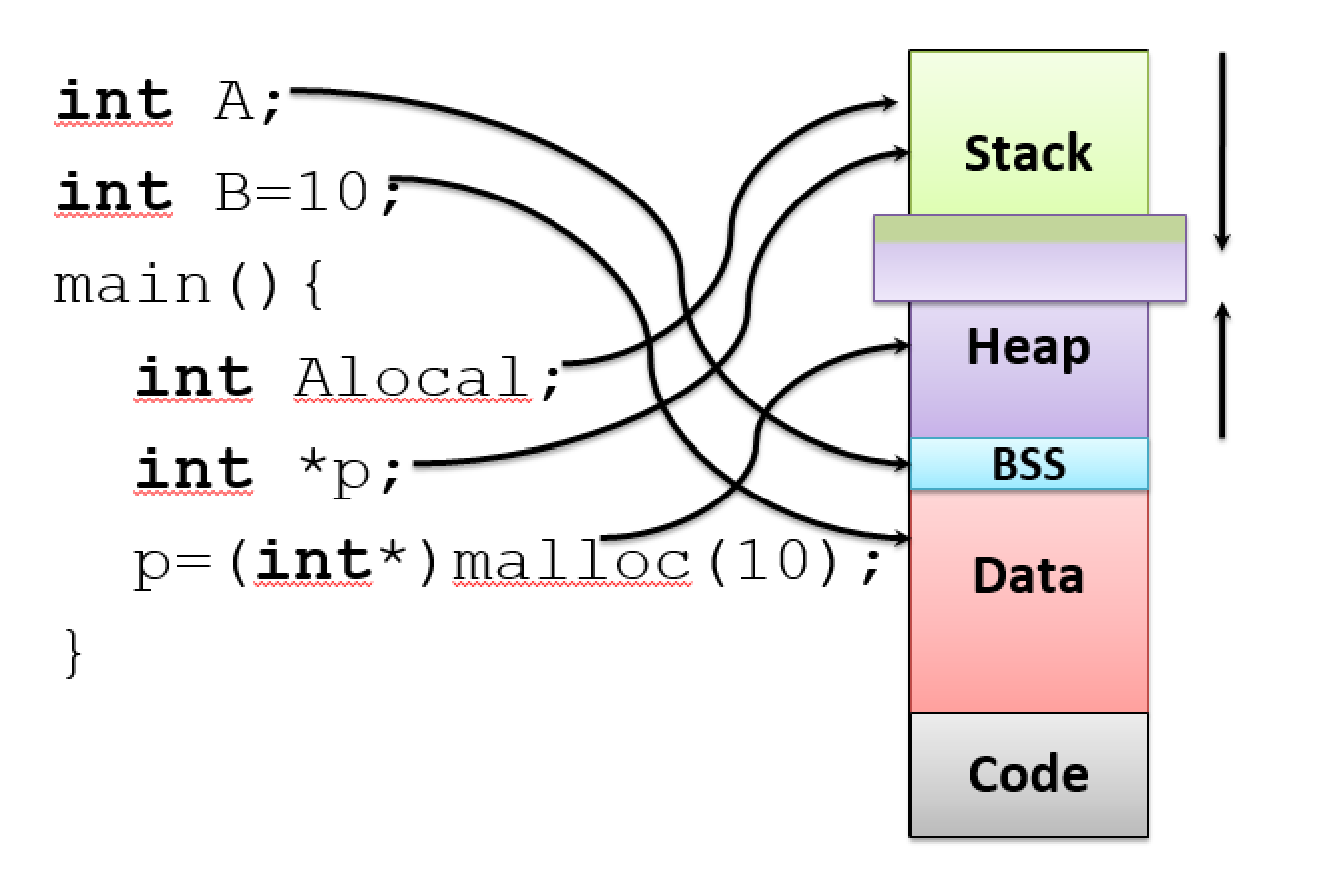
Memory layout of C program



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MASM : Hello world

model small
.stack 100h ; reserve 256 bytes of stack space
.data
message db "Hello world, I'm learning Assembly$"
.code
main proc
mov ax, seg message
mov ds, ax
mov ah, 09 // 9 in the AH reg indicates Procedure
//should write a bit-string to the screen.
lea dx, message // Load Eff Address
int 21h
mov ax,4c00h // Halt for DOS routine (Exit Program)
int 21h
main endp
end main

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Memory Model: Segment Definition

- .model small
  - Most widely used memory model.
  - The code must fit in 64k.
  - The data must fit in 64k.
- .model medium
  - The code can exceed 64k.
  - The data must fit in 64k.
- .model compact
  - The code must fit in 64k.
  - The data can exceed 64k.
- .medium and .compact are opposites.

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Data Allocation Directives

- db : define byte dw: def. word (2 bytes)
- dd: def double word (4) dq : def quad word (8)
- equ : equate assign numeric expr to a name

.data

db A 100 dup (?) ; define 100 bytes, with no initial values for bytes

db "Hello" ; define 5 bytes, ASCII equivalent of "Hello".

dd PtrArray 4 dup (?) ;array[0..3] of dword

maxint equ 32767 ; define maxint=32767

count equ 10 * 20 ; calculate a value (200)

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MASM: Loop

- Assembly code: Loop
  - Loop simply decreases CX and checks if CX != 0, if so, a Jump to the specified memory location

```
MOV CX,100
   _LABEL:      INC AX
                LOOP    _LABEL
```

  - LOOPNZ : LOOPs when the zero flag is not set

```
MOV CX,10
_CMPLOOP:DEC AX
         CMP AX,3
         LOOPNE CMPLOOP
```

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MASM: Nested Loop

- Assembly code: Nested Loop: One CX register

```
 mov     cx, 8
Loop1: push    cx
           mov     cx, 4
Loop2:  stmts
           loop    Loop2
           pop     cx
           stmts
           loop    Loop1
```

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