Interfacing DAC/ADC *without Peripheral Controller*

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Outline

- Peripheral communications
- DAC
  - Properties
  - Generic Model
  - Interfacing
- ADC
  - Properties
  - Generic Model
  - Interfacing
- Display

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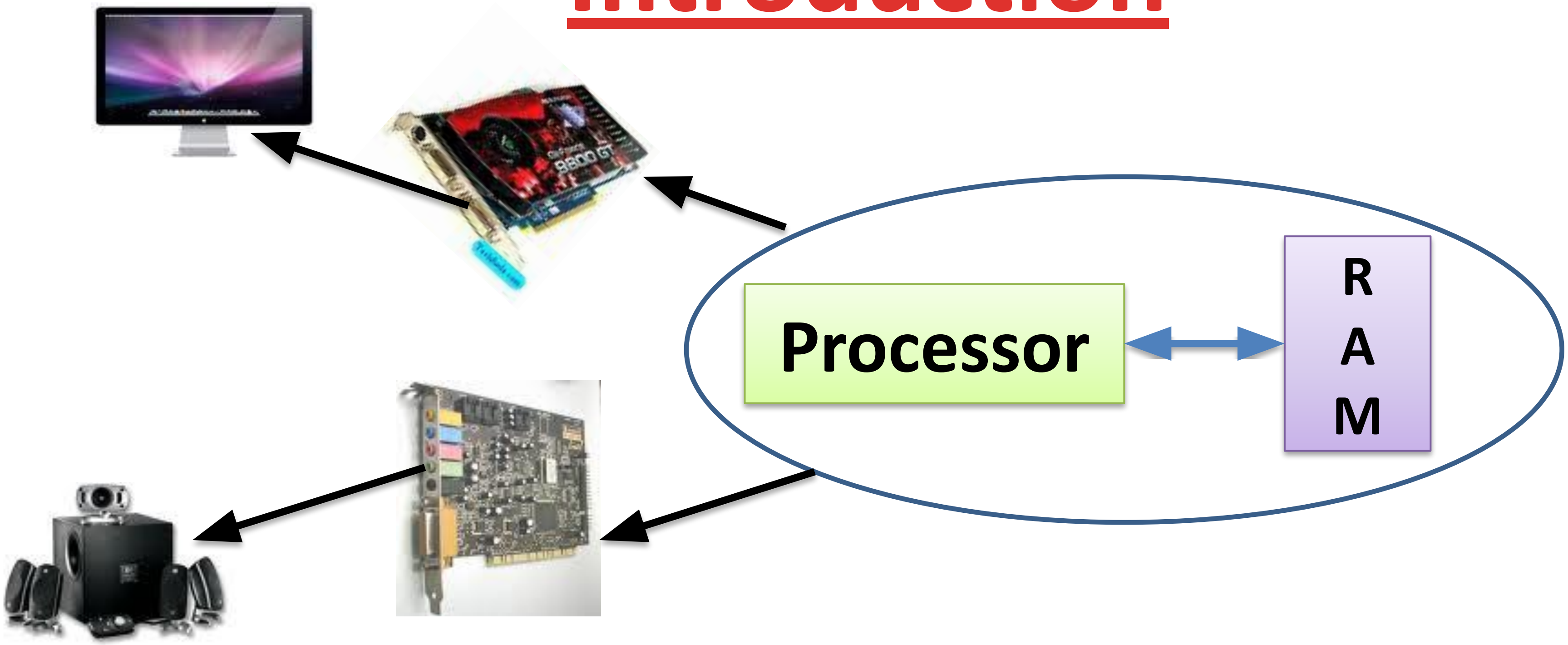
Introduction



- Peripherals : HD monitor, 5.1 speaker
- Interfaces : Intermediate Hardware
  - Nvidia GPU card, Creative Sound Blaster card
- Interfaces : Intermediate Software/Program
  - Nvidia GPU driver , Sound Blaster Driver software

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Primary function of MPU

- Read Instruction from memory
- Execute instruction
- Read/Write data to memory
- Some time send result to output device
  - LEDs, Monitor, Printer
- Interfacing a peripheral
  - Why: To enable MPU to communicate with I/O
  - Designing logic circuit H/W for a I/O
  - Writing instruction (S/W)

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Transmission controller

- Transmission Controller:
  - MPU control, Device Control (DMA)
- Type of IO mapping
  - Peripheral (IN/Out), Memory mapped IO (LD/ST,MV)
- Format of communication
  - Synchronous (T & R sync with clock), Asynchronous
- Mode of Data Transfer
  - Parallel, Serial (UART)
- Condition for data transfer
  - Uncond., Polling, Interrupt, Ready signal, Handshake

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Digital to Analog Converter

- Used for play sound in speaker
- Used by AC97 (Audio codec)
- MP3 Sound store digital format in HDD
- Slow as compared to processor/MPU
- Parameters
  - Resolution (8 bit/16 bit)
  - Settling time (1micro sec)

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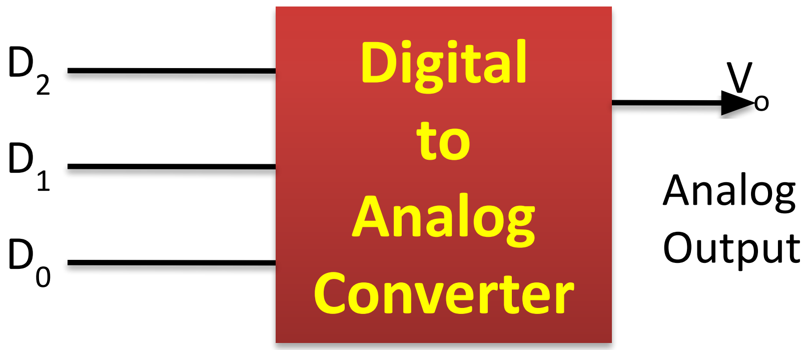
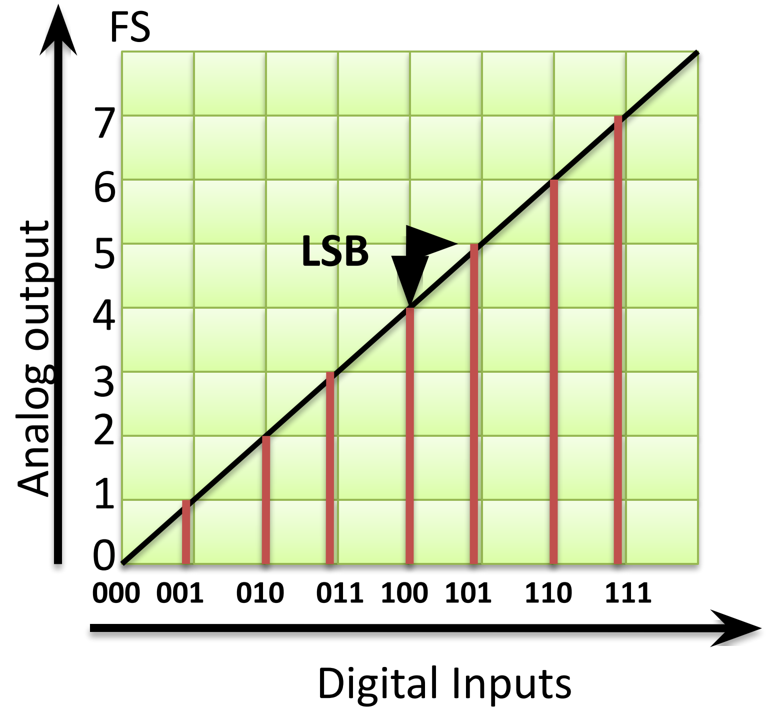
D/A converter





- FullScaleOutput=(FullScaleValue – 1LSBValue)
- 1MSB Value=1/2 * FSV

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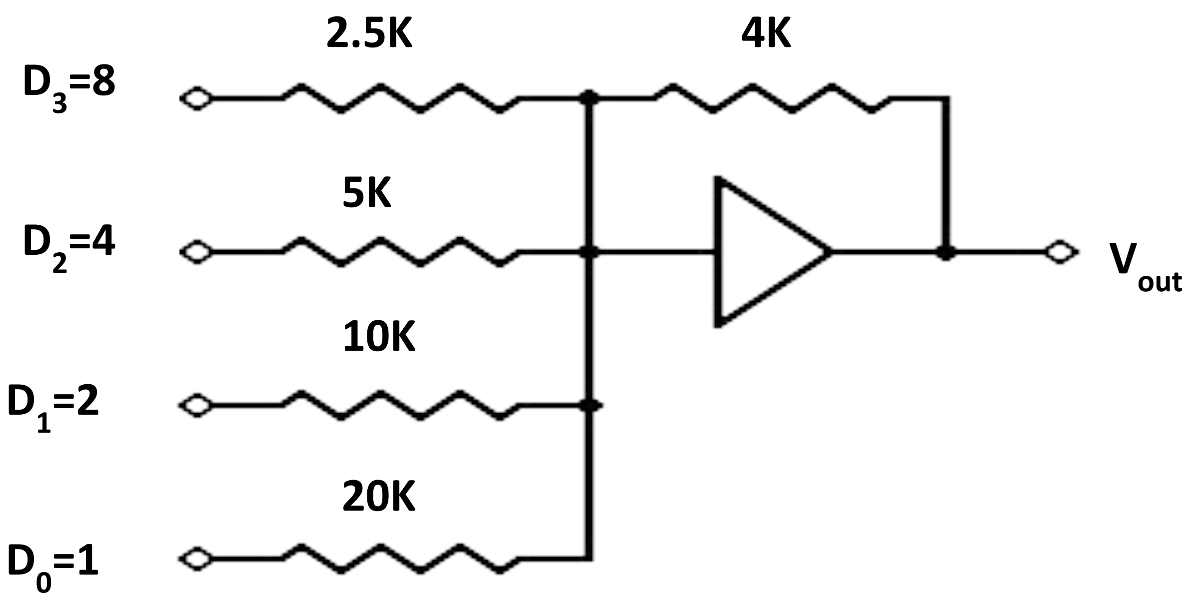
Circuit Realization



- $Vo = Vref/R * (A_1/2 + A_2/4 + \ldots A_n/2^n)$
- Vo is proportional to values of Data Bits Value

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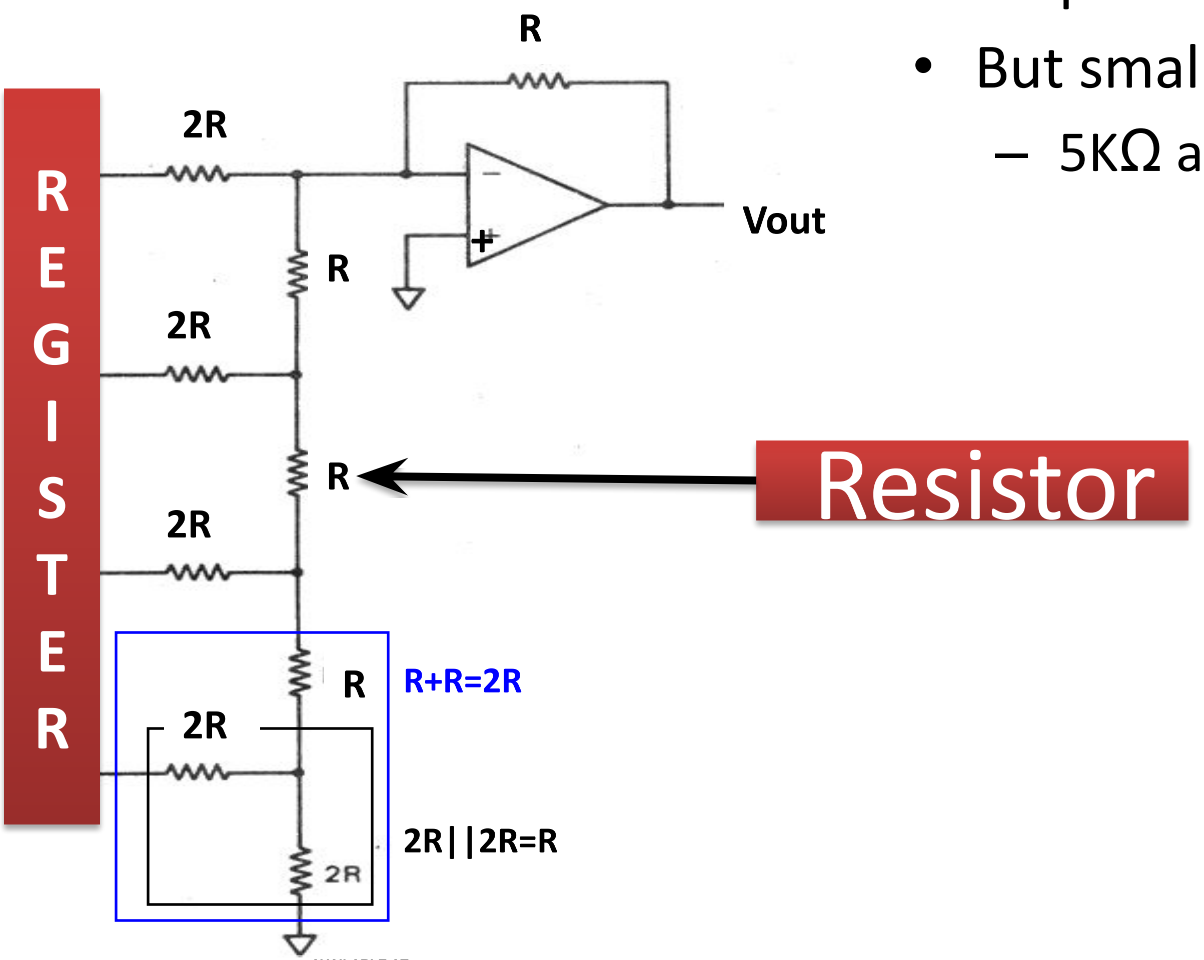
Practical DAC : R-2R ladder network

- Resistive Ladder Network



- Require two type Resistor
- But small value
  - 5KΩ and 10KΩ

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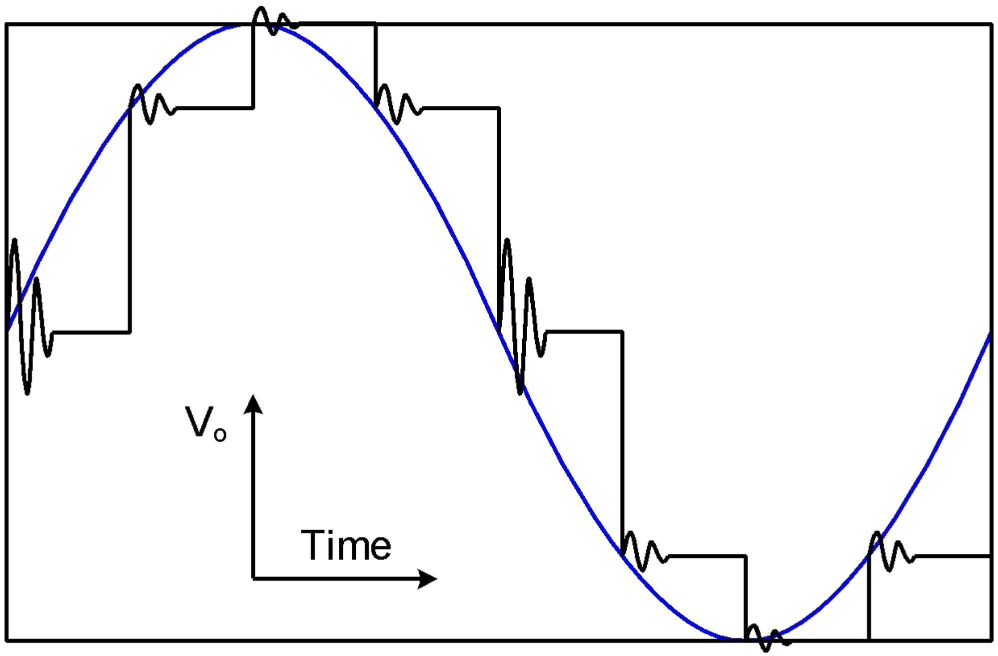
Output Glitches



- Cause: Signal and clock skew in circuits
- Especially severe at MSB transition where all bits are switching –

  0111…111 →

  1000…000

- Glitches cause waveform distortion, spurs and elevated noise floors
- High-speed DAC output is often followed by a de-glitching SHA (Hold Buffer)

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Performance of DAC

- Resolution
- Reference Voltages
- Settling Time
- Linearity
- Speed
- Errors

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Resolution

- Amount of variance in output voltage for every change of the LSB in the digital input.
- How closely can we approximate the desired output signal(Higher Res. = finer detail=smaller Voltage divisions)
- A common DAC has a 8 - 12 bit Resolution

$$\text{Resolution} = V_{LSB} = \frac{V_{\text{Ref}}}{2^N}$$

N = Number of bits

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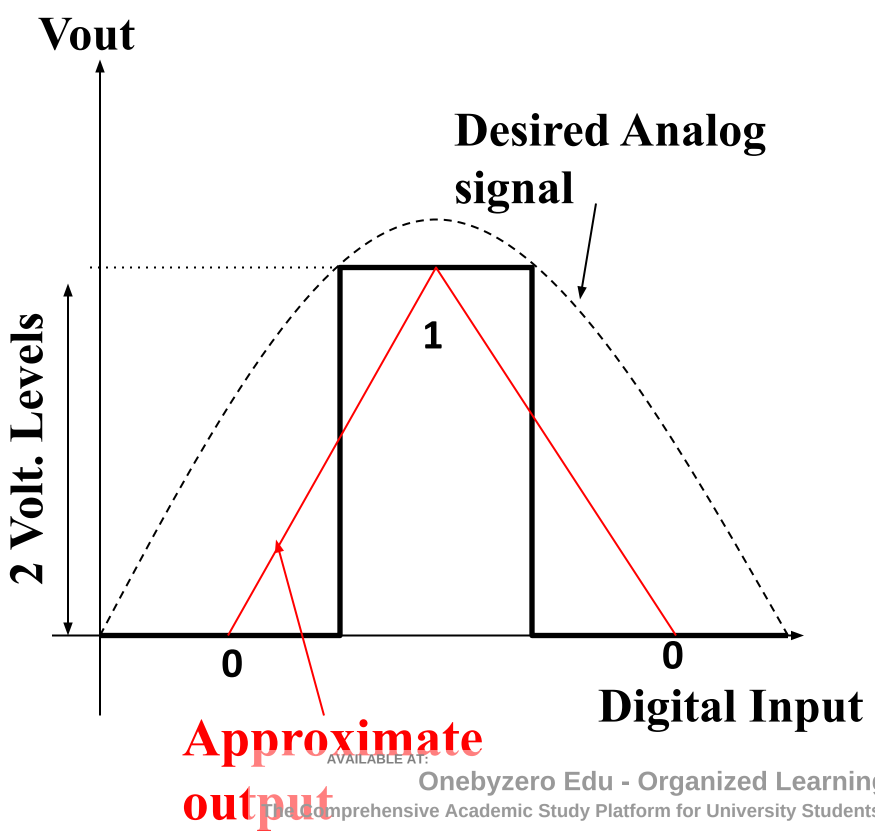
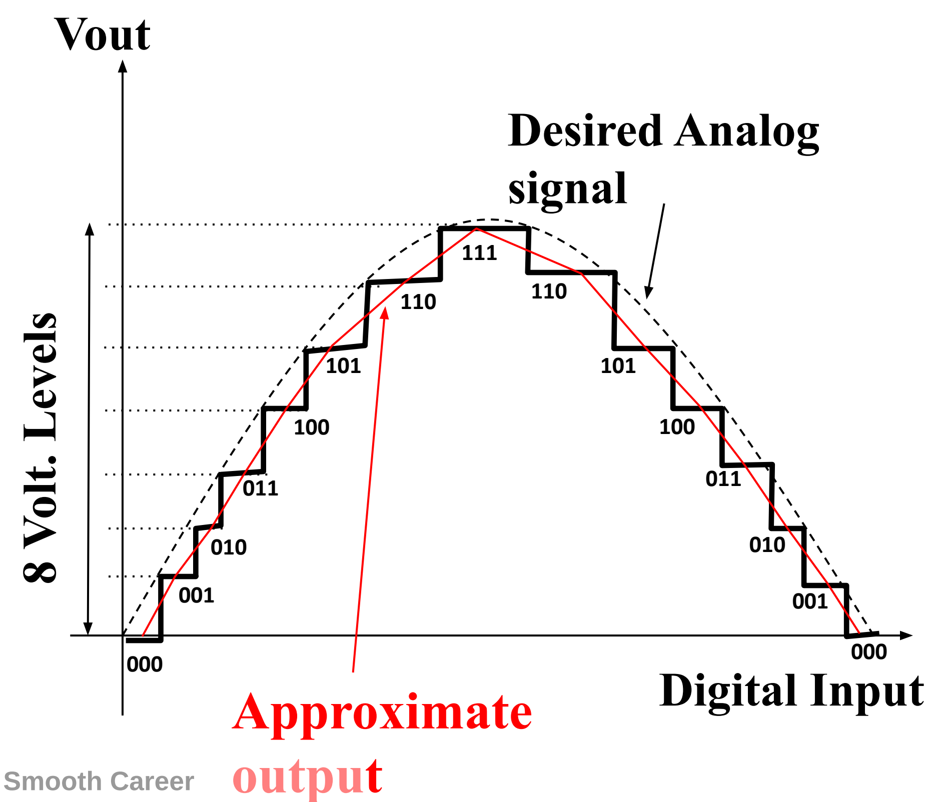
Resolution

Poor Resolution(1 bit)



Better Resolution(3 bit)



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Reference Voltage

- A specified voltage used to determine how each digital input will be assigned to each voltage division.
- Types:
  - Non-multiplier: internal, fixed, and defined by manufacturer
  - Multiplier: external, variable, user specified

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Settling Time

- Settling Time: The time required for the input signal voltage to settle to the expected output voltage(within +/- V_{LSB}).
- Any change in the input state will not be reflected in the output state immediately. There is a time lag, between the two events.

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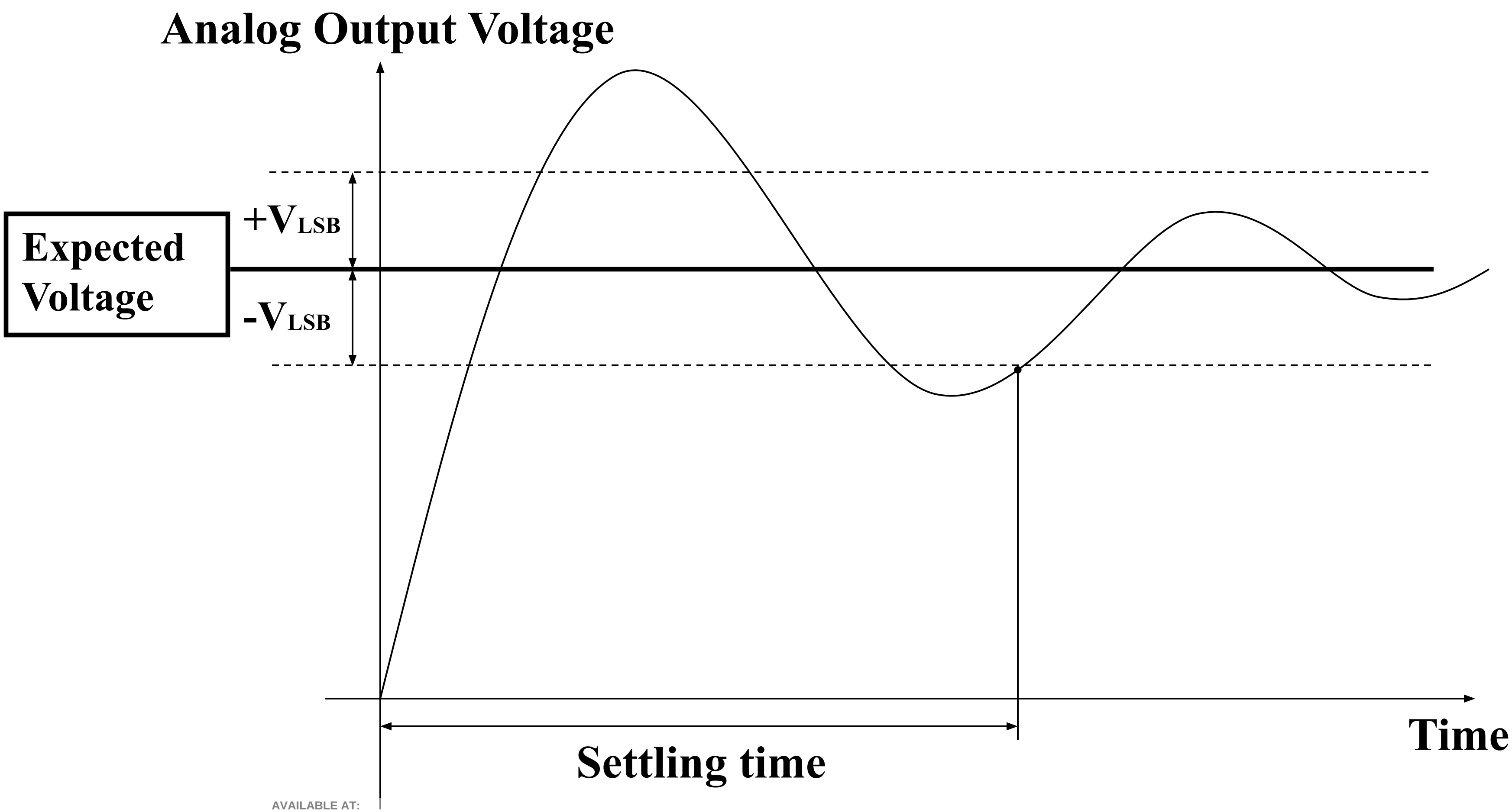
Settling Time



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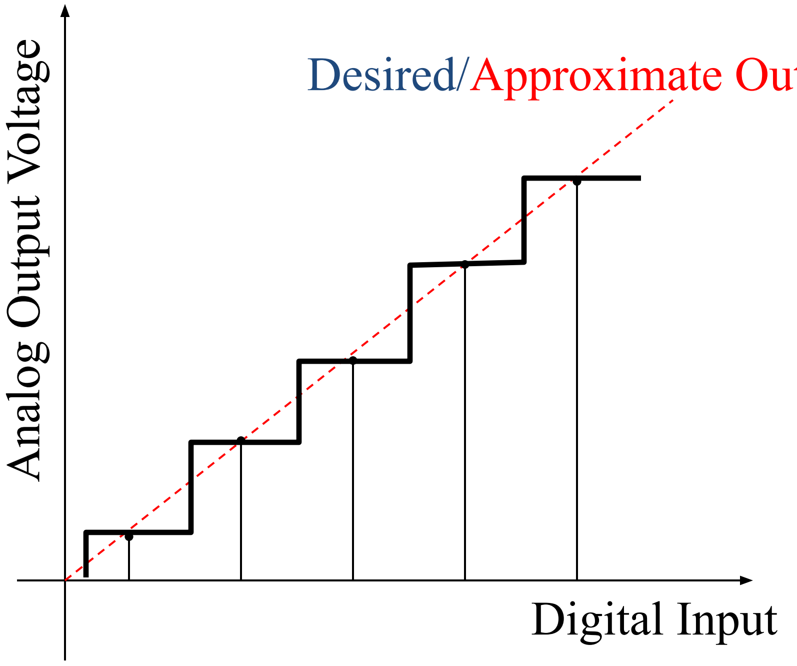
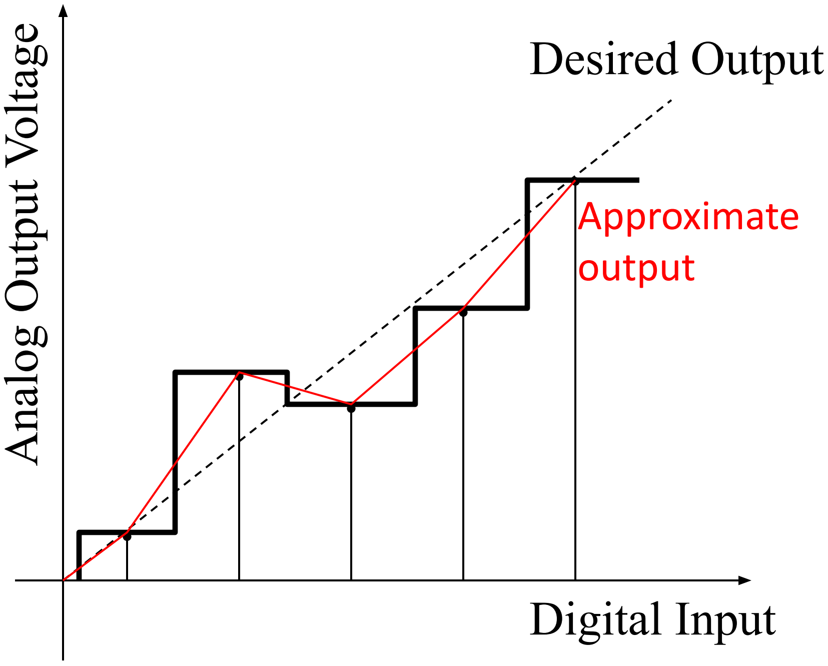
Linearity

Linearity(Ideal Case)



Perfect Agreement

NON-Linearity(Real World)



Miss-alignment

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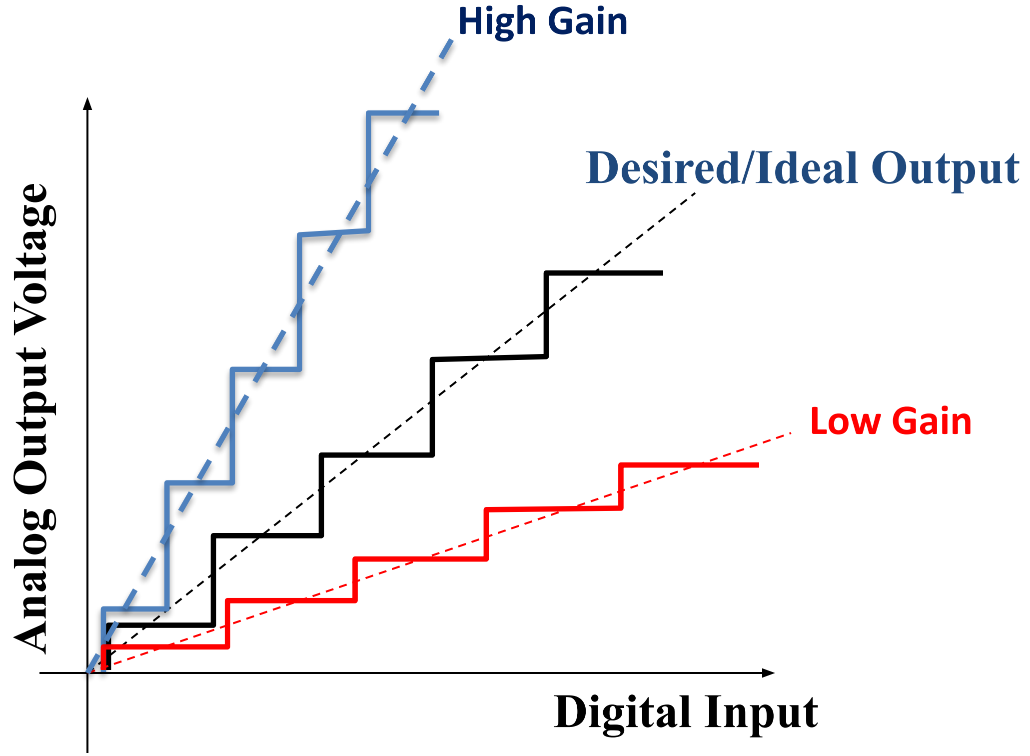
Errors Gain

- Gain Error: Difference in slope of the ideal curve and the actual DAC output

High Gain Error: Actual slope greater than ideal

Low Gain Error: Actual slope less than ideal



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Speed

- Rate of conversion of a single digital input to its analog equivalent
- Conversion Rate
  - Depends on clock speed of input signal
  - Depends on settling time of converter

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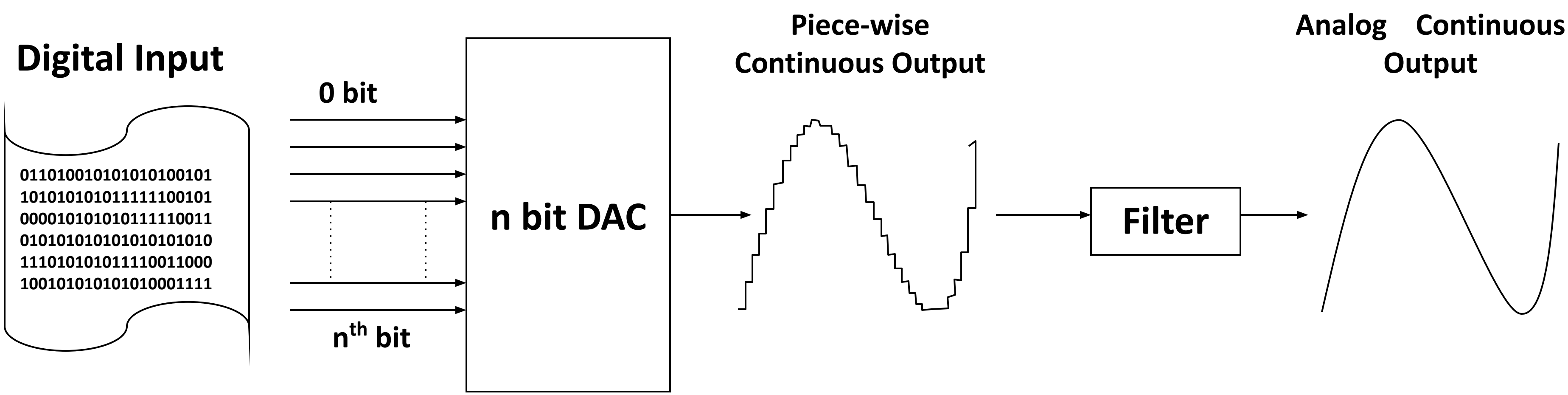
Generic Used: Audio player

- Used when a continuous analog signal is required.
- Signal from DAC can be smoothed by a Low pass filter



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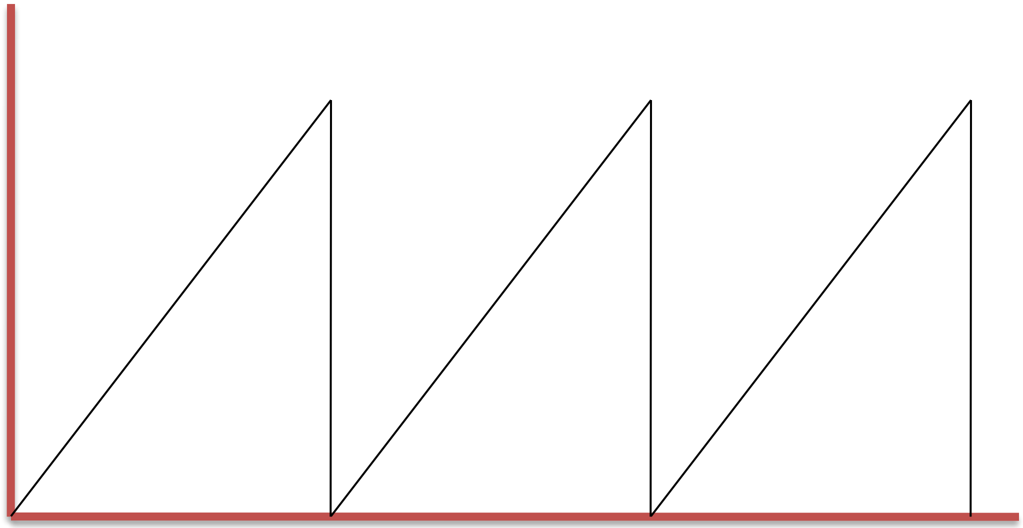
Interfacing 8-bitDAC with 8085

- Design an output port with Address FFH to interface 1408 DAC
- Write a program to generate a continuous RAMP waveform

Output



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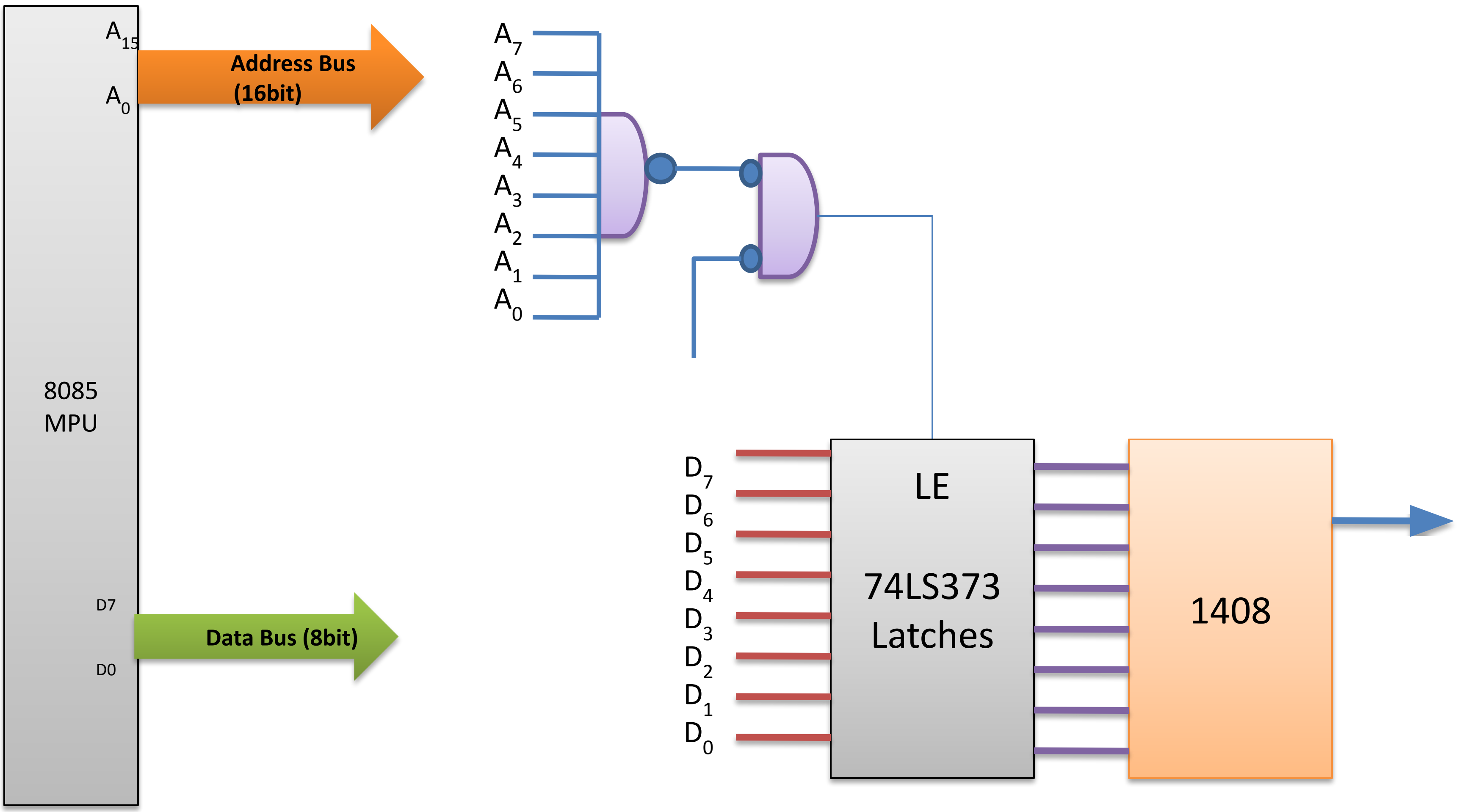
Time

Interfacing Diagram



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Program to generate continuous RAMP waveform

```
        MVI    A, 00H      ; Load Acc with first I/P
DTOA:OUT    FFH         ; Output to DAC
        MVI    B, COUNT     ; Setup Reg. for Delay
        DCR    B
        JNZ    DELAY
        INR    A        ; Next Input
        JMP    DTOA        ; Go back to Output
```

Slope of RAMP can be varied by changing Delay

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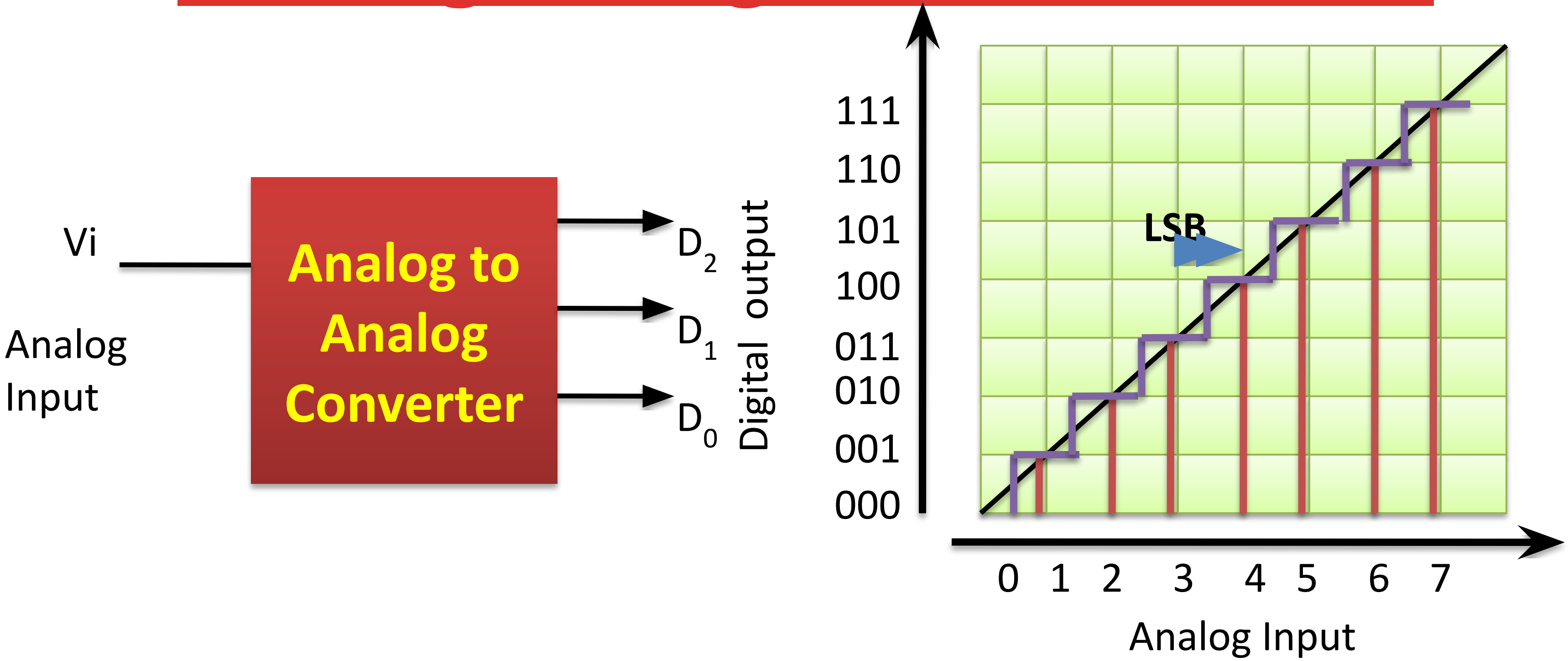
Analog to Digital Conversion



- ADC are slower then DAC
- Interfaced using Status Check

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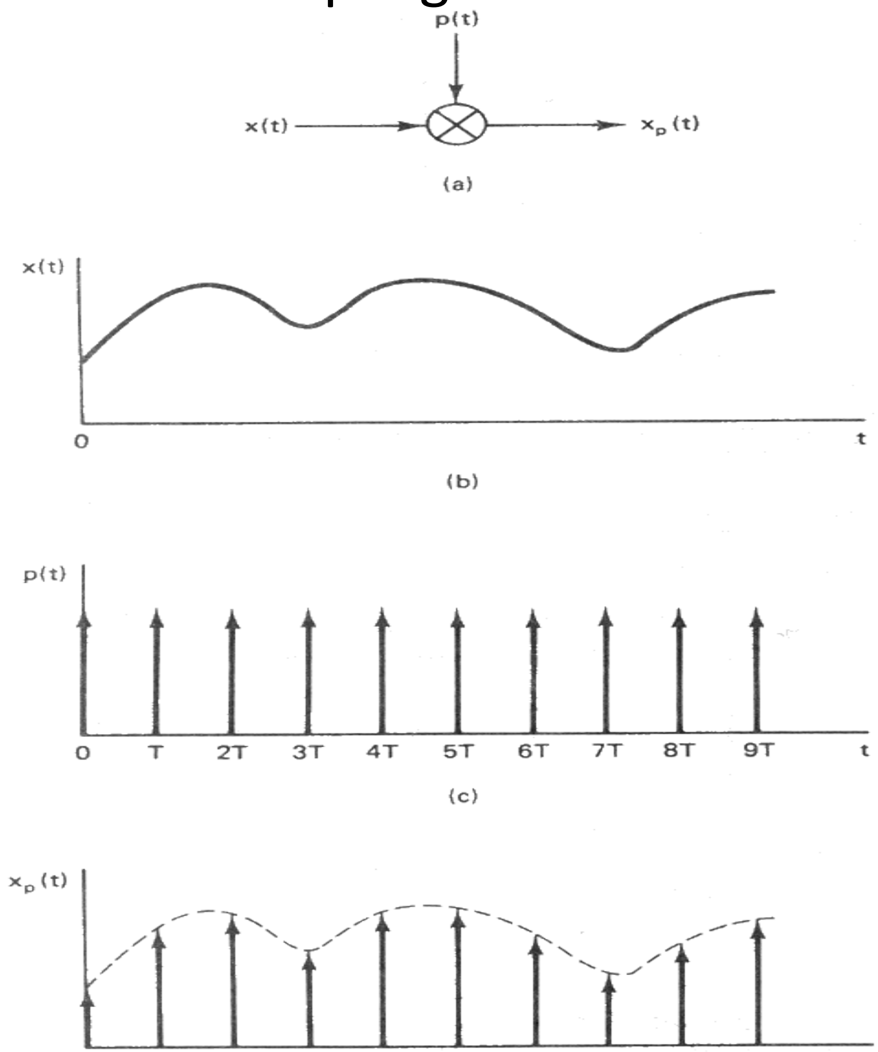
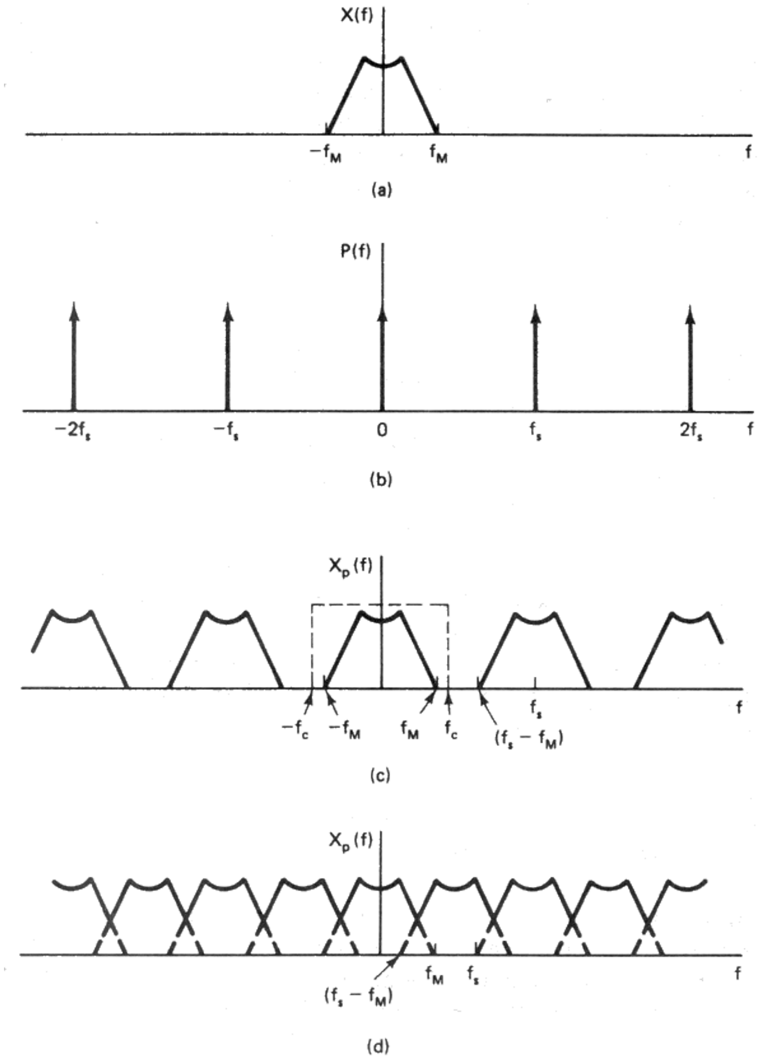
Sampling Concepts

- Sampling



- Fourier Transform



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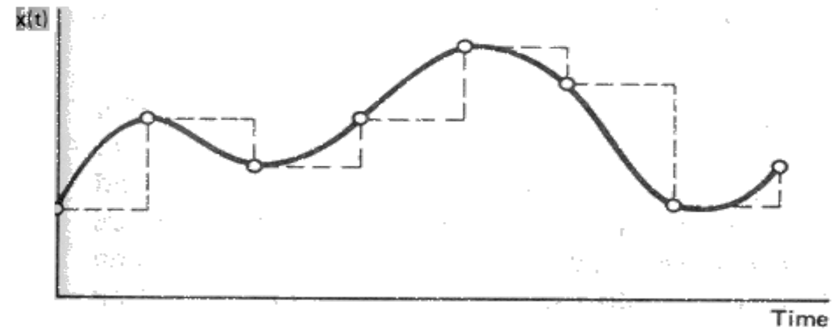
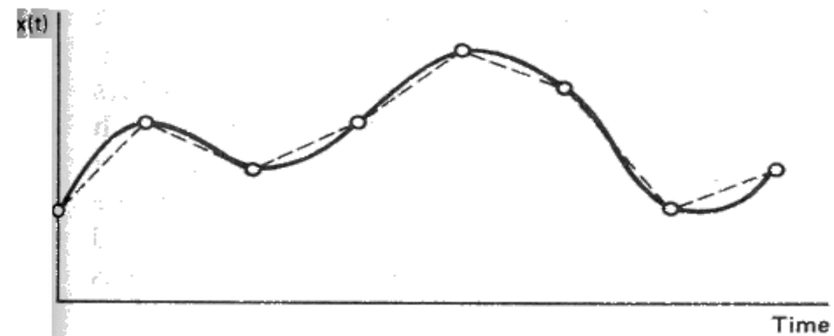
Interpolation

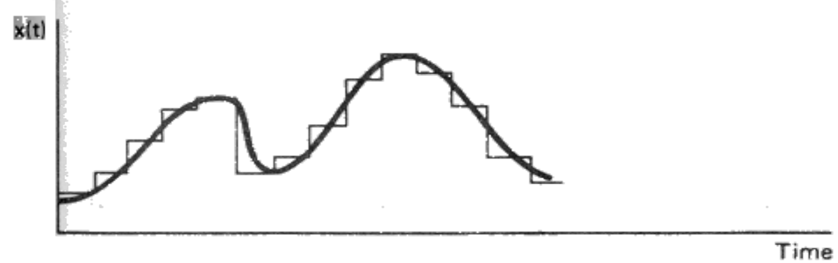
- The process of reconstructing a signal from its values at discrete instants of time
  - Zero order hold or One Point
  - Linear or Two Point
  - Band limited or Low pass Filtering



(a)



(b)



(c)

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Algorithm for finding unknown N

- Suppose my range is 0-1024 and assume some value of N between 0-1024
- You have to find the value of N
  - You can ask me (what about value X)
  - Answer (N>X, N<X, N==X)
  - Operation with X (X++; X*2, X^2, X/2, X--)

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Algorithm for finding unknown N

- What is the best Algorithm to find
  - Sequential (increase X till X==N) O(N) algorithm
  - Successive approximation: (Binary Search)
    - Say R/2 as CMP(R/2, N) === if equal stop

      IF (R/2 < N) CMP (R/2+R/4,N)

      ELSE CMP (R/2-R/4, N)
- If you have N persons to do the comparisons
  - Ask to all people and Gather the information
- Mix of Both approach
  - If you have M comparator

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A/D Conversion Techniques

- Counter or Tracking ADC
- Successive Approximation ADC
  - Most Commonly Used
- Parallel or Flash ADC
  - Fast Conversion

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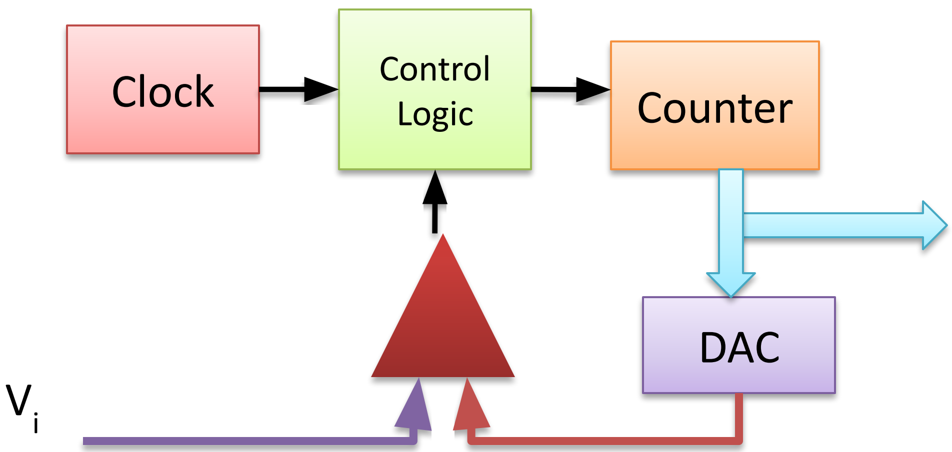
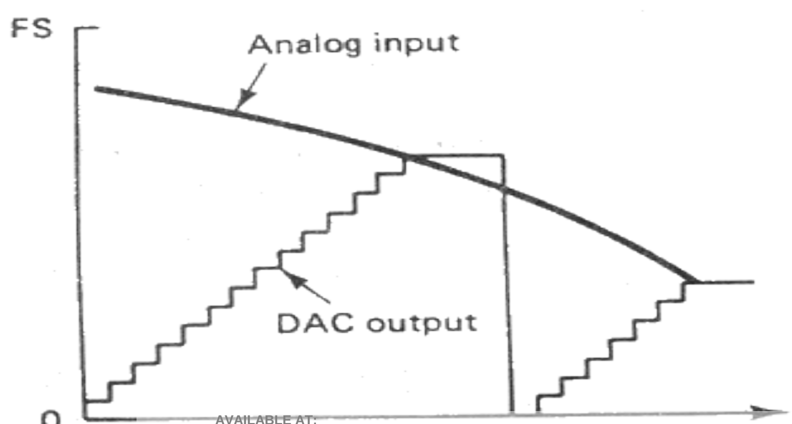
Counter Type ADC

- Block diagram



- Waveform



- Operation
  - Reset and Start Counter
  - DAC convert Digital output of Counter to Analog signal
  - Compare Analog input and Output of DAC
    - $Vi < V_{DAC}$
      - Continue counting
    - $Vi = V_{DAC}$
      - Stop counting
  - Digital Output = Output of Counter
- Disadvantage
  - Conversion time is varied
    - 2^n Clock Period for Full Scale input

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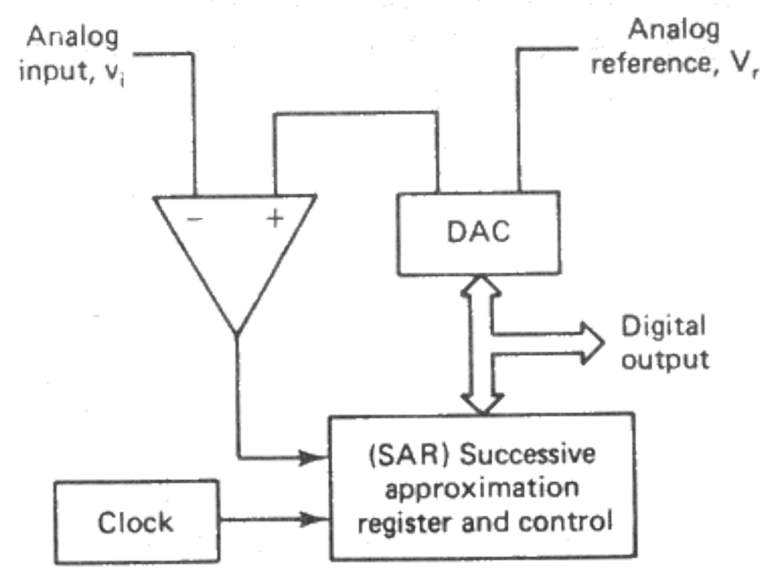
Successive Approximation ADC

- Most Commonly used in medium to high speed Converters
- Based on approximating the input signal with binary code and then successively revising this approximation until best approximation is achieved
- SAR(Successive Approximation Register) holds the current binary value

- Block Diagram



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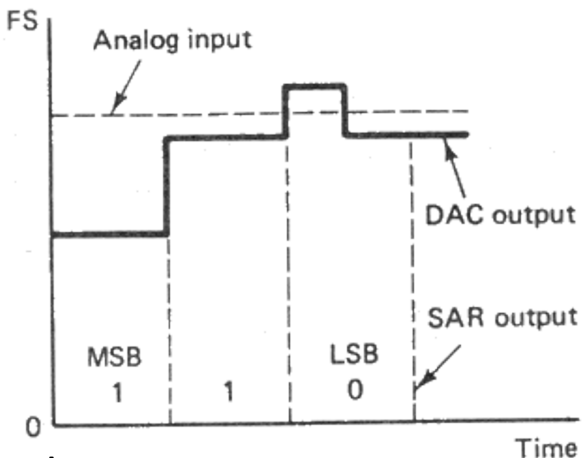
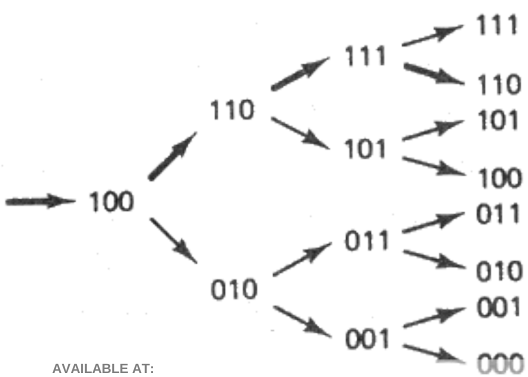
Successive Approximation ADC

- Circuit waveform



- Logic Flow



- Conversion Time
  - n clock for n-bit ADC
  - Fixed conversion time
- Serial Output is easily generated
  - Bit decision are made in serial order

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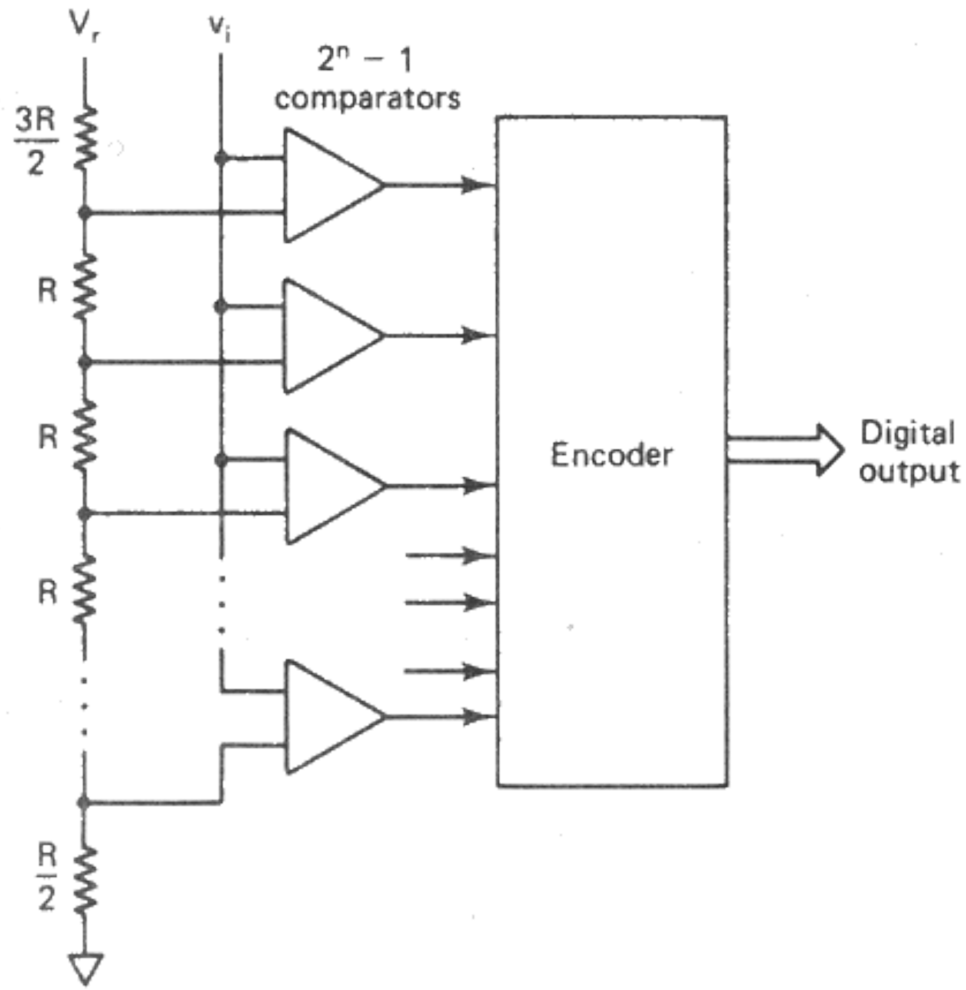
Parallel or Flash ADC

- Very High speed conversion
  - Up to 100MHz for 8 bit resolution
  - Video, Radar, Digital Oscilloscope
- Single Step Conversion
  - $2^n - 1$ comparator
  - Precision Resistive Network
  - Encoder
- Resolution is limited
  - Large number of comparator in IC



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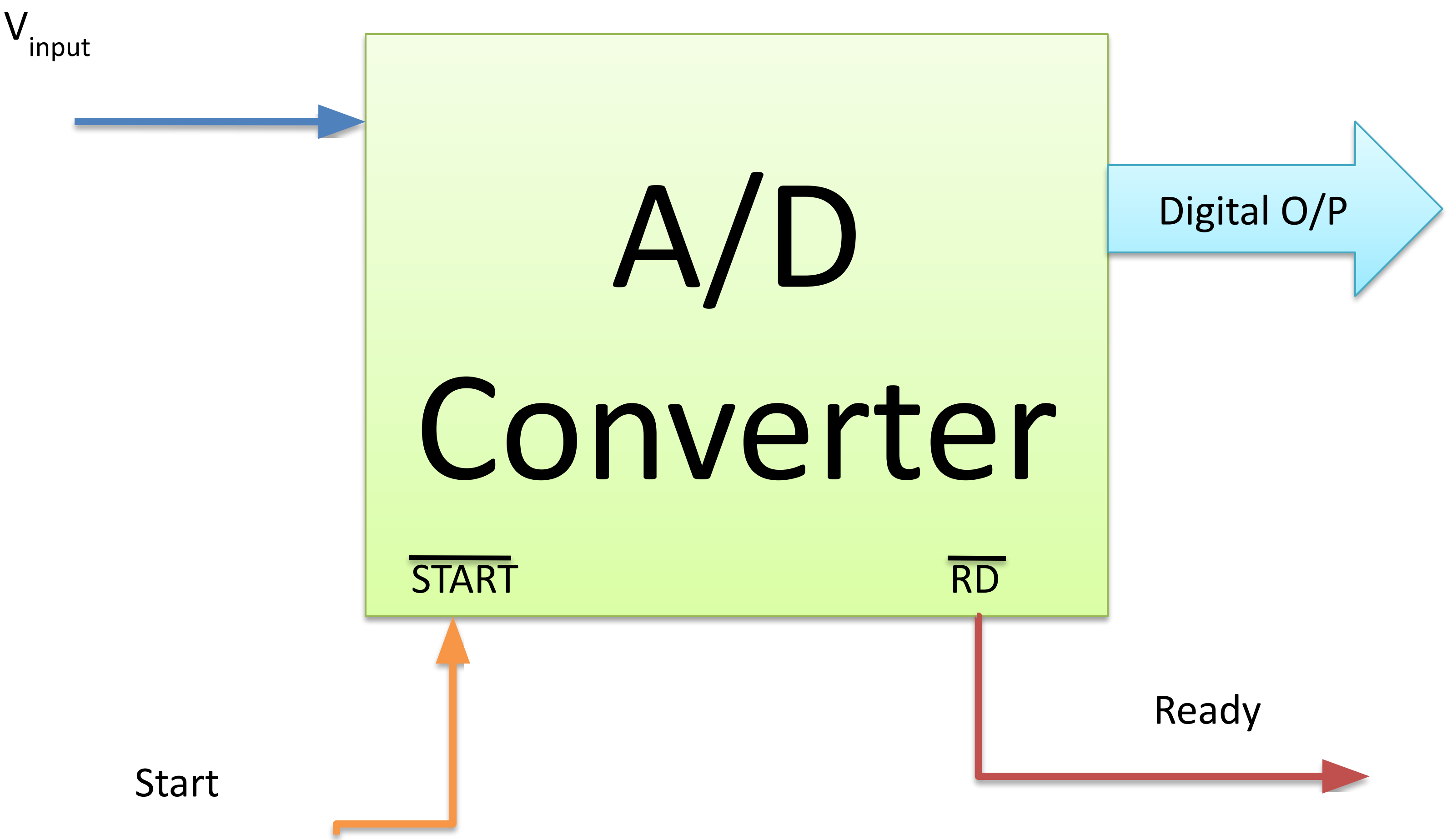
Generic ADC



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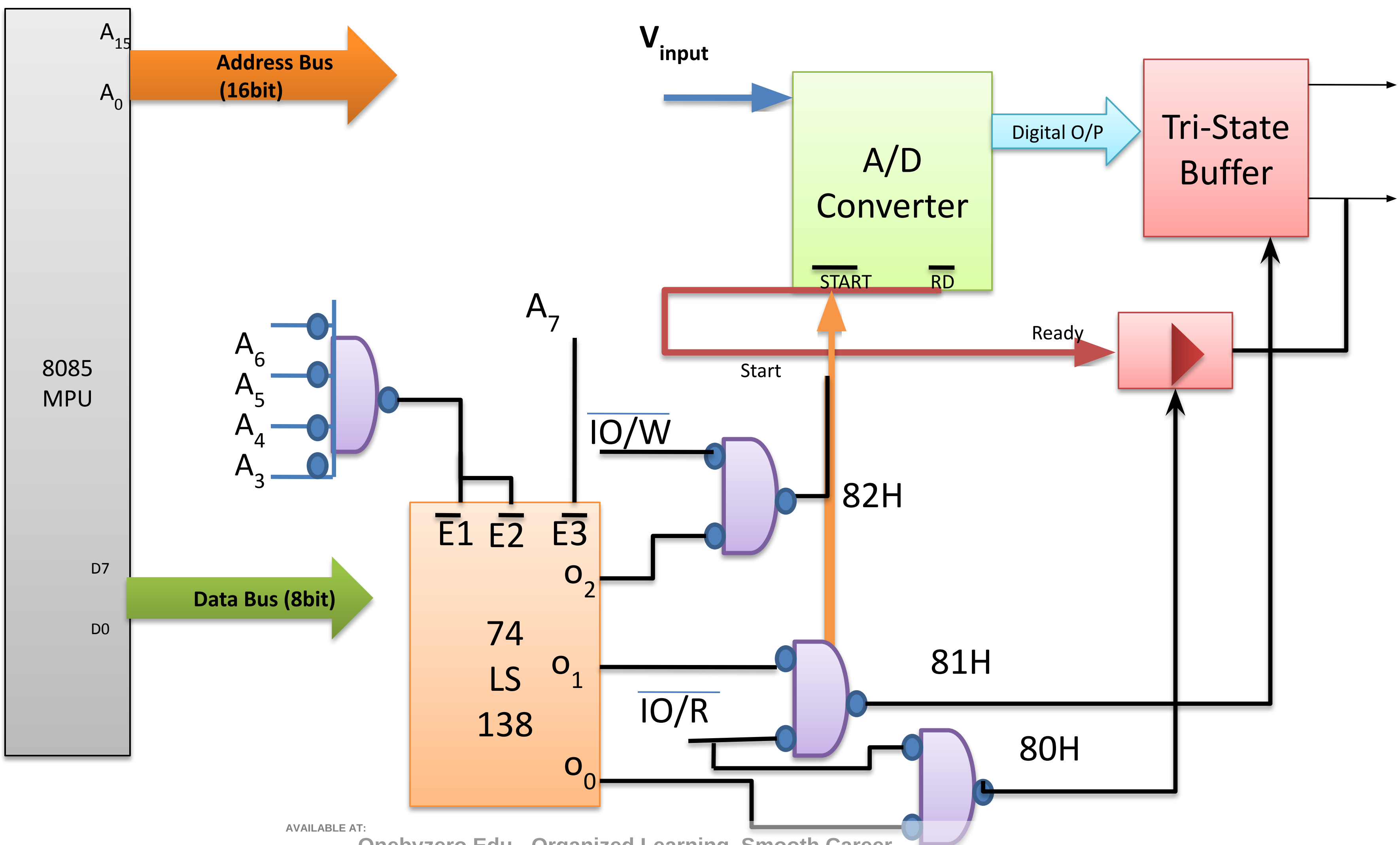
Interface ADC using Status Check



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Program to Interface ADC

```
        OUT 82H   ; Start Conversion
TEST:   IN 80H  ;Read DR Status
        RAR       ; Rotate Do to carry
        JC TEST  ; if Do==1 conv. done
        IN 81H   ; Read the output
        RET           ; Return
```

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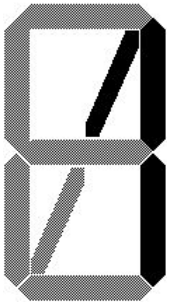
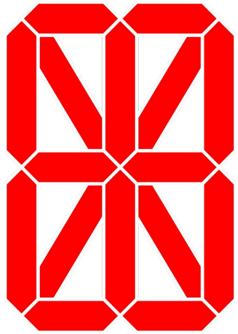
Display

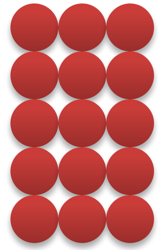
7 Seg



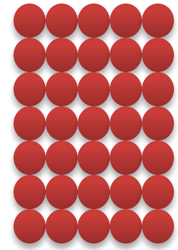
9 Seg



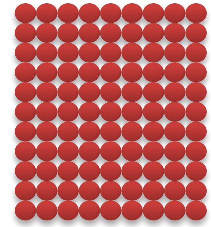
16 Seg



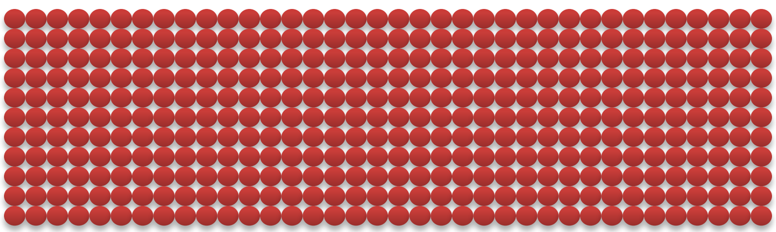
3x5 DotMatix



5x7



9x11



Dot Matrix Display Panel

25x80 character monitor

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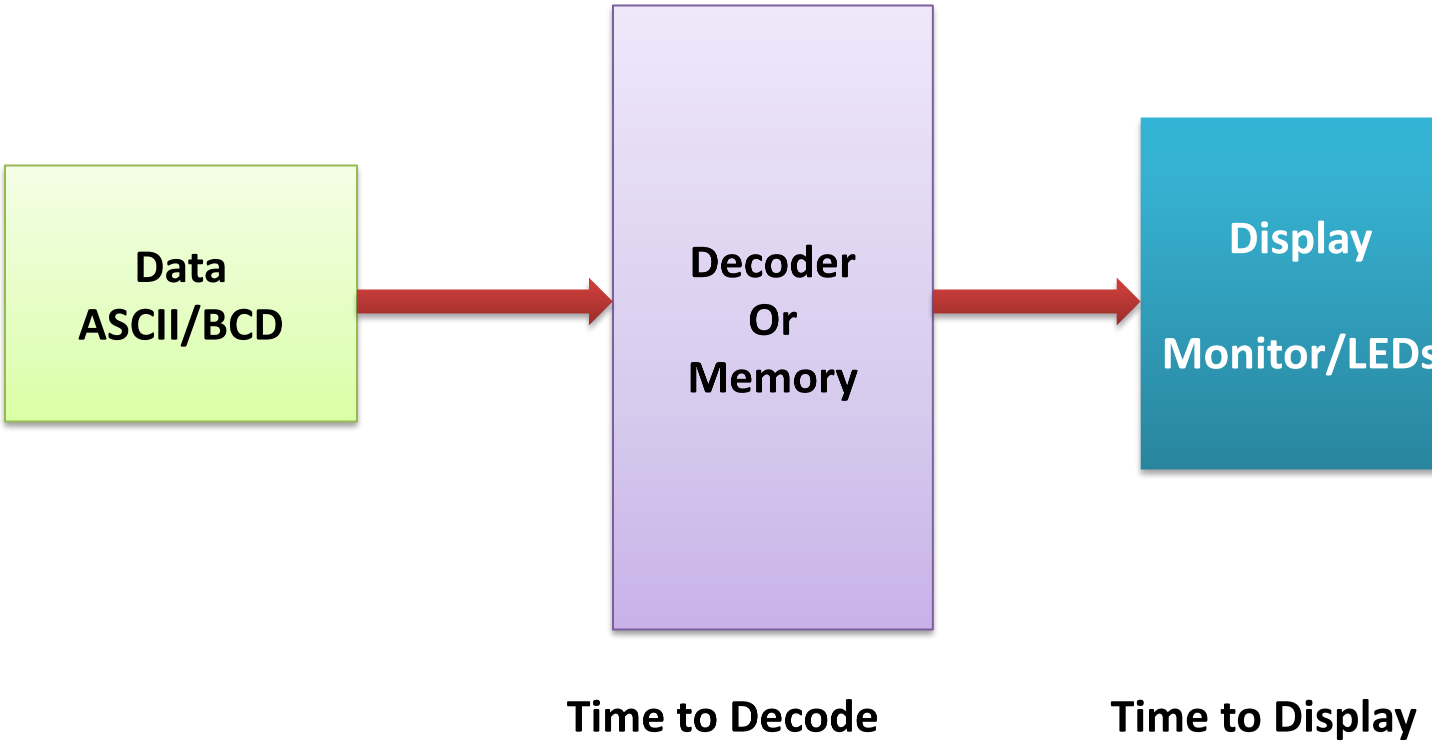
Generic Model of Display



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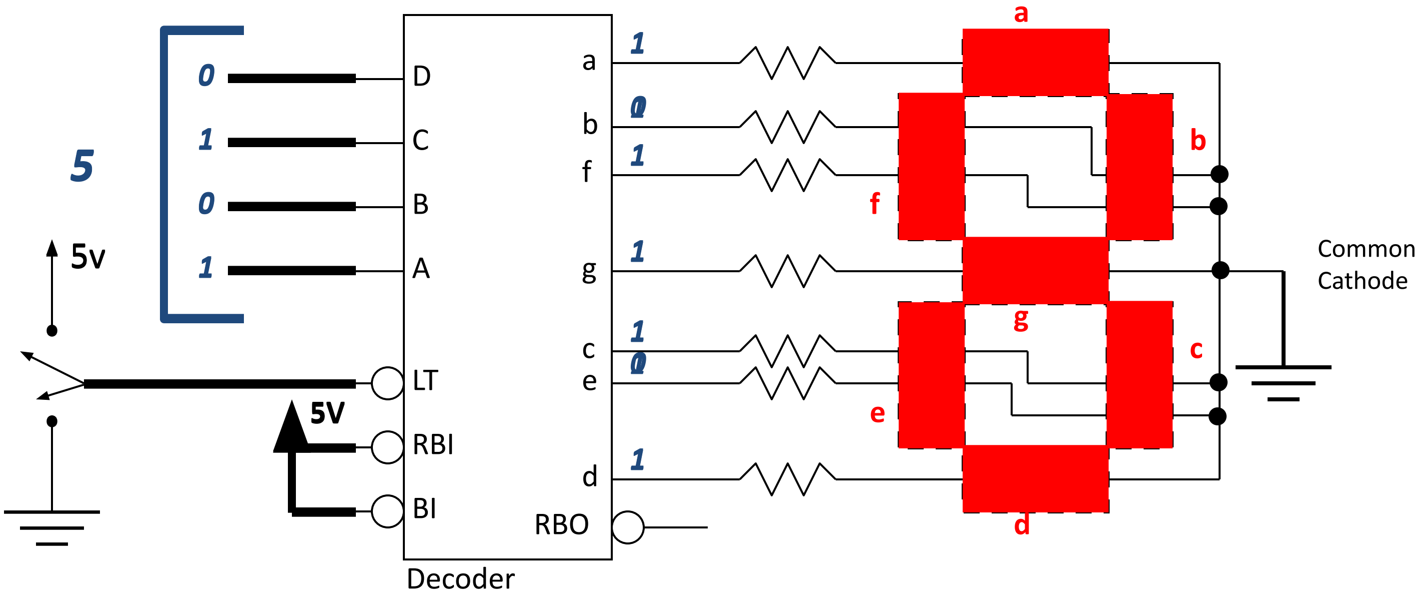
7 Segment LED Interfaces

- Data to 7 Seg Decoder



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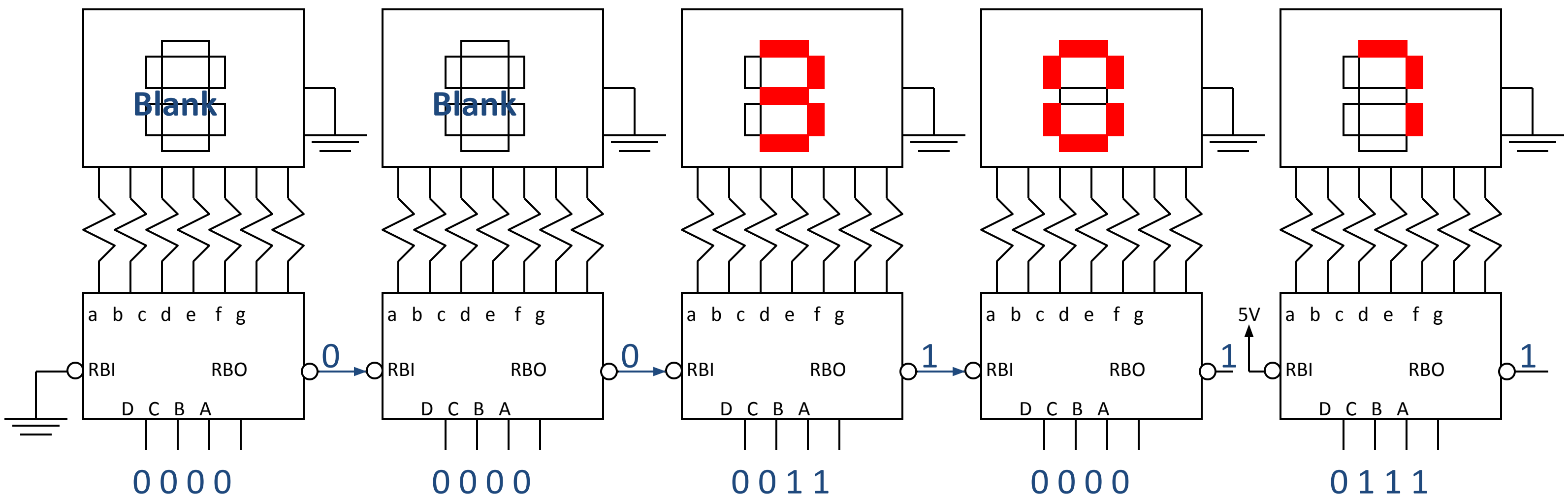
Multiple 7 Segment LED Interfaces

- Data to 7 Seg Decoder



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Reference

- R S Gaonkar, “Microprocessor Architecture”, Unit II preface, Chapter 13

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