William Stallings Computer Organization and Architecture

Chapter 4

Internal Memory

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Characteristics

- ⌘Location
- ⌘Capacity
- ⌘Unit of transfer
- ⌘Access method
- ⌘Performance
- ⌘Physical type
- ⌘Physical characteristics
- ⌘Organisation

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Location

- CPU
- Internal
- External

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Capacity

- Word size
  - The natural unit of organisation
- Number of words
  - or Bytes

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Unit of Transfer

- Internal
  - Usually governed by data bus width
- External
  - Usually a block which is much larger than a word
- Addressable unit
  - Smallest location which can be uniquely addressed
  - Word internally
  - Cluster on M$ disks

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Access Methods (1)

- Sequential
  - Start at the beginning and read through in order
  - Access time depends on location of data and previous location
  - e.g. tape
- Direct
  - Individual blocks have unique address
  - Access is by jumping to vicinity plus sequential search
  - Access time depends on location and previous location
  - e.g. disk

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Access Methods (2)

- Random
  - Individual addresses identify locations exactly
  - Access time is independent of location or previous access
  - e.g. RAM
- Associative
  - Data is located by a comparison with contents of a portion of the store
  - Access time is independent of location or previous access
  - e.g. cache

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Memory Hierarchy

- Registers
  - In CPU
- Internal or Main memory
  - May include one or more levels of cache
  - “RAM”
- External memory
  - Backing store

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Performance

- Access time
  - Time between presenting the address and getting the valid data
- Memory Cycle time
  - Time may be required for the memory to “recover” before next access
  - Cycle time is access + recovery
- Transfer Rate
  - Rate at which data can be moved

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Physical Types

- Semiconductor
  - RAM
- Magnetic
  - Disk & Tape
- Optical
  - CD & DVD
- Others
  - Bubble
  - Hologram

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Physical Characteristics

- ⌘Decay
- ⌘Volatility
- ⌘Erasable
- ⌘Power consumption

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Organisation

- ⌘Physical arrangement of bits into words
- ⌘Not always obvious
- ⌘e.g. interleaved

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The Bottom Line

- How much?
  - Capacity
- How fast?
  - Time is money
- How expensive?

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Hierarchy List

- Registers
- L1 Cache
- L2 Cache
- Main memory
- Disk cache
- Disk
- Optical
- Tape

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So you want fast?

- It is possible to build a computer which uses only static RAM (see later)
- This would be very fast
- This would need no cache
  - How can you cache cache?
- This would cost a very large amount

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Locality of Reference

- During the course of the execution of a program, memory references tend to cluster
- e.g. loops

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Semiconductor Memory

- RAM
  - Misnamed as all semiconductor memory is random access
  - Read/Write
  - Volatile
  - Temporary storage
  - Static or dynamic

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Dynamic RAM

- Bits stored as charge in capacitors
- Charges leak
- Need refreshing even when powered
- Simpler construction
- Smaller per bit
- Less expensive
- Need refresh circuits
- Slower
- Main memory

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Static RAM

- ⌘Bits stored as on/off switches
- ⌘No charges to leak
- ⌘No refreshing needed when powered
- ⌘More complex construction
- ⌘Larger per bit
- ⌘More expensive
- ⌘Does not need refresh circuits
- ⌘Faster
- ⌘Cache

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Read Only Memory (ROM)

- ⌘ Permanent storage
- ⌘ Microprogramming (see later)
- ⌘ Library subroutines
- ⌘ Systems programs (BIOS)
- ⌘ Function tables

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Types of ROM

- Written during manufacture
  - Very expensive for small runs
- Programmable (once)
  - PROM
  - Needs special equipment to program
- Read “mostly”
  - Erasable Programmable (EPROM)
    - Erased by UV
  - Electrically Erasable (EEPROM)
    - Takes much longer to write than read
  - Flash memory
    - Erase whole memory electrically

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Organisation in detail

- A 16Mbit chip can be organised as 1M of 16 bit words
- A bit per chip system has 16 lots of 1Mbit chip with bit 1 of each word in chip 1 and so on
- A 16Mbit chip can be organised as a 2048 x 2048 x 4bit array
  - Reduces number of address pins
    - Multiplex row address and column address
    - 11 pins to address (2^{11}=2048)
    - Adding one more pin doubles range of values so x4 capacity

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Refreshing

- Refresh circuit included on chip
- Disable chip
- Count through rows
- Read & Write back
- Takes time
- Slows down apparent performance

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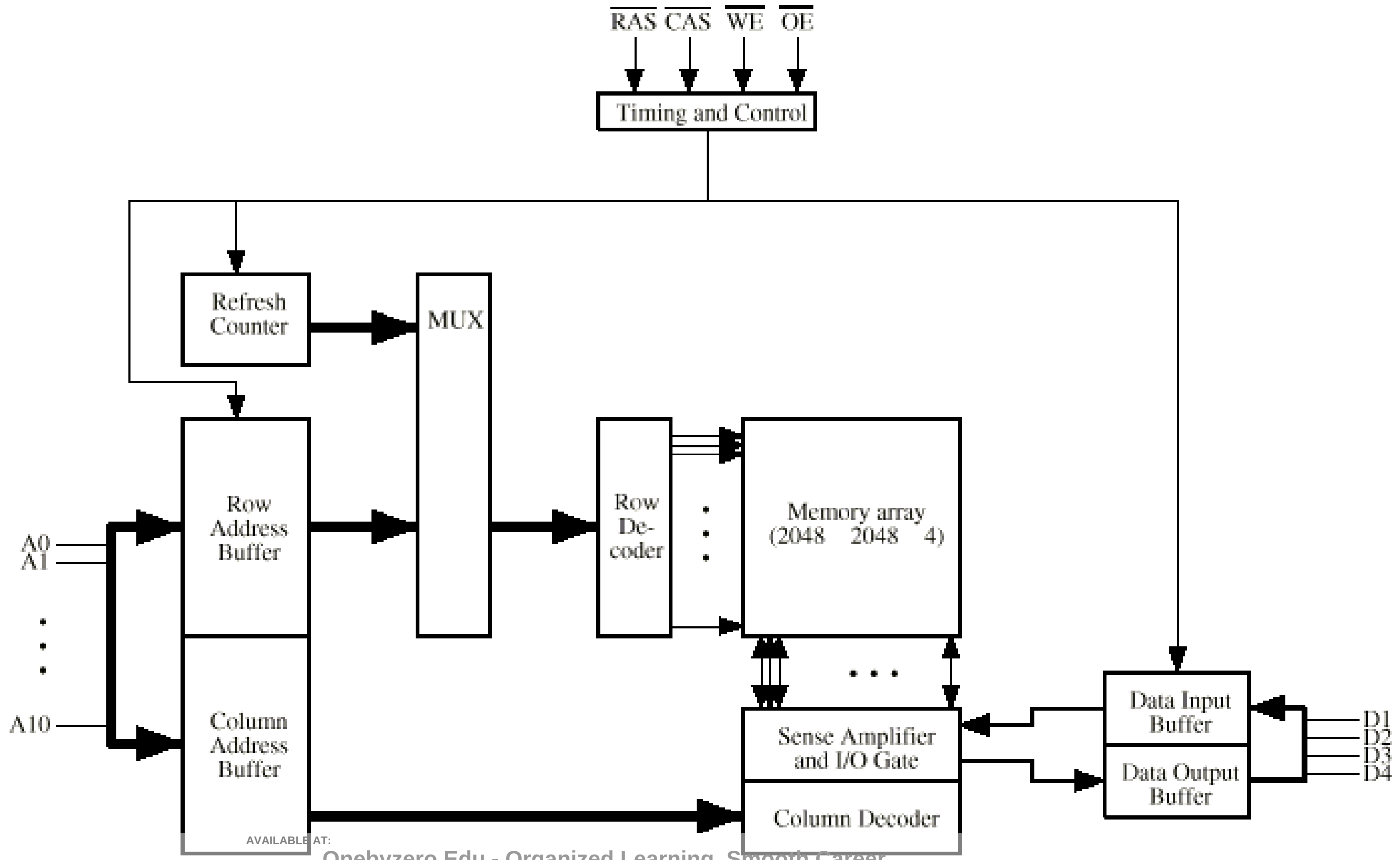
Typical 16 Mb DRAM (4M x 4)



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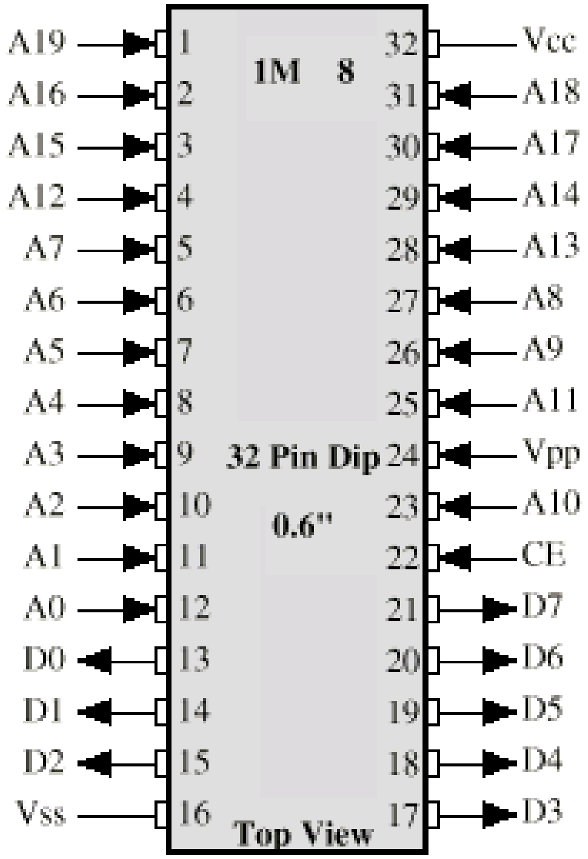
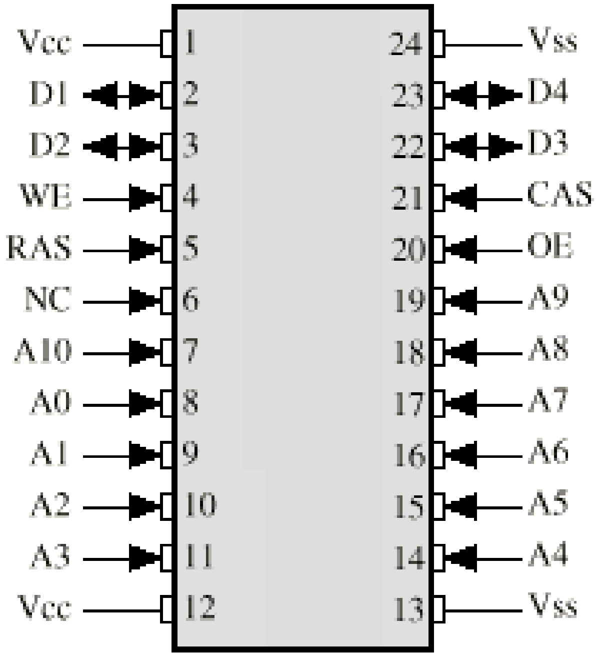
Packaging



(a) 8 Mbit EPROM



(b) 16 Mbit DRAM

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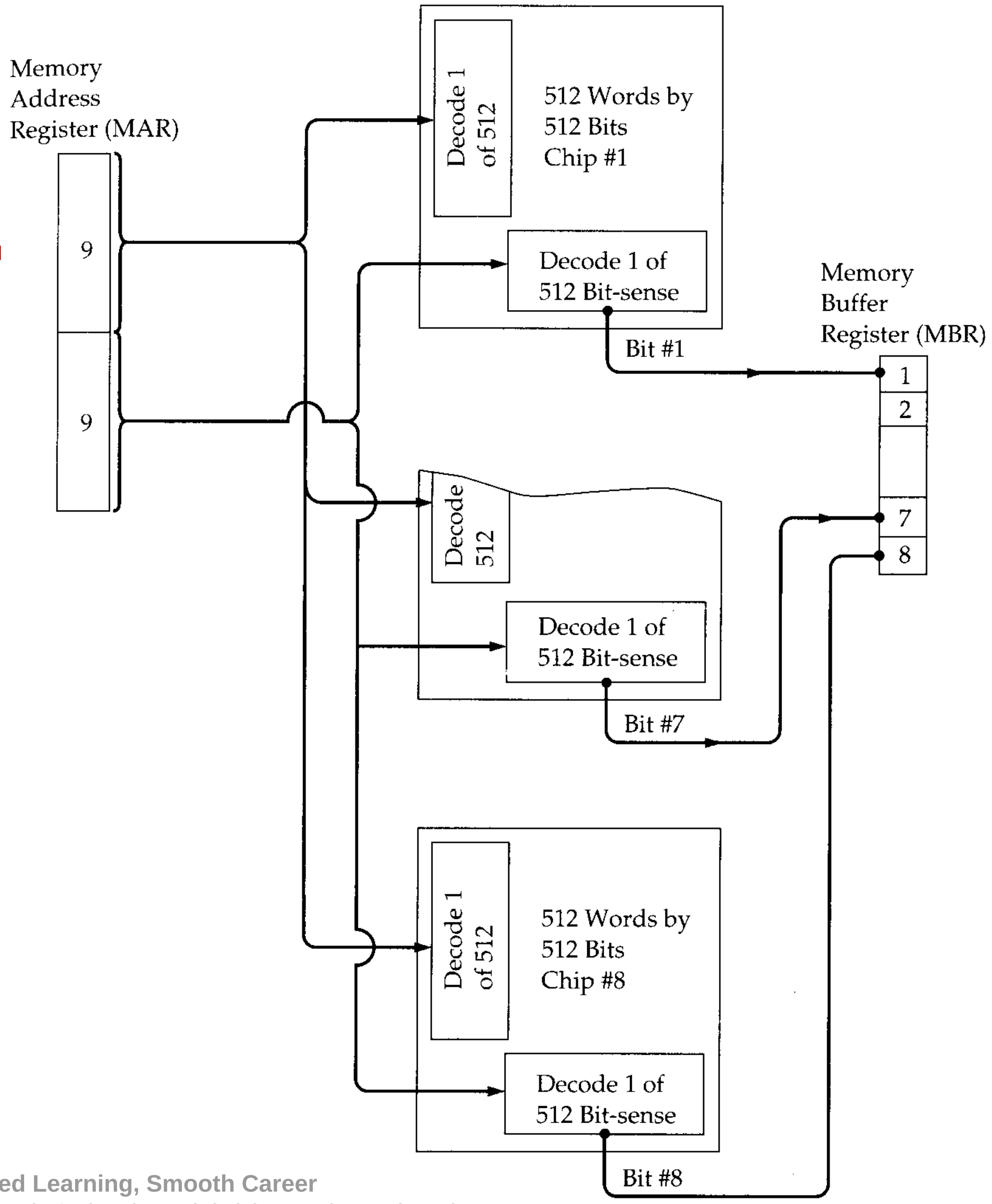
Module Organisation



Memory Address Register (MAR)
9
9
Decode 1 of 512
512 Words by 512 Bits Chip #1
Decode 1 of 512 Bit-sense
Bit #1
Memory Buffer Register (MBR)
1
2
7
8
Decode 512
Decode 1 of 512 Bit-sense
Bit #7
Decode 1 of 512
512 Words by 512 Bits Chip #8
Decode 1 of 512 Bit-sense
Bit #8

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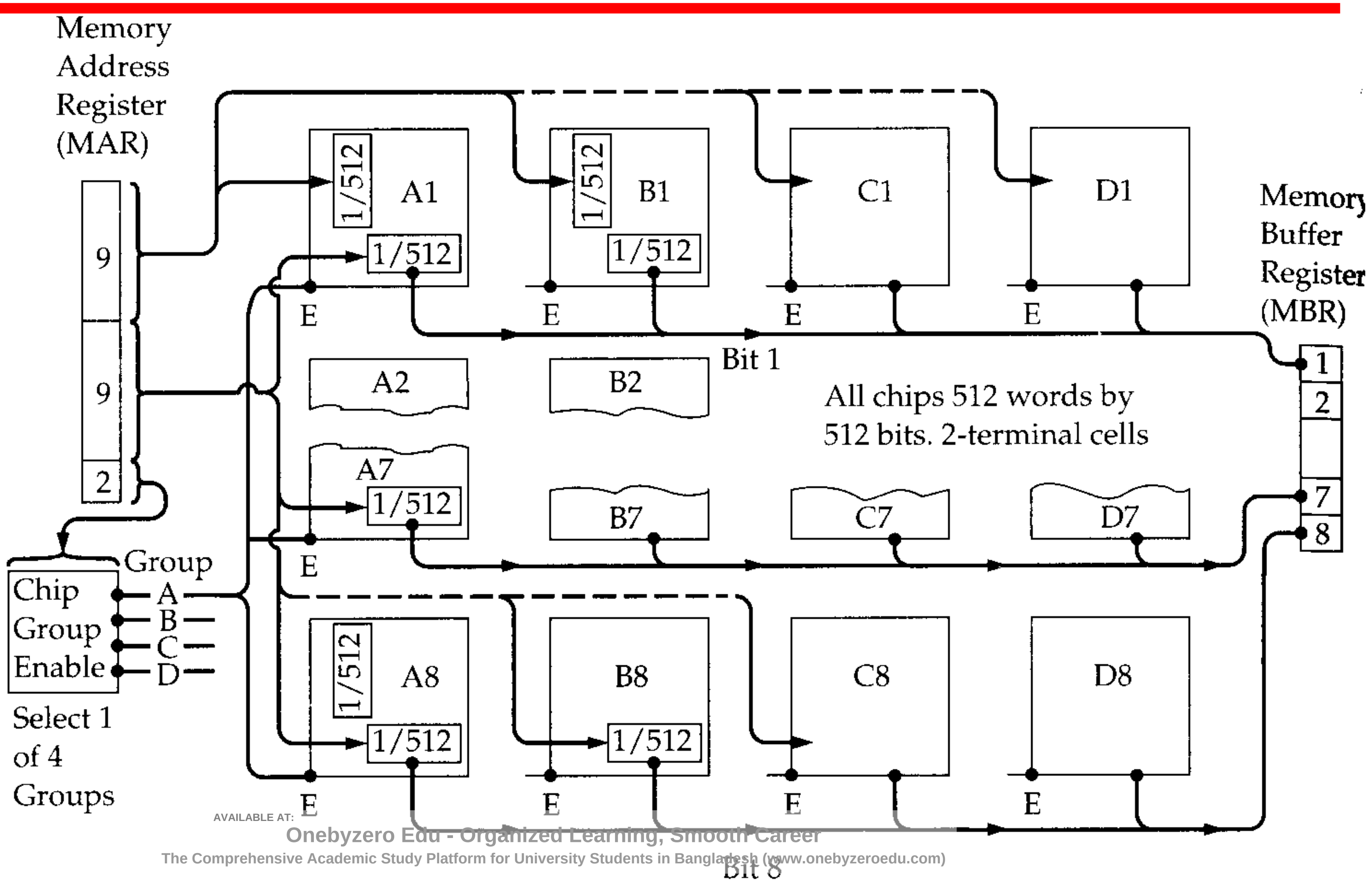
Module Organisation (2)


Memory Address Register (MAR)
9
9
2
Chip Group Enable
Group
A
B
C
D
Select 1 of 4 Groups
1/512
A1
1/512
B1
C1
D1
E
A2
B2
A7
B7
C7
D7
A8
B8
C8
D8
Bit 1
Bit 8
All chips 512 words by 512 bits. 2-terminal cells
Memory Buffer Register (MBR)
1
2
7
8

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Error Correction

- Hard Failure
  - Permanent defect
- Soft Error
  - Random, non-destructive
  - No permanent damage to memory
- Detected using Hamming error correcting code

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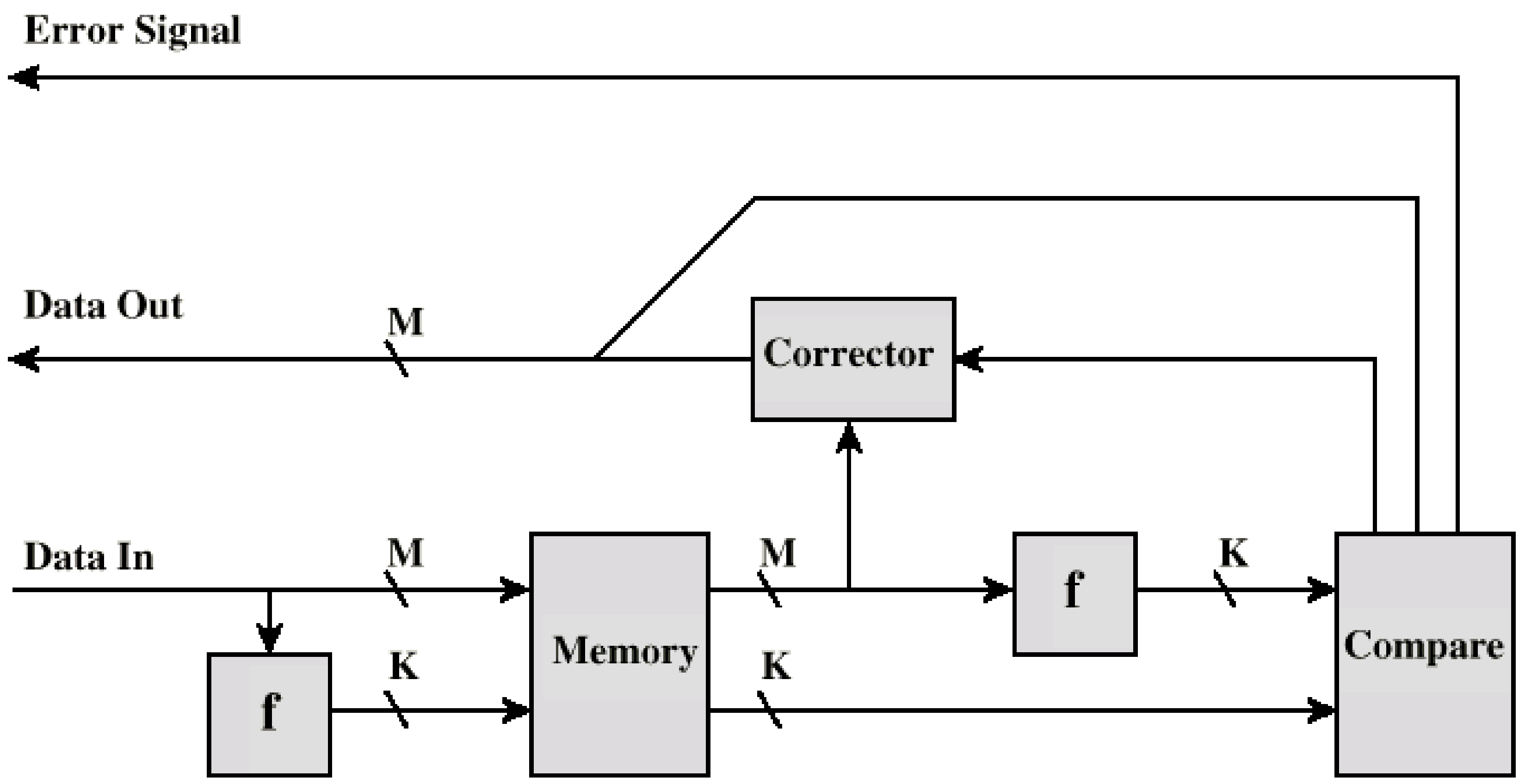
Error Correcting Code Function



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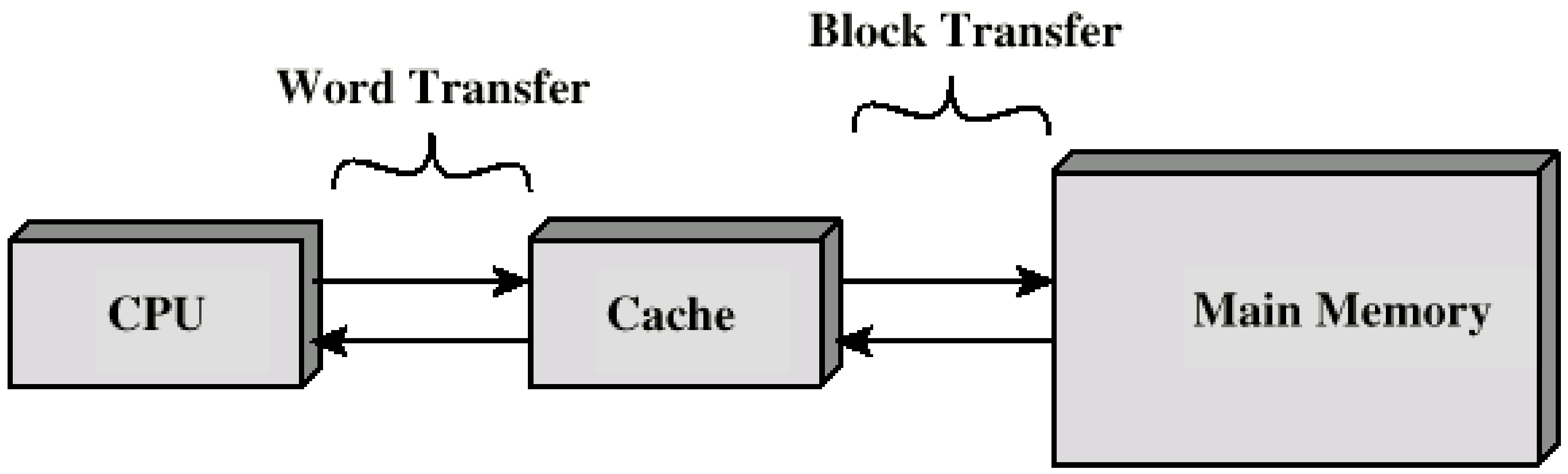
Cache

- ⌘Small amount of fast memory
- ⌘Sits between normal main memory and CPU
- ⌘May be located on CPU chip or module



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Cache operation - overview

- ⌘CPU requests contents of memory location
- ⌘Check cache for this data
- ⌘If present, get from cache (fast)
- ⌘If not present, read required block from main memory to cache
- ⌘Then deliver from cache to CPU
- ⌘Cache includes tags to identify which block of main memory is in each cache slot

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Cache Design

- Size
- Mapping Function
- Replacement Algorithm
- Write Policy
- Block Size
- Number of Caches

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Size does matter

- Cost
  - More cache is expensive
- Speed
  - More cache is faster (up to a point)
  - Checking cache for data takes time

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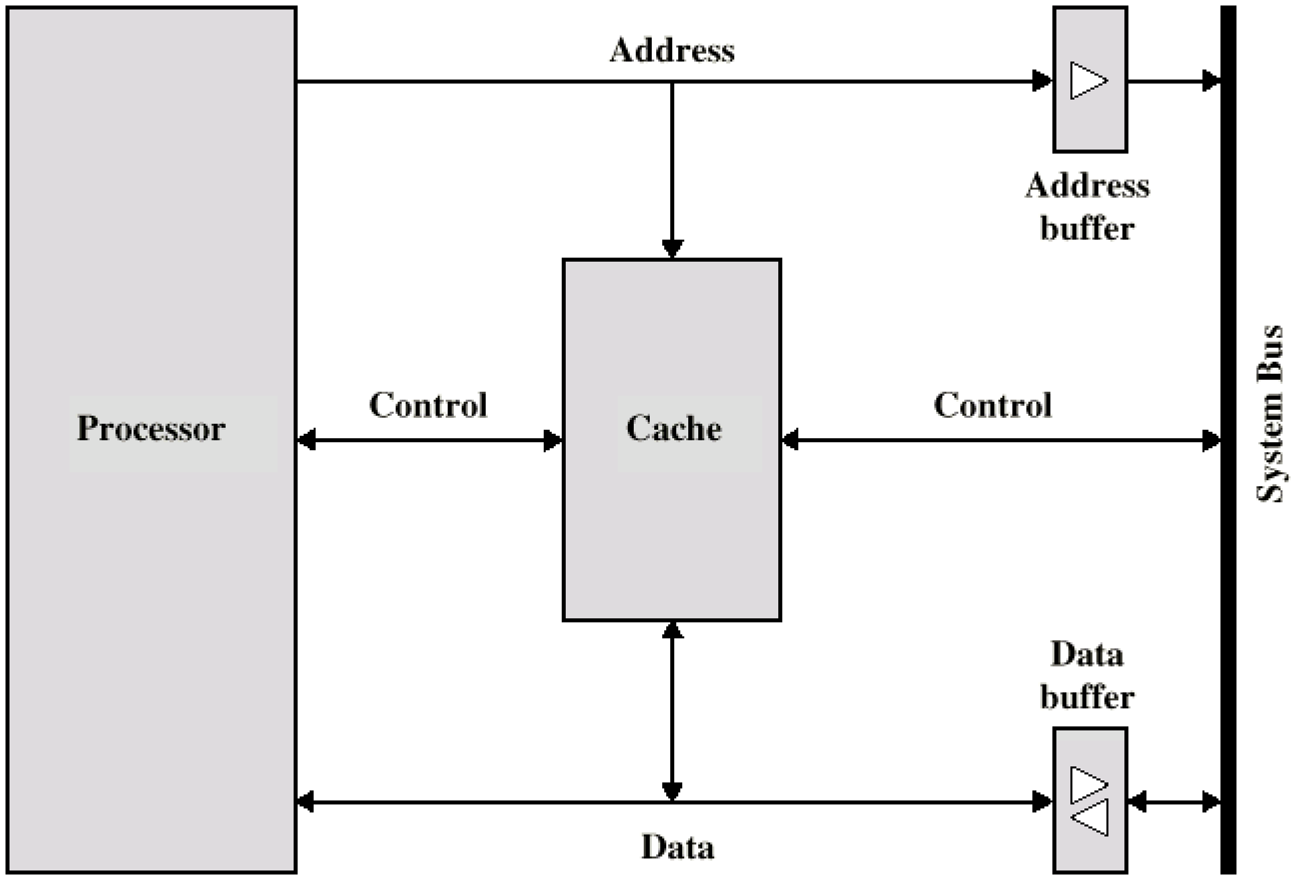
Typical Cache Organization



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Mapping Function

- Cache of 64kByte
- Cache block of 4 bytes
  - i.e. cache is 16k (2^{14}) lines of 4 bytes
- 16MBytes main memory
- 24 bit address
  - (2^{24}=16M)

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Direct Mapping

- Each block of main memory maps to only one cache line
  - i.e. if a block is in cache, it must be in one specific place
- Address is in two parts
- Least Significant w bits identify unique word
- Most Significant s bits specify one memory block
- The MSBs are split into a cache line field r and a tag of s-r (most significant)

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Direct Mapping Address Structure

Tag s-r	Line or Slot r	Word w
8	14	2

- 24 bit address
- 2 bit word identifier (4 byte block)
- 22 bit block identifier
  - 8 bit tag (=22-14)
  - 14 bit slot or line
- No two blocks in the same line have the same Tag field
- Check contents of cache by finding line and checking Tag

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Direct Mapping Cache Line Table

Cache line	Main Memory blocks held
0	0, m, 2m, 3m…2^s-m
1	1,m+1, 2m+1…2^s-m+1
m-1	m-1, 2m-1,3m-1…2^s-1

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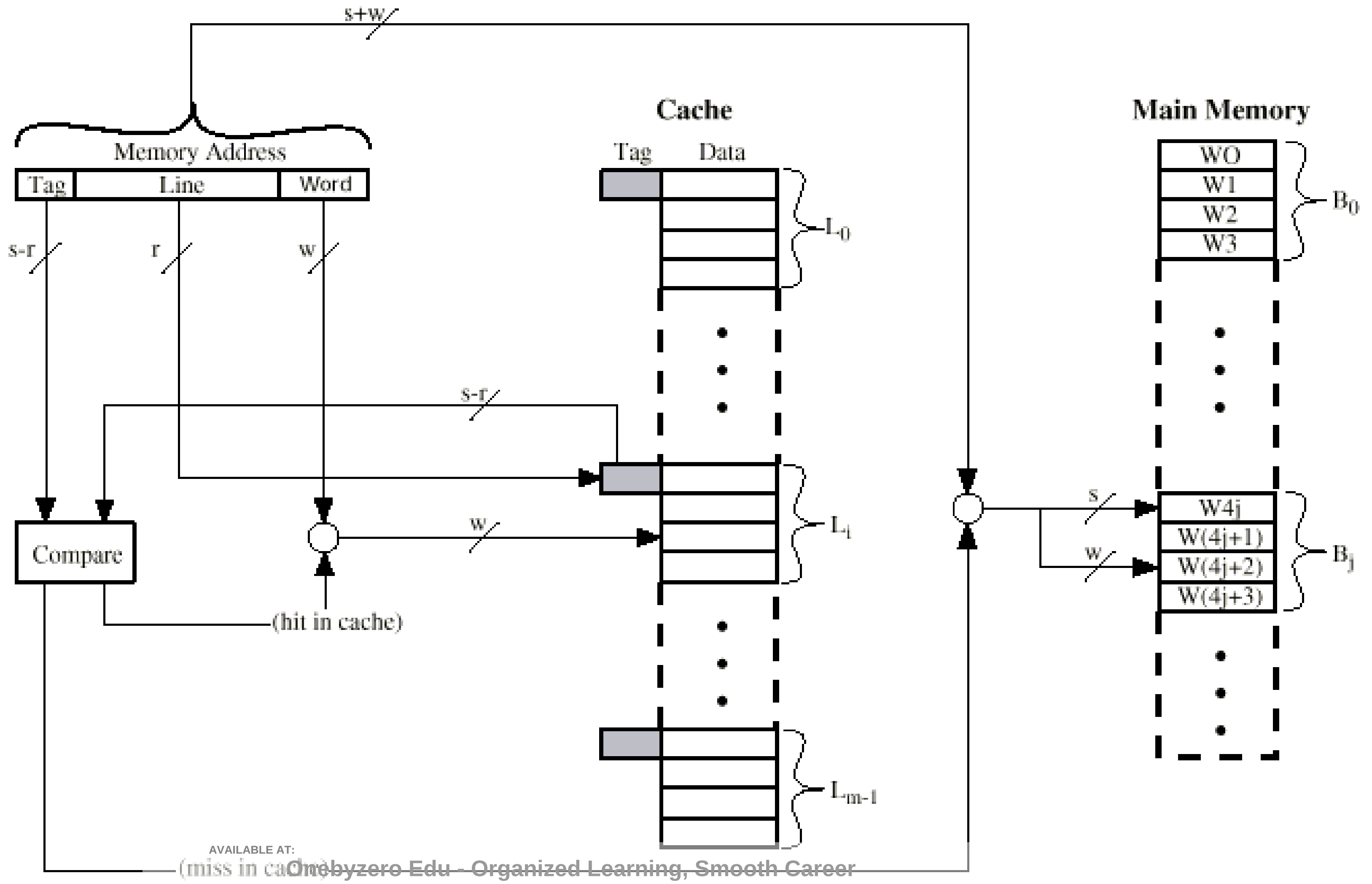
Direct Mapping Cache Organization



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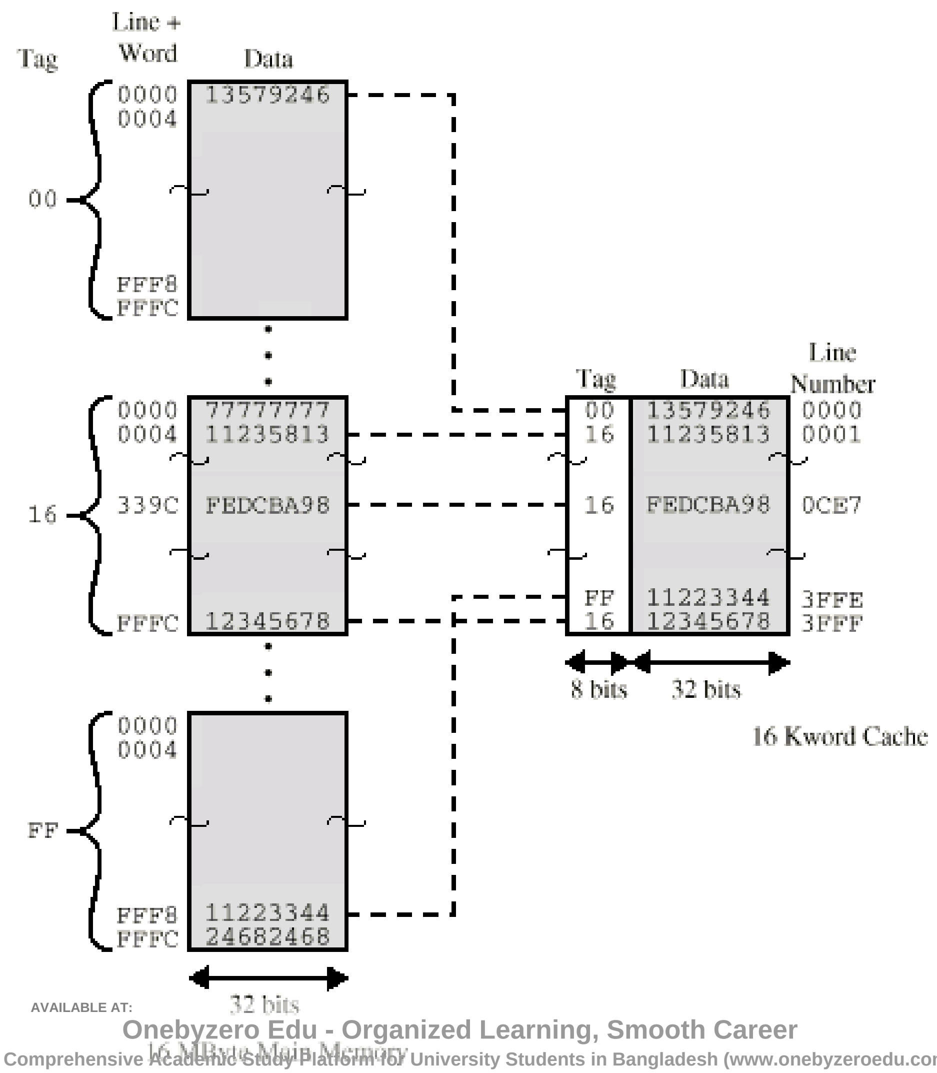
Direct Mapping Example



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Direct Mapping pros & cons

- Simple
- Inexpensive
- Fixed location for given block
  - If a program accesses 2 blocks that map to the same line repeatedly, cache misses are very high

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Associative Mapping

- ⌘A main memory block can load into any line of cache
- ⌘Memory address is interpreted as tag and word
- ⌘Tag uniquely identifies block of memory
- ⌘Every line’s tag is examined for a match
- ⌘Cache searching gets expensive

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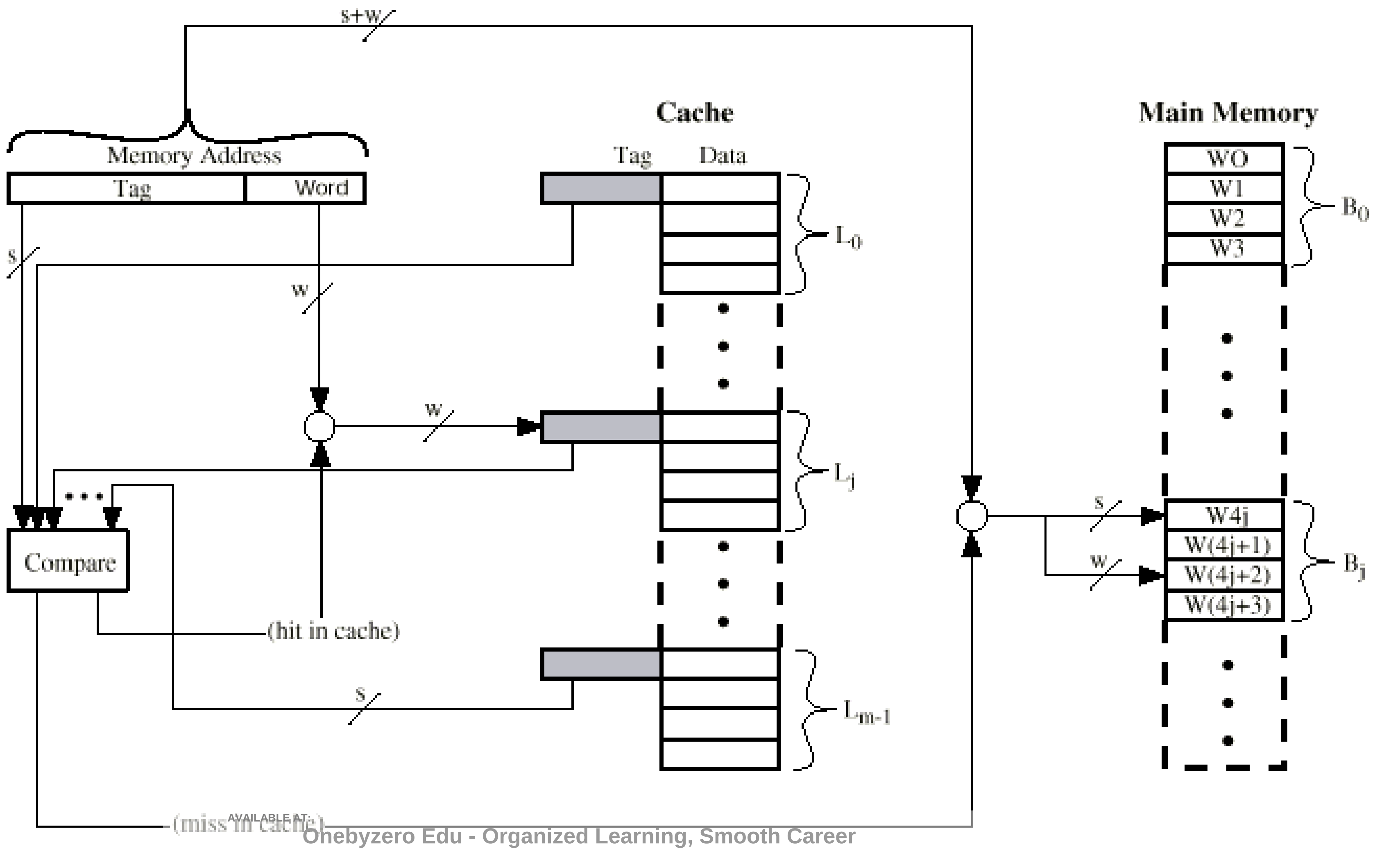
Fully Associative Cache Organization



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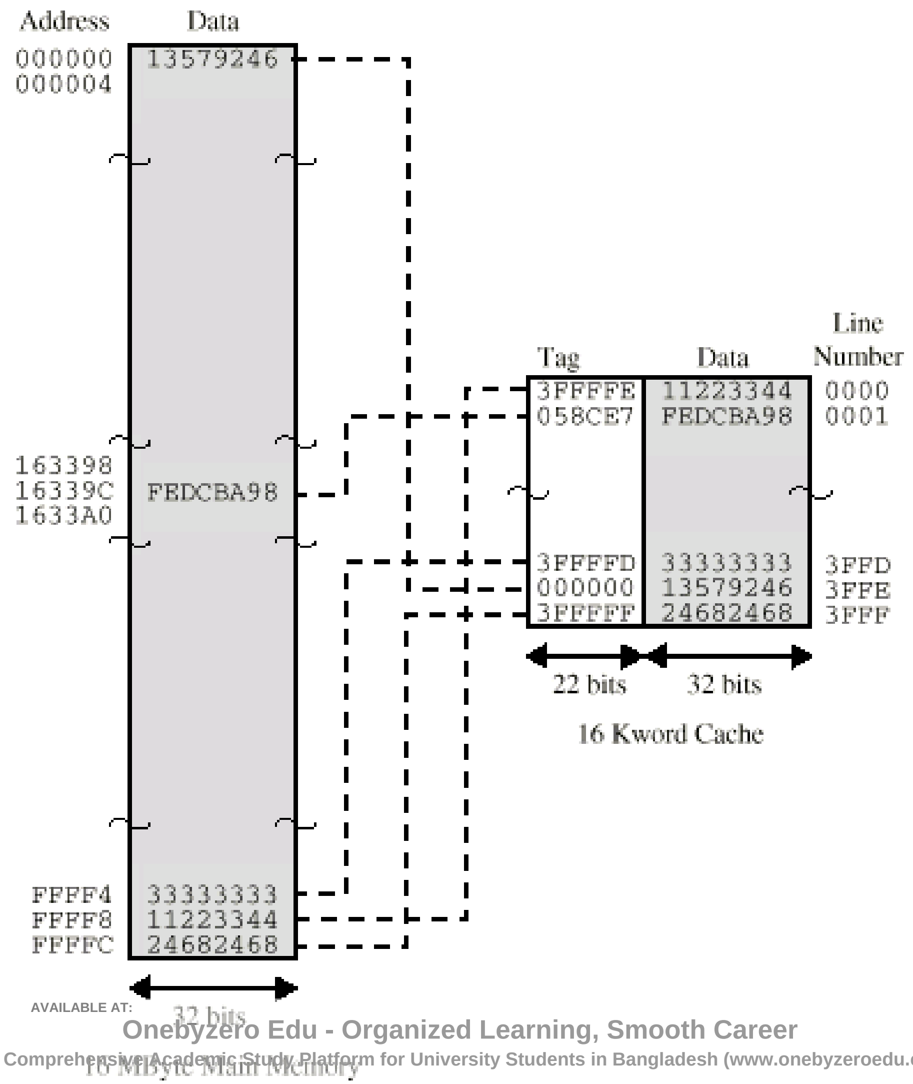
Associative Mapping Example



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Associative Mapping Address Structure

Tag 22 bit	Word 2 bit

- 22 bit tag stored with each 32 bit block of data
- Compare tag field with tag entry in cache to check for hit
- Least significant 2 bits of address identify which 16 bit word is required from 32 bit data block
- e.g.
  - Address Tag Data Cache line
  - FFFFFC FFFFFC 24682468 3FFF

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Set Associative Mapping

- Cache is divided into a number of sets
- Each set contains a number of lines
- A given block maps to any line in a given set
  - e.g. Block B can be in any line of set i
- e.g. 2 lines per set
  - 2 way associative mapping
  - A given block can be in one of 2 lines in only one set

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Set Associative Mapping Example

- 13 bit set number
- Block number in main memory is modulo 2^{13}
- 000000, 00A000, 00B000, 00C000 … map to same set

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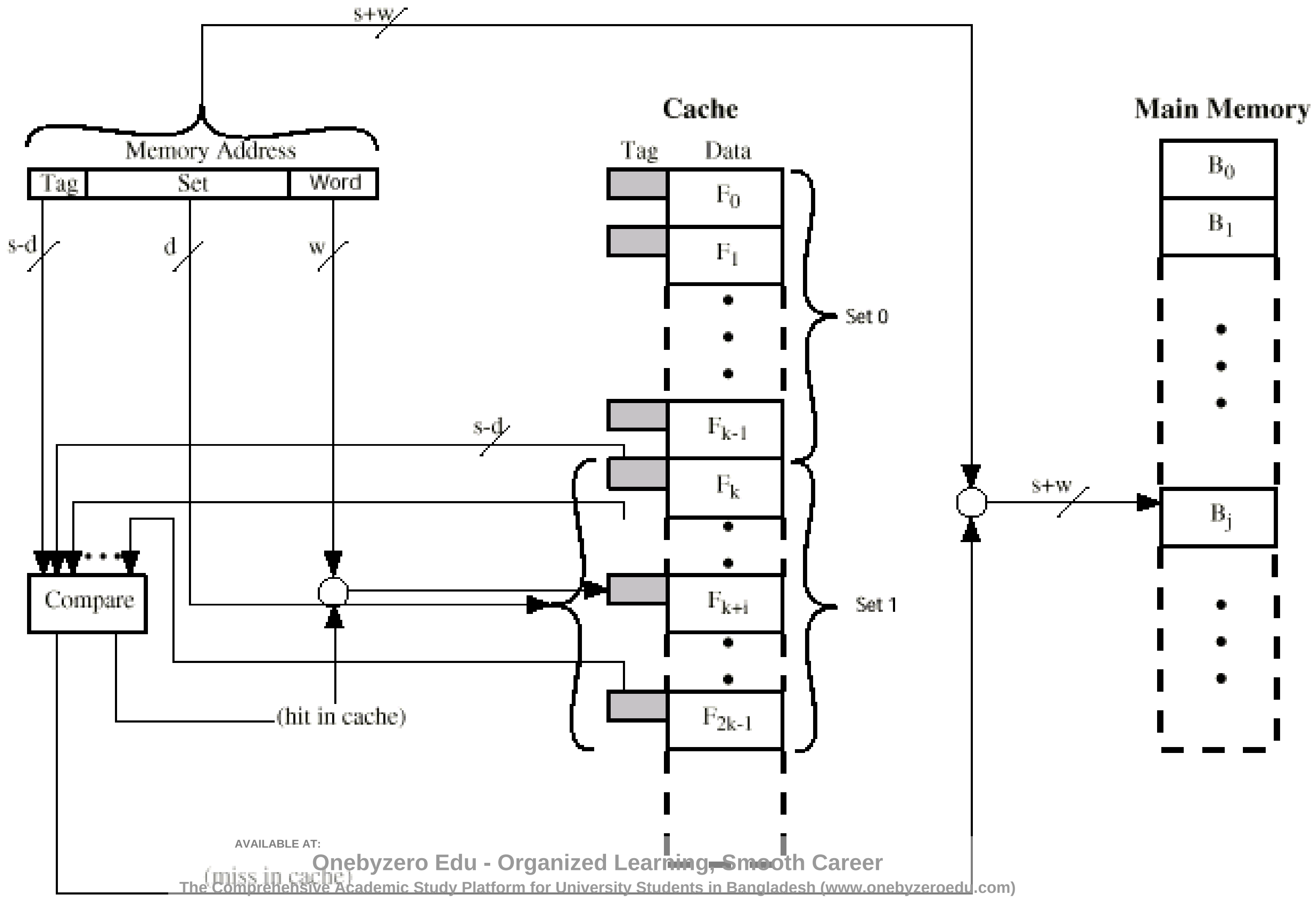
Two Way Set Associative Cache Organization



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Set Associative Mapping Address Structure

Tag 9 bit	Set 13 bit	Word 2 bit

- Use set field to determine cache set to look in
- Compare tag field to see if we have a hit
- e.g

Address	Tag	Data	Set number
1FF 7FFC	1FF	12345678	1FFF
001 7FFC	001	11223344	1FFF

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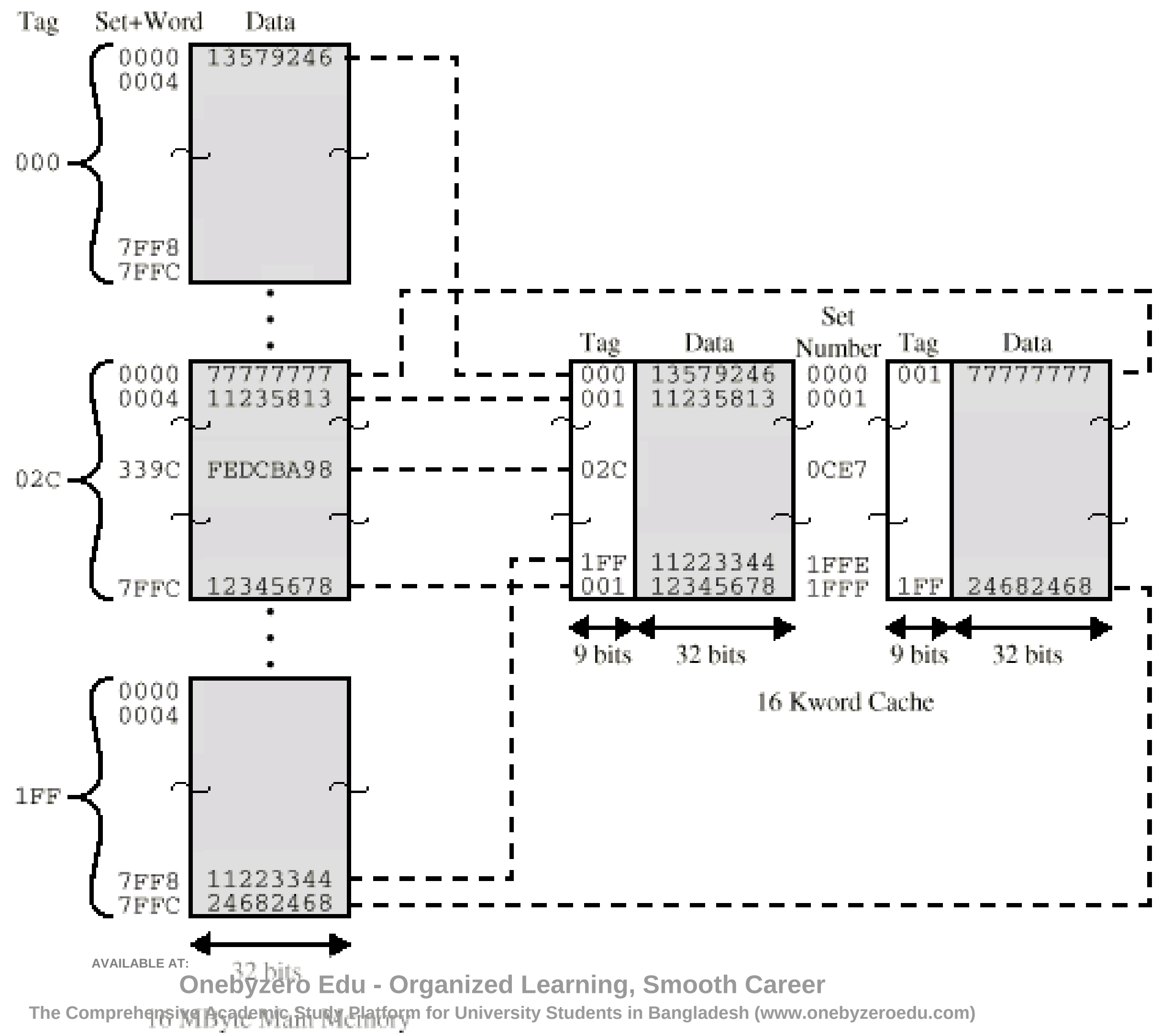
Two Way Set Associative Mapping Example



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Replacement Algorithms (1) Direct mapping

- ⌘No choice
- ⌘Each block only maps to one line
- ⌘Replace that line

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Replacement Algorithms (2) Associative & Set Associative

- Hardware implemented algorithm (speed)
- Least Recently used (LRU)
- e.g. in 2 way set associative
  - Which of the 2 block is lru?
- First in first out (FIFO)
  - replace block that has been in cache longest
- Least frequently used
  - replace block which has had fewest hits
- Random

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Write Policy

- Must not overwrite a cache block unless main memory is up to date
- Multiple CPUs may have individual caches
- I/O may address main memory directly

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Write through

- All writes go to main memory as well as cache
- Multiple CPUs can monitor main memory traffic to keep local (to CPU) cache up to date
- Lots of traffic
- Slows down writes

- Remember bogus write through caches!

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Write back

- ⌘Updates initially made in cache only
- ⌘Update bit for cache slot is set when update occurs
- ⌘If block is to be replaced, write to main memory only if update bit is set
- ⌘Other caches get out of sync
- ⌘I/O must access main memory through cache
- ⌘N.B. 15% of memory references are writes

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Pentium Cache

- Foreground reading
- Find out detail of Pentium II cache systems
- NOT just from Stallings!

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Newer RAM Technology (1)

- Basic DRAM same since first RAM chips
- Enhanced DRAM
  - Contains small SRAM as well
  - SRAM holds last line read (c.f. Cache!)
- Cache DRAM
  - Larger SRAM component
  - Use as cache or serial buffer

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Newer RAM Technology (2)

- Synchronous DRAM (SDRAM)
  - currently on DIMMs
  - Access is synchronized with an external clock
  - Address is presented to RAM
  - RAM finds data (CPU waits in conventional DRAM)
  - Since SDRAM moves data in time with system clock, CPU knows when data will be ready
  - CPU does not have to wait, it can do something else
  - Burst mode allows SDRAM to set up stream of data and fire it out in block

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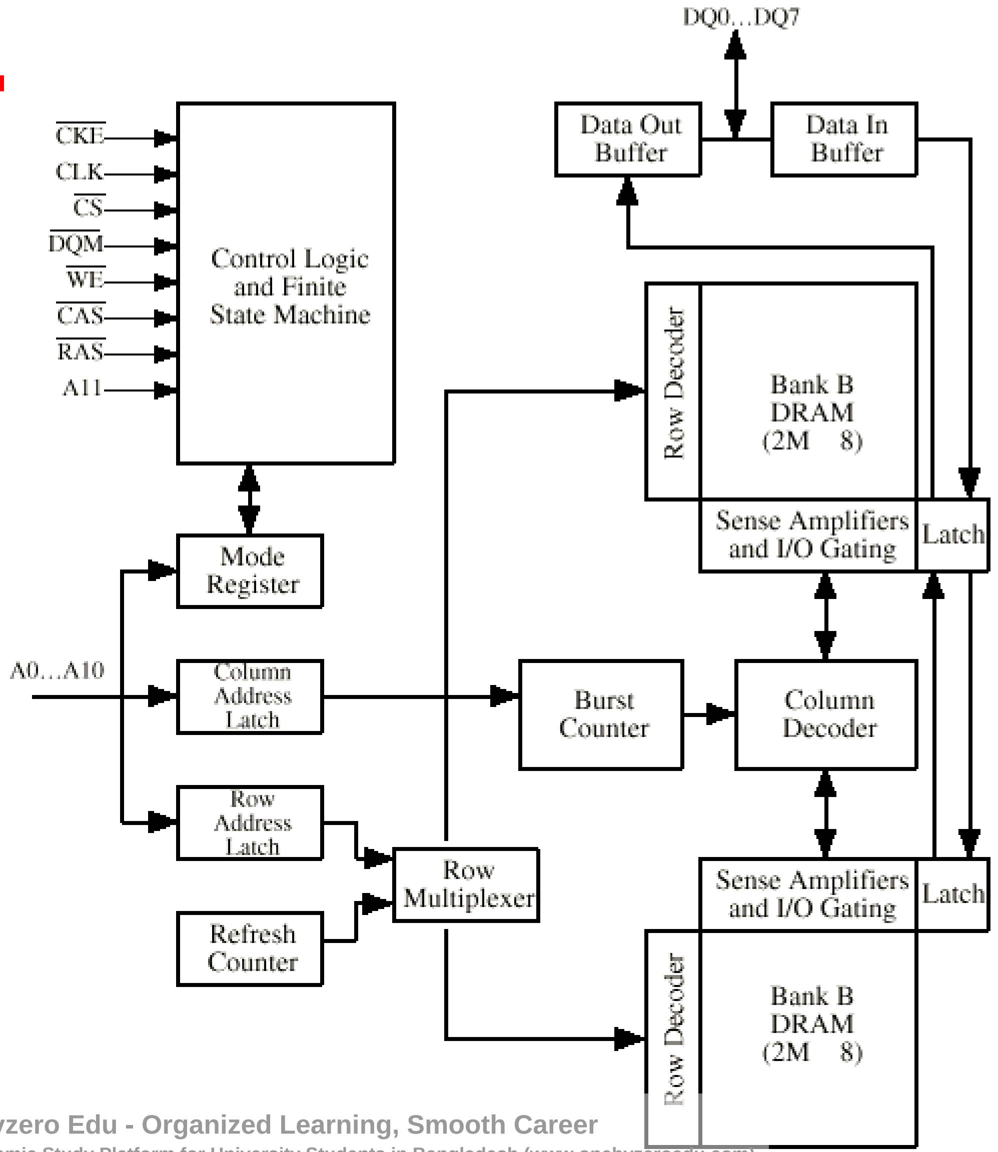
SDRAM



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Newer RAM Technology (3)

- Foreground reading
- Check out any other RAM you can find
- See Web site:
  - The RAM Guide

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